

WISMO-CDMA

Dual-Band Embedded Module Hardware Specification

Reference: **WM_Dpt_Projet_Type_N° ordre**

Level : **1.5**

Date: **17 May 2002**

PRELIMINARY

Document Information

Level	Date	History of the evolution	Writer
Rev 1	12/17/01		CNowak
Rev 2	03/07/02		CNowak

	Name	Function	Date	Signature
Written by	CNowak			
Checked by				
Approved by				

Distribution List

-

Contents

1	WISMOCDMA Introduction.....	8
1.1	Scope	8
1.2	Applicable Standards	8
1.3	Safety and Governmental Agency Approval	8
2	Product Features.....	9
2.1	General Specifications WISMOCDMA module:	9
2.2	RF Features.....	9
2.3	Baseband Features	9
3	Detailed Description	11
3.1	RF	11
3.1.1	Transmitter	11
3.1.1.1	RFT3100-1.....	11
3.1.1.2	Transmitter Specification	12
3.1.2	Receiver 12	12
3.1.2.1	RFR3100	12
3.1.2.2	IFR3000	12
3.1.2.3	Receiver Specification	13
3.1.3	Synthesizer.....	13
3.2	Baseband	13
3.2.1	Power	14
3.2.1.1	ON-OFF	14
3.2.1.1.1	Mode One	14
3.2.1.1.2	Mode Two	15
3.2.1.1.3	Mode Three.....	15
3.2.1.2	Vcc_Out.....	15
3.2.1.3	Charging	15
3.2.2	Digital	15
3.2.2.1	MSM5101	15
3.2.2.2	Memory	15
3.2.3	System Connector.....	16
3.2.3.1	System Connector Description	16
3.2.3.2	I/O Description Parameters	16
3.2.3.3	System Connector Names and Pinouts.....	17
3.2.3.4	GPx_INT	19
3.2.3.5	Keypad.....	20
3.2.3.6	I/O Interfaces	21
3.2.3.6.1	UART – 1	21
3.2.3.6.2	UART – 2	22

3.2.3.6.3	R-UIM	22
3.2.3.6.4	USB	24
3.2.3.6.5	LCD	26
3.2.3.7	General Purpose ADC	26
3.2.3.8	Audio	27
3.2.3.8.1	MIC	27
3.2.3.8.2	Speaker	28
3.2.3.8.3	Ringer	29
3.2.3.8.4	Vibra	30
4	Electrical Specification	31
4.1	DC Electrical Specifications	31
4.1.1	Absolute Maximum Ratings	31
4.1.2	Recommended Operating Conditions	31
4.1.3	DC Characteristics	32
4.2	Power Consumption	33
4.3	Timing Characteristics	33
5	Mechanical	34
5.1	PCB dimension	34

Figures

Figure 3-1	RF Block Diagram	11
Figure 3-2	Baseband Block Diagram	14
Figure 3-3	Interrupt Sense Circuit	20
Figure 3-4	Multiplexing Arrangement for Keypad COLs	21
Figure 3-5	Multiplexing Arrangement for UART-2	22
Figure 3-6	Multiplexing Arrangement for R-UIM	23
Figure 3-7	Multiplexing Arrangement for USB	24
Figure 3-8	Example Connections for Philips PDIUSBP11 Transceiver	25
Figure 3-9	Example Connections for Micrel MIC2550 Transceiver	25
Figure 3-10	MIC_1 Differential Interface	28
Figure 3-11	MIC_2 Single-Ended Interface	28
Figure 3-12	SPK_1 Differential Interface	29
Figure 3-13	SPK_2 Single-Ended Interface	29
Figure 3-14	Ringer Circuit	30

Tables

Table 3-1	I/O Pin Parameters	16
Table 3-2	System Connector Pin Assignment	17
Table 3-3	Signal Name and Alternate Function	19
Table 3-4	UART-1 Pin Names and Numbers	21
Table 3-5	LCD Pin Numbers and Names	26
Table 3-6	GPADC Analog Input Spec.	27
Table 4-1	Absolute Maximum Ratings	31
Table 4-2	Recommended Operating Conditions	31
Table 4-3	DC Characteristics	32
Table 4-4	Power Consumption	33

Overview

1 WISMOCDMA Introduction

1.1 Scope

Code Division Multiple Access, a cellular technology also known as **IS-95**, competes with GSM technology for dominance in the cellular world. There are now different variations, but the original CDMA is now known as **cdmaOne**. Developed originally by Qualcomm and enhanced by Ericsson, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme. The Telecommunications Industry Association (TIA) adopted CDMA, in 1993. By December 2000, there were 27 million subscribers on **cdmaOne** systems worldwide. Over 35 countries have either commercial or trial activity ongoing. Enhancing today's data capabilities is the 1XRTT CDMA standard - this next evolutionary step for **cdmaOne** operators will provide packet data rates up to 144 kbps, significant capacity increases as well as extended battery life for handsets. This development is based on 1XRTT technology into an embedded module.

1.2 Applicable Standards

- 14.4 kbps Data Services IS-707
- 14.4 kbps Radio Link Protocol and Inter-band Operations TSB-74
- Addendum 1 (to the IS-2000 standard) TIA/EIA/IS-2000 PN-4756 (Ballot Version)
- CDMA Data Services Revision for IS-95B IS-707A
- CDMA Data Services Revision for cdma2000 Rel. 0 IS-707A-1
- CDMA Dual-Mode Air Interface Standard IS-95A, IS-95B
- CDMA Voice Coder Standards IS-96
- cdma2000: Signaling Layer 2 Standard for Spread Spectrum Systems
- PN-4430 (Ballot Resolution Version 0.14, to be published as TIA/EIA-IS-2000.4)
- IS-95 adapted for 1900 MHz frequency band J-STD-008
- Medium Access Control (MAC) for cdma2000 Spread
- PN-4429 (Ballot Resolution Version, to be published as TIA/EIA-IS-2000.3)
- TIA/EIA-95-B
- Option 3: Enhanced Variable Rate (max 8 kbps) Voice Coder (EVRC) IS-127
- OTA Update: Roaming System Selection and Programming Block IS-683A
- Physical Layer Standard for cdma2000 Spread Spectrum Systems PN-4428 (Ballot Resolution Version, to be published as TIA/EIA-IS-2000.2)
- Short Message Service including mobile origination IS-637A
- Upper Layer (Layer3) Signaling Standard for cdma2000 Spread Spectrum Systems PN-4431 (Ballot Resolution Version 1.06, to be published as TIA/EIA-IS-2000.5)

1.3 Safety and Governmental Agency Approval

The WISMOCDMA CDMA module shall comply with the following standards or guidelines:

- Formal Qualification Test, as mutually specified by Wavecom and manufacturer.
- IEC950, for electrical safety
- UL950, for electrical safety
- FCC Part 15B power supply, conducted requirements only
- FCC Part 22 (800 MHz), Part 24 (1900 MHz)
- SAR

- CSA for Canada
- Canada IC-133
- CDG 1, 2, 3
- IS-98D

2 Product Features

2.1 General Specifications WISMOCDMA module:

- | | |
|---------------------------------|--|
| - Support voice communication | Interface connector. |
| - Wireless interface | CDMA2000 (IS-95C) |
| - Wireless data rate | 144 kbps |
| - Supporting OS | All via AT Commands MS Windows CE 3.0 |
| - Current consumption | |
| Receive Mode | Max 150mA |
| Transmission Mode | Max 770mA |
| Sleep Mode | 3.8mA |
| - Dimension | 58 x 32 x 5.9 mm (Including shielding) |
| - Weight | |
| - Operating Temperature | -30°C ~ +60°C |
| - Mode | CDMA |
| - Band (CDMA2000) – (Dual Band) | |
| Band class 0 | (800MHz) |
| Band class 1 | (USPCS 1900MHz) |
| - Antenna | RF Pad |
| - Test | RF Connector |

2.2 RF Features

- WISMOCDMA CDMA module shall support Rx and Tx specifications per IS-98D and IS-95A/IS-95B, Sections 2.1.2 through 2.1.3.1.1, 2.1.4, 2.2.3, and 2.1.3.1.9 through 2.1.3.1.10 as well as the corresponding portions of Section 6.
- WISMOCDMA CDMA module shall pass CDG-2 and CDG-3 interoperability testing specifications on Lucent, Nortel and Motorola infrastructures.

2.3 Baseband Features

The WISMOCDMA uses the Qualcomm MSM5105 and PM1000 for its Baseband hardware. The features of this solution include:

MSM5105

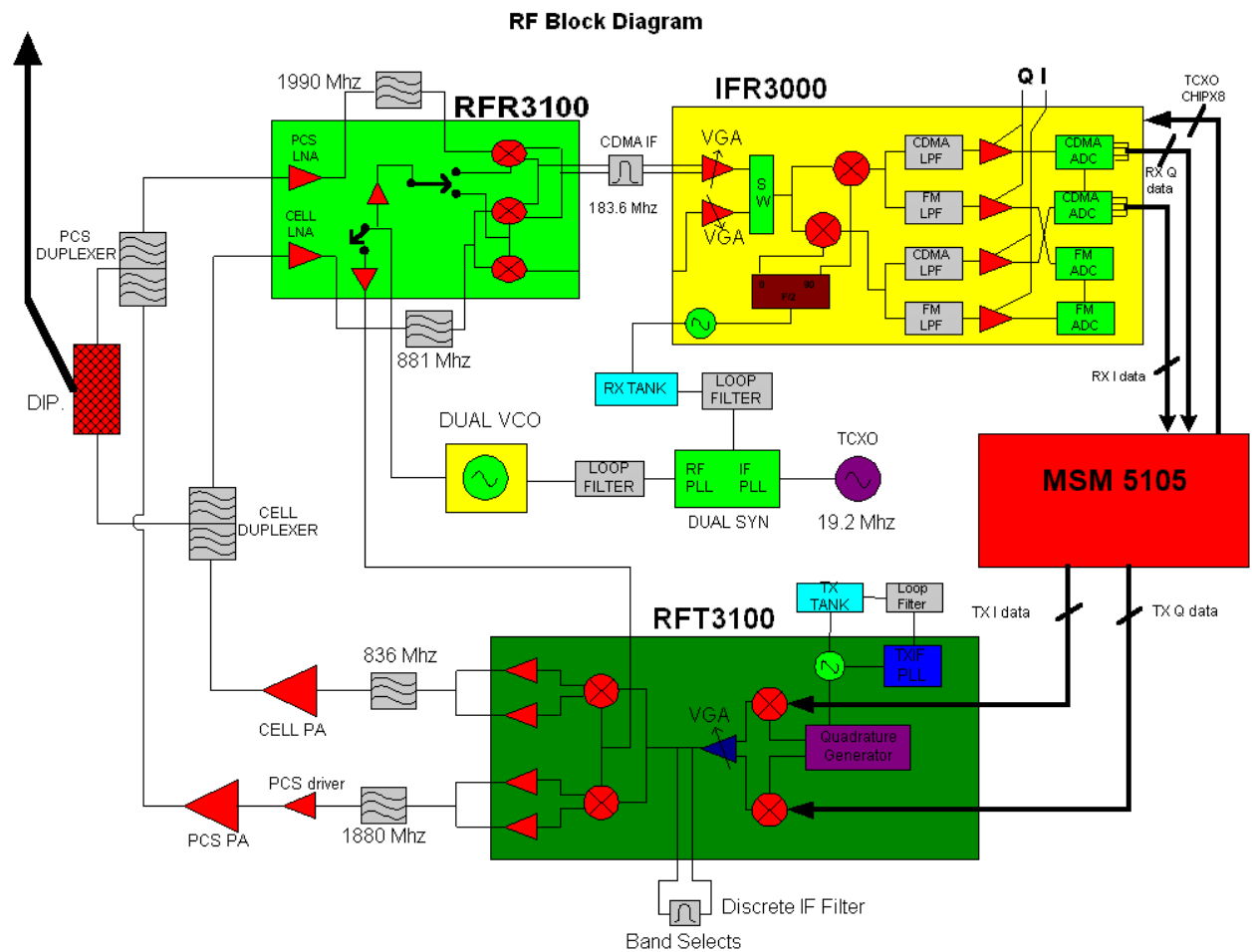
- Embedded QDSP2000 digital signal processor core, enabling features such as voice recognition, voice memo, speech compression, acoustic echo cancellation,
- 16-bit wide Flash and SRAM support
- Standard MIDI ringer
- Voice mode V1 (EVRC, IS-96A, PureVoice^a), all radio configurations
- High-speed data using both fundamental and supplemental channels
- ARM7TDMI
- General-Purpose Interface Bus
- Microprocessor power down modes

- Internal watchdog and sleep timers
- Battery Management
- Charge Control
- Linear voltage regulation
- Programmable voltages for Digital and RF
- LCD Light driver
- Keypad Light driver
- Ringer driver
- Vibra driver
- RTC circuit
- SBI control

3 Detailed Description

3.1 RF

Figure 3-1 RF Block Diagram



3.1.1 Transmitter

3.1.1.1 RFT3100-1

34	GPIO_INT_2	BS-PU2[3]	DTR	
35-A	GPIO_INT_7	BS		
36-A	GPIO_INT_3	BS-PU2[3]	DSR	
50	GPIO_INT_40	BS-PU2[3]		
51	GPIO_INT_19	BS-PU3	DCD	
52	GPIO_INT_9	BS-PD3-KP		USB-SUSPND
53	GPIO_INT_8	BS-		
54	GPIO_INT_18	BS-PD1	RI	

3.2.3.5 Keypad

The WISMOCDMA module provides for a 5 x 5 keypad matrix. The five Rows are used to sense key contact closure when connected to an external keypad. The Row pins have active pull-ups built in to reduce the need for external components. ROW pins are dedicated inputs that are mapped to the Interrupt Controller. If the Row pins are used in a keypad they can still be used as interrupt inputs. See Figure 3-3 for Interrupt sense circuit. The five Columns are multi-function GPIO_INT pins. When the GPIO_INT pins are used as Columns their other functions are unavailable. Figure 3-4 shows the Row and Column pins on the System connector.

Figure 3-3 Interrupt Sense Circuit

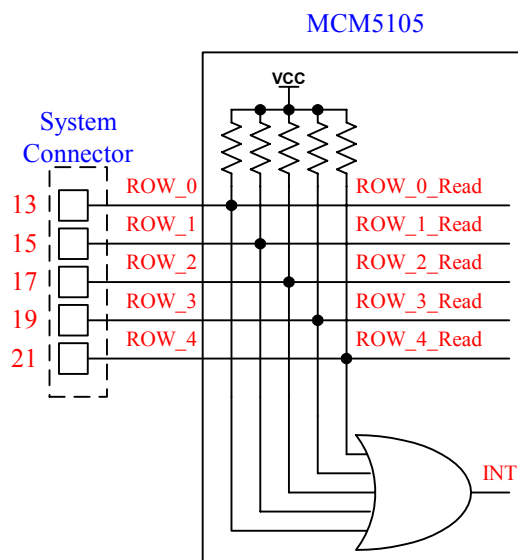
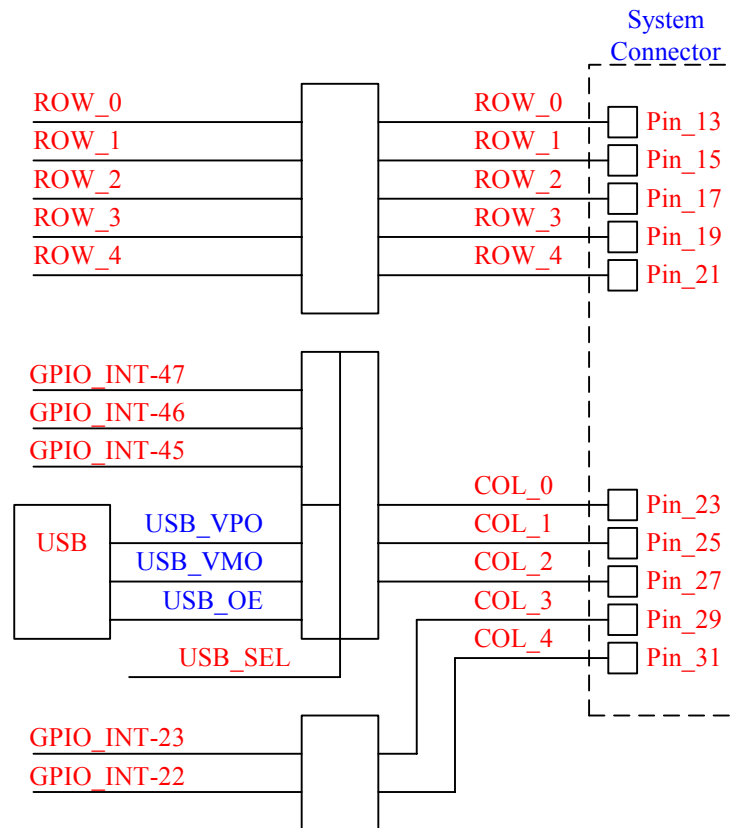


Figure 3-4 Multiplexing Arrangement for Keypad COLs



3.2.3.6 I/O Interfaces

The WISMOCDMA module has 5 external communication Interfaces. Each Interface and its functions are described below. Not all the Interfaces can be used at the same time.

3.2.3.6.1 UART – 1

The UART communicates with serial data that conforms to RS-232 interface protocol. The UART is fully configurable by SW. UART_1 has 4 dedicated pins on the System Connector these are shown in Table 3-4

Table 3-4 UART-1 Pin Names and Numbers

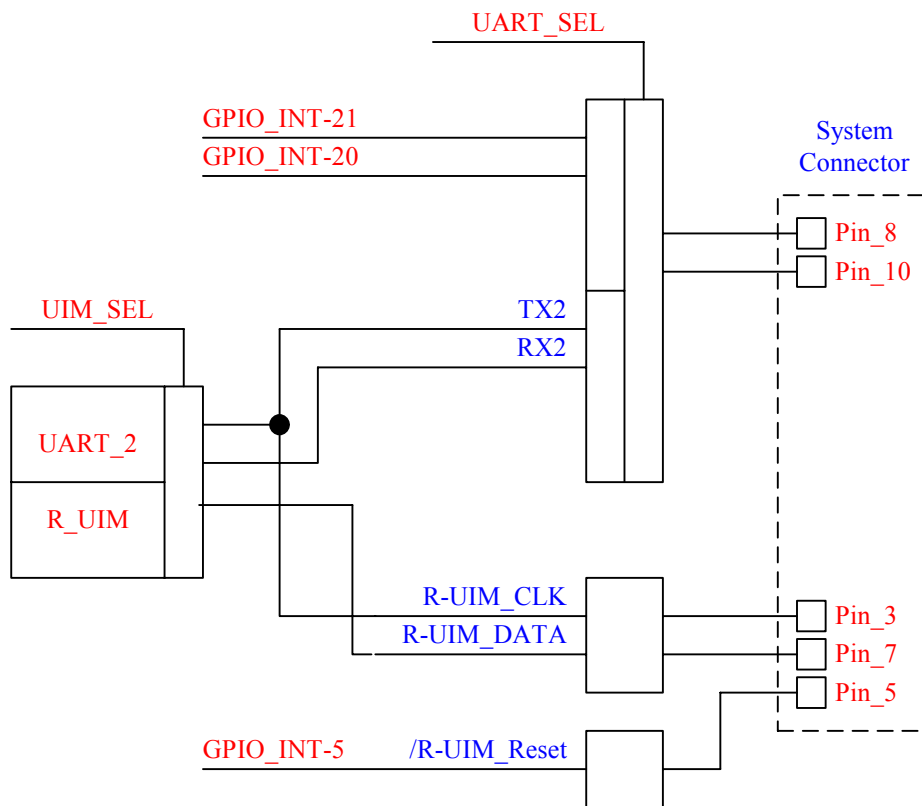
Signal Name	Description	Sys. Conn. #
RS232_RX	Transmit serial data output	32
RS232_TX	Receive serial data input	39
RS232_RTS	Clear to send (INPUT)	30
RS232_CTS	Request to send (OUTPUT)	37

3.2.3.6.2 UART - 2

The UART communicates with serial data that conforms to RS-232 interface protocol. The UART is fully configurable by SW.

UART-2 uses pins 8 and 10 on the System Connector. When UART-2 is selected, R_UIM and GPIO_INT 20 and 21 are not available. When the UART is not selected all GPIO_INT signals and R_UIM signals can be used. Figure 3-5 shows the multiplexing scheme for UART-2.

Figure 3-5 Multiplexing Arrangement for UART-2



3.2.3.6.3 R-UIM

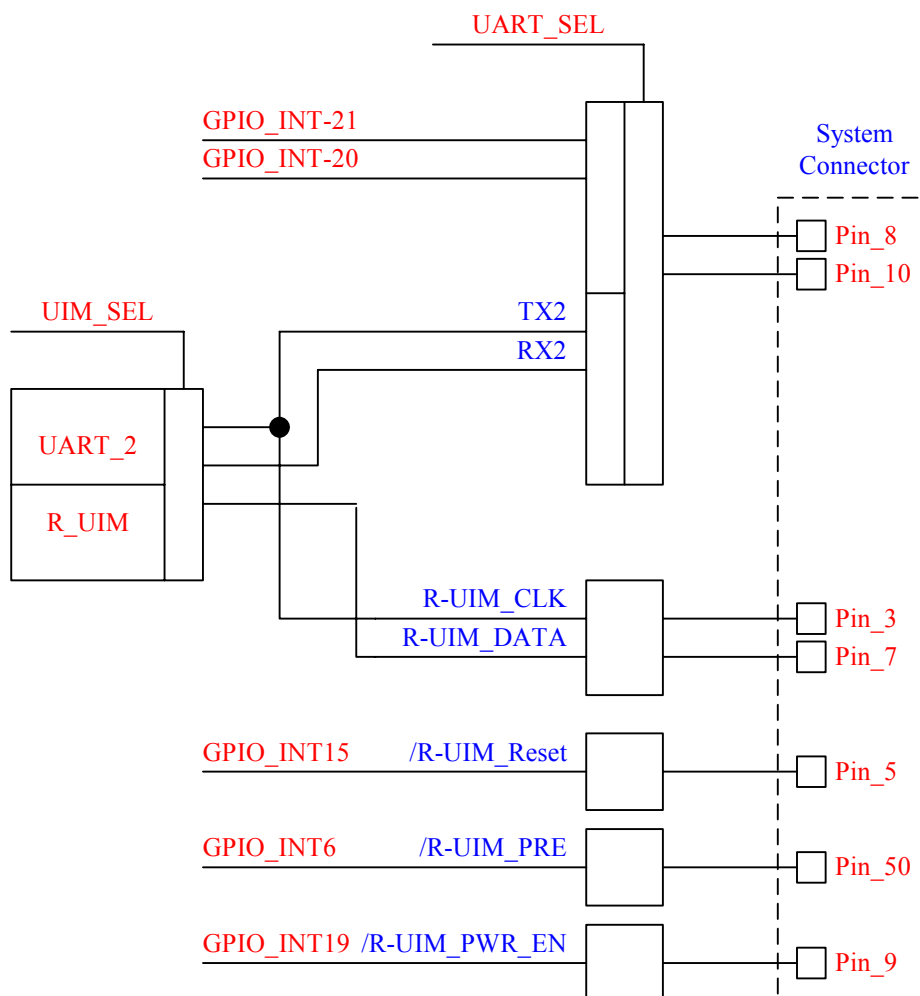
The R-UIM Interface provides for communication with a CDMA smart card. The R-UIM controller shares functions with the UART, as seen in Figure 3-5. When the R-UIM is enabled the UART is disabled, but the GPIO_INT signals available for use.

The R-UIM Interface consists of Clock, Data, Pwr_En, Pre, and Reset signals. The Clock and Data are part of the UART block, but the Pwr_En, Pre, and Reset (Control) signals are GPIO_INT lines. The Control signals are under SW control. When the R-UIM is not in use the Control lines are available for User defined functions. Figure 3-6 shows the multiplexing scheme for R-UIM.

R-UIM power is controlled by the Pwr_En signal. This signal is used to enable an LDO regulator in order to supply power to the R-UIM. The R-UIM has a constant current draw of 50 mAs and can spike to 50 mAs above this level. Refer to the R-UIM spec. for further details.

The R-UIM Present signal is not defined in the R-UIM space. This signal maybe a function of the R-UIM card holder. This signal need not be used as the SW will be configured for an R-UIM if one is capable of being used.

Figure 3-6 Multiplexing Arrangement for R-UIM

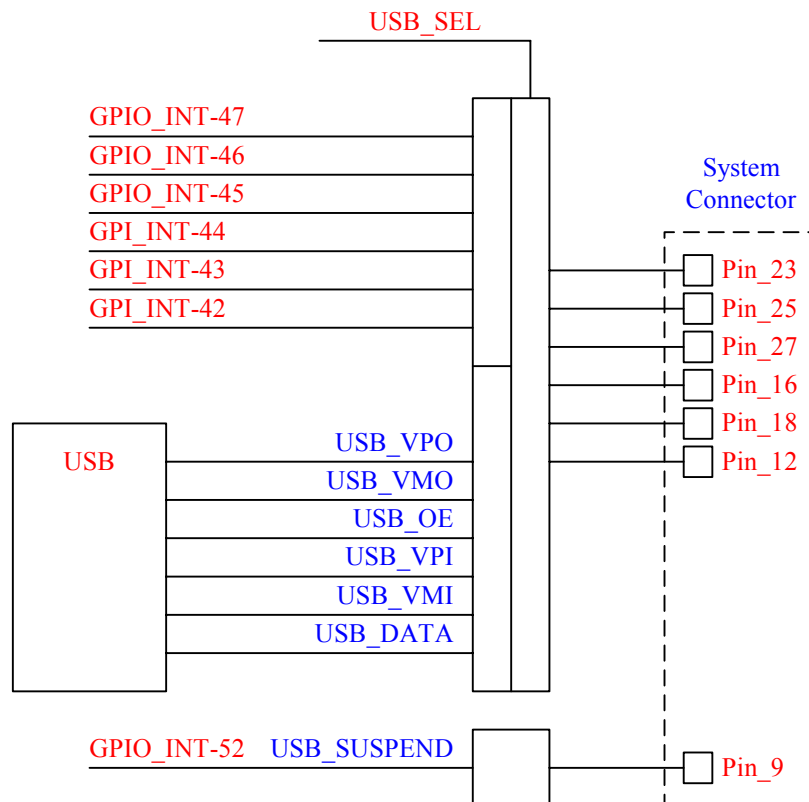


3.2.3.6.4 USB

The WISMOCDMA System Connector contains a USB interface to provide an efficient interconnection between modem and OEM products. The WISMOCDMA USB interface is USB Rev 1.1 compliant. An external USB transceiver is required to implement the interface.

The USB signals are multiplexed with GPIO_INT [0,1,2,6] and GPI_INT [3,4,5], as selected by SW. When the USB is configured the GPx_INT signals are not available. Figure 3-7 shows the multiplexing scheme for the USB.

Figure 3-7 Multiplexing Arrangement for USB



The USB interface supports connections to transceivers with both separate input and output data pins (Philips PDIUSBP11) or with bi-directional data pins (Micrel MIC2550). Selection of the transceiver type is done by SW.

The following figures show the connections between the System Connector and the two transceivers.

Refer to the appropriate data sheet for each transceiver connection requirements.

Figure 3-8 Example Connections for Philips PDIUSBP11 Transceiver

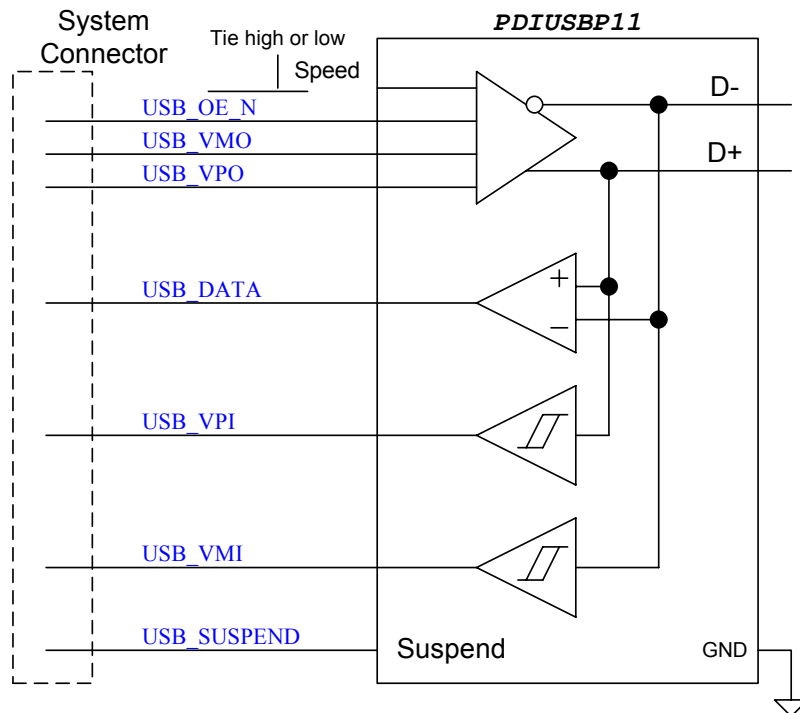
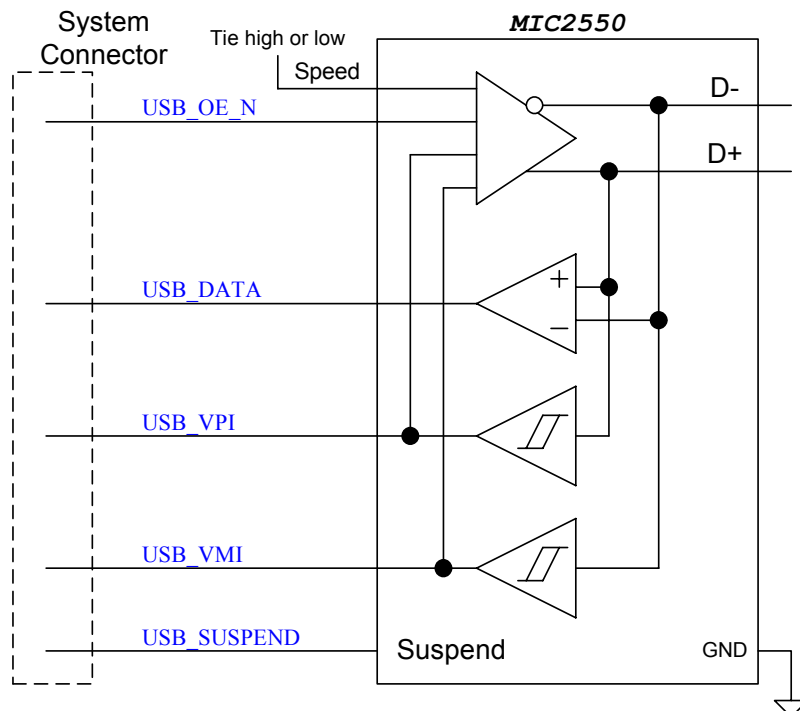


Figure 3-9 Example Connections for Micrel MIC2550 Transceiver



3.2.3.6.5 LCD

The WISMOCDMA module has a parallel interface for connecting to an LCD display. Pin 40 provides power to external circuits that will be powered down when the module is OFF. See Table 3-5 for a complete list of pin names and numbers. Read is available on pin 14 when jumper B is installed. The interface can be used for communication with any device that needs a parallel interface.

Table 3-5 LCD Pin Numbers and Names

Pin #	Signal Name	Function
40	Vcc_OUT	Supply Voltage to LCD
50	LCD_CS	Chip Select
51	LCD_D/C	Data or Command select
53	/WR	Write
9	/RD	Read
36	A1	Address 1
20	Data0	Data 0
22	Data1	Data 1
24	Data2	Data 2
26	Data3	Data 3
28	Data4	Data 4
35	Data5	Data 5
29	Data6	Data 6
31	Data7	Data 7

3.2.3.7 General Purpose ADC

The System Connector has 2 General Purpose Analog-to-Digital Converter (GPADC) inputs. Bat_Temp is found on pin 33 and ADC_0 is on pin 38. The 2 inputs are multiplexed into 1 10-bit ADC, Table 3-6 shows the ADC Analog Input Spec. Software controls, which ADC is being read.

Table 3-6 GPADC Analog Input Spec.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Channel Isolation		$f \leq 1\text{KHz}$	38	50		dB
Top Reference Voltage	VRT		2.425	2.5	2.575	V
Full Scale input voltage			6.5 mV		VRT	V
Input Bandwidth		With 200K source impedance			1.0	KHz
Input Resistance			3			M ohm
Input Capacitance					10	pF

3.2.3.8 Audio

The WISMOCDMA provides audio input and output on the System Connector. The System Connector provides for two MICs and two Speakers to be connected. MIC Bias (MBIAS) is provided to limit current consumption when the primary MIC is not being used.

3.2.3.8.1 MIC

The WISMOCDMA System Connector provides two microphone interfaces to the main board. The primary interface (MIC_1) is a differential interface. The secondary interface (MIC_2) is single-ended. The single-ended application is normally used for the headset. MBIAS is provided in under SW control for tuning the MIC off and there by having minimum power consumption. MBIAS provides 1mA of current at 1.8v DC.

Figure 3-10 is example of a differential microphone in a typical handset application.

Figure 3-10 MIC_1 Differential Interface

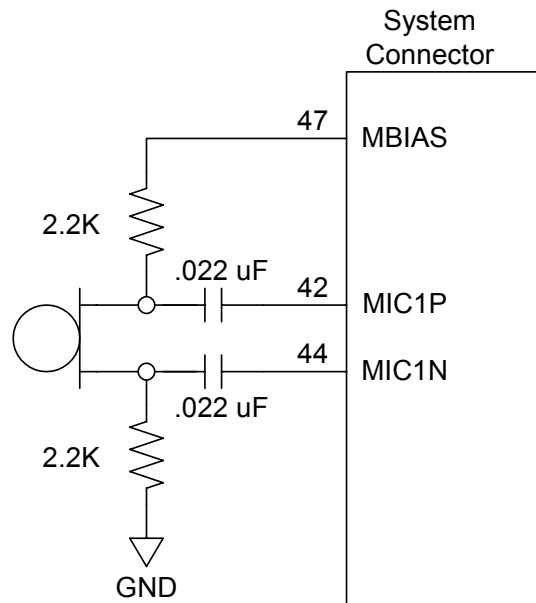
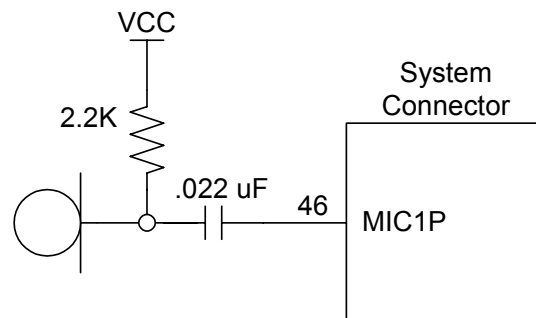


Figure 3-11 is example of a single-ended microphone in a typical handset application.

Figure 3-11 MIC_2 Single-Ended Interface



3.2.3.8.2 Speaker

The WISMOCDMA System Connector provides two speaker interfaces to the main board. The primary interface (SPK_1) is a differential interface. The secondary interface (SPK_2) is single-ended. The single-ended application is normally used for the headset. The output power for the differential SPK_1 is 35mW for a full-scale +3 dBm0 sine wave into a 32-OHM speaker. The

output power for the single-ended SPK_2 is 8.8mW for a full-scale +3 dBm0 sine wave into a 32-OHM speaker.

Figure 3-12 is example of a differential speaker in a typical handset application.

Figure 3-12 SPK_1 Differential Interface

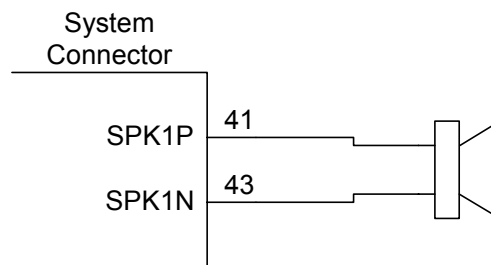
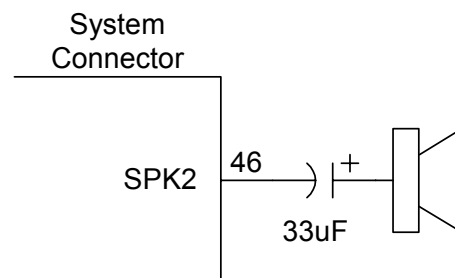


Figure 3-13 is example of a single-ended speaker in a typical handset application.

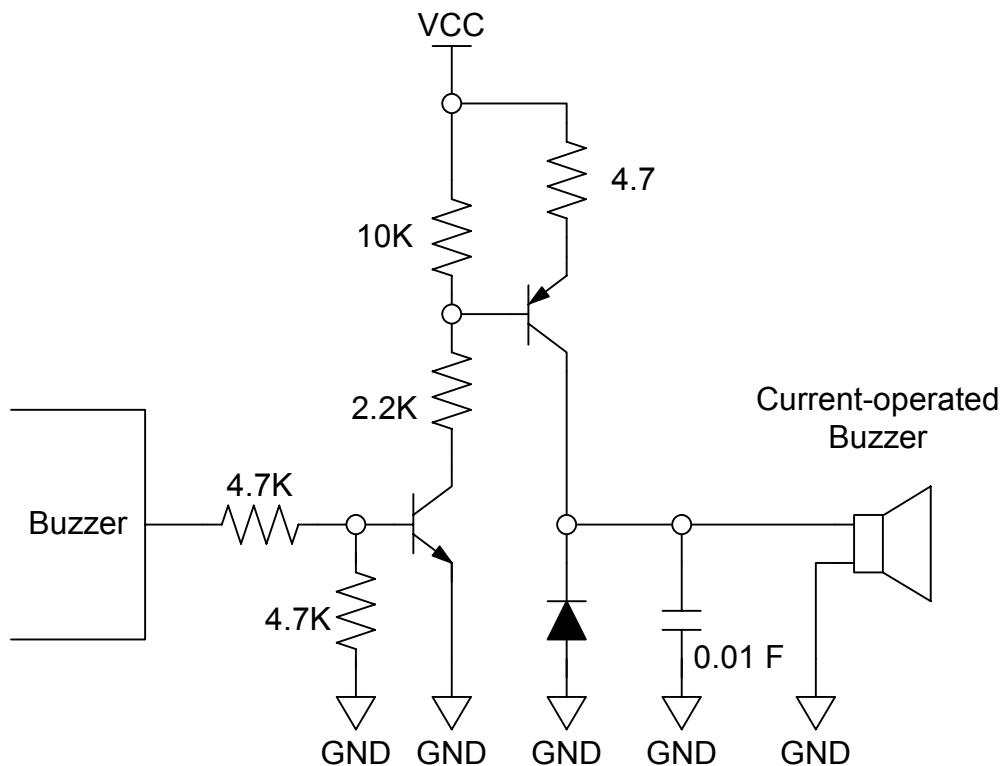
Figure 3-13 SPK_2 Single-Ended Interface



3.2.3.8.3 Ringer

SW controls the Ringer generation circuit. The signal on the Ringer pin of the System Connector is a digital pulse stream. The pulse stream can be a single tone or the sum of two different frequencies or DTMF tones.. Figure 3-14 shows a typical application.

Figure 3-14 Ringer Circuit



3.2.3.8.4 Vibra

The Vibra output is controlled by SW. The signal on the Vibra pin of the System Connector is a digital pulse stream. The circuit needed to run the Vibra motor is dependant on the device being used. Refer to the manufacturers requirements for the appropriate drive circuit.

4 Electrical Specification

4.1 DC Electrical Specifications

4.1.1 Absolute Maximum Ratings

Operating the WISMOCDMA under conditions that exceed those listed in Table 4-1 may result in damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the WISMOCDMA under any other conditions in Table 4-1 is not implied.

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage temperature	TS	-55	+150	C
Supply voltage (Battery)	VBATT	-0.5	4.2	Vdc
Supply voltage (Charger)	CHG_IN	-0.5	4.2	Vdc
Voltage applied to any input or output pin	Vin	-0.5	VCC + 0.5	Vdc

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambiant operating temperature	TS	-30	-	+60	C
Battery supply voltage	VBATT	3.6	-	4.2	Vdc
Charger supply voltage	CHG_IN	4.2	4.2	4.2	Vdc

4.1.3 DC Characteristics

Table 4-3 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level input voltage, CMOS/Schmitt	V_IH	0.65xVccP	-	VccP+0.3	Volts
Low-level input voltage, CMOS/Schmitt	V_IL	-0.3	-	0.35xVccP	Volts
Input high leakage current	I_IH	-	-	2	uA
Input low leakage current	I_IL	-2	-	-	uA
Input high leakage current with pull-down	I_IHPD	10	-	60	uA
Input low leakage current with pull-up	I_ILPU	-60	-	-10	uA
High-level, three-state leakage current	I_OZH	-	-	2	uA
Low-level, three-state leakage current	I_OZL	-2	-	-	uA
High-level, three-state leakage current with pull-down	I_OZHPD	10	-	60	uA
Low-level, three-state leakage current with pull-up	I_OZLPU	-60	-	-10	uA
High-level, three-state leakage current with keeper	I_OZHKP	-25	-	-3	uA
Low-level, three-state leakage current with keeper	I_OZLKP	3	-	25	uA
High-level output voltage, CMOS	V_OH	VccP-0.45	-	VccP	Volts
Low-level output voltage, CMOS	V_OL	0.0	-	0.45	Volts
Input capacitance	C_IN	-	-	15	pF
ADC Full-Scale Input Range	A_FS	GND	-	V_RT	-
ADC Input Serial Resistance	A_ISR	-	5	-	Kohm
ADC Input capacitance	A_C_IN	-	12	-	pF
Input offset voltage at MIC1, MIC2	MV_IO	-5	-	+5	mV
Input bias current at MIC1, MIC2	MI_IB	-200	-	+200	nA
Input capacitance at MIC1, MIC2	M_CI	-	5	-	pF
Input DC Common Mode Voltage	-	0.85	0.9	0.95	V
Microphone Bias supply voltage	MBIAS	1.69	1.8	1.91	V
MBIAS Output DC source current	-	1	1.07	-	mA
Input impedance MIC1, MIC2	M_ZIN	62	72	82	Kohm

4.2 Power Consumption

Table 4-4 Power Consumption

Operating Mode	Band	Average	Units	Notes
		HI_Power = 3.0v		
CDMA RxTx Full Power	Cellular	615	mA	
	PCS	770		
CDMA RxTx Average Power	Cellular	340	mA	
	PCS	445		
CDMA Rx Active	Cellular	TBD	mA	
	PCS	TBD		
CDMA Sleep	Cellular	3.8	mA	
	PCS	3.8		

4.3 Timing Characteristics

5 Mechanical

5.1 PCB dimension

Q2338 WISMO

RF Circuitry Description

Frequency Tuning

This product has factory preset frequency adjustment. There is no frequency field adjustment for this product. In the field, frequency is locked to the base station and controlled by the VCTCXO adjustments to offset any possible error.

Limiting Power

Each mobile is individually calibrated at the factory to ensure a minimum MAX power of 23.933dBm (CDMA) and 25.191dBm (PCS CDMA) MIN power of -50 dBm by employing proper frequency and temperature compensation schemes for both the RX and TX automatic gain control (AGC) amplifier.

Suppression of Spurious Radiations

Spurious and harmonic suppression is achieved by proper design with various filters and sufficient use of metallic shields. Rigorous testing at the factory ensures continuous compliance.

Frequency Stability

A voltage controlled temperature compensated crystal oscillator (VCTCXO) is utilized as a frequency reference for all of the transceiver local oscillators. This crystal oscillator is specified to a frequency stability of +/- 2.5 ppm. The synthesizer lock status is constantly monitored by the microprocessor and transmission is disabled whenever an out of lock condition is detected. The mobile is locked to the base station and makes necessary frequency adjustments on the VCTCXO to correct and frequency errors between the mobile and the base station.

Limiting Modulation

The audio input is sampled, digitally limited, and then filtered to an amplitude and frequency limit the signal applied to the modulator. The device supports IS-2000 for CDMA operation. The device has an operating temperature of -30°C to +60°C. The functions include a compandor, PLL lock detector, filtering of received data, audio signal filtering for signals.

Digital Circuitry Description

MSM Part

MSM5105 is the core element of the CDMA system terminal that includes an ARM7TDMI core. It is made up of a CPU, encoder, interleaver, deinterleaver, viterbi decoder, and vocoder. The CPU controls the terminal operations. Digital voice data that has been inputted is digitally encoded at a variable rate. Then it is convolutionally encoded so error detection and correction can be made. Coded symbols are interleaved in order to cope with multipath-fading. Each data channel is scrambled by the long code PN sequence of the user in order to ensure the confidentiality of the calls.

Moreover, binary quadrature codes are used based on Walsh functions in order to discern each channel. Data created thus are 4-phase modulated by a pair of pilot PN codes and they are used to create I and Q data. When received, I and Q data are demodulated into symbols by the demodulator, and then deinterleaved in reverse. The errors of data received from the Viterbi decoder are detected and corrected. They are voice decoded at the vocoder in order to output the original digital voice data.

The MSM5105 supports Enhanced Variable rate Vocoder (EVRC) operation in addition to the standard 8k and 13k vocoding rates.

Interface Connector Part

Keypad functions are routed to the MSM5105 and checked and processed. In combination with the host device the keypad will illuminate and provide use of LEDs. The terminal status and operation will also be reflected as characters and icons on the display of the attached LCD. All data and control signals including power and ground with external sources or a battery is through the receptacle connector.

Audio Processing Part

MIC signals are routed through the receptacle connector and are inputted into the audio codec within the MSM5105 to be converted onto digital signals. In addition, digital audio outputs are passed from the MSM5105, converted to analog via the audio codec and routed to the earpiece.

Memory Part

16 Mbit Flash Memory and 4 Mbit Static RAM are used. The Flash is the primary storage device containing application code and Non-volatile configuration parameters. The SRAM for run time processing and temporary storage.

Power Supply Part

The device operates on a input voltage range of +3.6 v DC ~ +4.2 v DC. There are a couple of different ways to power on the device. Once one of these methods is used the MSM5105 activates the PS_hold line to hold the power high and turn on all the regulators.

Logic Part

The logic part consist of the CPU, RAM, and ROM. They are as follows:

CPU: ARM7TDMI Core

Flash: 16 Mbits

SRAM: 4 Mbits