

The block diagram illustrates the system architecture centered around the W78E516 CPU (U8). The CPU is connected to an EEPROM (24C16B, U6) via I2C and to an OSILATOR (50Mhz, X1) for clocking. It also interfaces with a 3-wire bus connected to the gmZan1 3-channel ADC Zoom Engine (U1). The CPU's BACK ON/OFF pin is connected to a WS9315 (U10) via the CNT pin, which in turn connects to the BACK pin of CN3. The WS9315 also provides a 5V supply to the CPU. The CPU's IRQ pin is connected to the gmZan1. The gmZan1 is powered by 3.3V from the POWER PART and provides a 3.3V supply to the CPU. The POWER PART includes a MIC4596 and an ACM1085, which is connected to the DC JACK for +12V input. The gmZan1 is connected to the D-SUB15 connector for RGB signals and SYNC. It also interfaces with a DDC1/2B (24LC211, U3) for display control. The gmZan1's EVEN [D23..D0] and ODD [D23..D0] data buses are connected to the SN75LVDS84 (U13), which drives the CN9 connector. The gmZan1's P_SYNC, PIXEL CLOCK, and DISPLAY EN signals are also connected to the display. The gmZan1's KEY INPUT is connected to the OSD KEY. The gmZan1's GREEN/RED LED is connected to the OSD KEY. The gmZan1's LCD PWR CONTROL (SI9933, U12) is connected to the DC JACK for +3.3V/+5V input and provides a PVCC supply to the display. The display is connected to JP2 and JP4 connectors. The AUDIO AMP (U11) is connected to the AUDIO JACK and provides an AUDIO OUT signal.

