Wireless Networks Falcon Packet Radio

RF Radio Set-up and Alignment

Rev 1.0 October 9, 2000

1.0 Introduction and Scope:

This document summarizes the set-up and alignment for the Johnson DataRadio RF module used in the Wireless Networks Falcon Packet Radio. Excerpts are from the Johnson DataRadio Technical Manual.

GENERAL INFORMATION

DM-3473 SYNTHESIZED UHF DATA MODULE GENERAL SPECIFICATIONS

The following general specifications are subject to change without notice.

GENERAL	
Frequency Range	403-434 MHz, 450-480 MHz
Frequency Control	Synthesized
Channel Spacing	12.5/25 kHz
Channel Steps	6.25 kHz or 10 kHz
Mode of Operation	Simplex or Half Duplex
Operating Voltage	+7.2V DC Nominal 6-9 VDC Max. Range
RF Input/Output	MCX Jack Female
Power and Data Interface	18 position dual row socket, 2mm (.0787 in.) pitch
Operating Temperature	-30° to +60° C (-22° to +140° F)
Max Dimensions	2.84" L (7.22 cm), 1.76" (4.47 cm) W, 0.45" (1.14 cm) H
Weight	≤ 40 grams
FCC Compliance	DM-3473 customer must apply
Rx to Tx, Tx to Rx Turnaround Time	≤ 10ms from Rx Enable (pin 7) / Tx Enable (pin 6) to Fc ± 500 Hz (See Section 3 for Tx to Rx, Rx to Tx protocol)
RECEIVER	
Bandwidth	30 MHz 450-480 MHz, 31 MHz 403-434 MHz without retuning
Frequency Stability	±1.5 PPM (-30° to +60° C)
Sensitivity - 12 dB SINAD	-116 dBm (Psophometrically weighted) 60% Max deviation, 1 kHz tone
RF Input Impedance	50 ohms
Spurious and Image Rejection	≥60 dB
Selectivity	≥50 dB (12.5 kHz), 60 dB (25 kHz)
Half IF	≥ 60 dB
	≥ 55 dB 403-408 MHz and 450-455 MHz
Intermodulation	≥60 dB
Conducted Spurious	≤-57 dBm
Receive Current Drain	≤ 60 mA
Receive Lock Time	< 7 ms from last synth enable pulse to lock detect
Rx Data/Audio	
Distortion	≤ 3% (psophometrically weighted)
Bias	2.5 VDC ± 0.5 VDC
Output Level	150 mV rms ± 50 mVrms 1 kHz tone with 60% max. deviation
Response	+1/–3 dB @2.5 kHz, +1/–3 dB @5 kHz
Load Impedance	≥10k ohms
Conducted Spurious Emissions	≤ -57 dBm

TRANSMITTER

Bandwidth	30 MHz 450-480 MHz, 31 MHz 403-434 without retuning
Frequency Stability	±1.5 PPM (-30° to +60° C)
TCXO Coupling	DC 2.5 VDC ± .05 VDC (customer supplied on Pin 10 in both Rx & Tx)
RF Power Output	2W @ 7.2 VDC nominal
RF Output Impedance	50 ohms
Duty Cycle	50%, 5 sec. max transmit
Transmitter Lock Time	≤ 7 ms from last synth enable pulse to lock detect
Tx Attach Time	≤ 3 ms from Tx Enable (pin 6) to 50% power out
Spurious and Harmonic FM	≤-20 dBm
Audio Response	+1/-3 dB from DC to 5 kHz (reference to 1 kHz)
Modulation Distortion	< 3% (psophometrically weighted)
Data Input Impedance	≥ 100 k ohm
Modulation Response Flatness	±3 dB from DC to 5 kHz (reference to 1 kHz -Programmable to ± 1 dB via J201, pin 9) across full RF band
Current Drain	1500 mA maximum, 1200 mA nominal @ 2 watts output (Refer to Section 2 for pin by pin current drain)
Transmitter Stability	No failure or instability at up to 10:1 VSWR
External Modulation Adjust	
Source Impedance	≤ 1 k ohms (pin 9)
External Modulation Adjust	0.5 Vdc - 5.0 Vdc to obtain ± 1.0 dB modulation flatness across RF band (pin 9)
Modulation Capability	200 mVrms (Band 2) to produce 1.5 kHz deviation 180 mVrms (Band 5) to produce 1.5 kHz deviation

SECTION 4

CIRCUIT DESCRIPTION

4.1 GENERAL

4.1.1 INTRODUCTION

The DM-3473 consists of a low dropout regulator power supply, frequency synthesizer and VCO (voltage controlled oscillator), 2 watt RF power amplifier, and dual down conversion FM receiver. A block diagram of the transceiver is located in Figure 4-1 and shows the four major sections of the unit.

The VCO is enclosed by a metal shield and soldered directly to the printed circuit board (PCB). The VCO unit is not field serviceable. The transmitter is also covered by a metal shield to prevent radiation of RF power causing interference. The 3473 comes standard with a reference oscillator stability of + 1.5 PPM over the entire operating temperature range.

4.2 POWER SUPPLY CIRCUIT DESCRIPTION

Main DC power is delivered to the transceiver on pin 5 of the user interface connector (J201). This pin requires a regulated power supply voltage between 6 and 9 VDC. The voltage on this pin powers the on board low drop out regulator U130. The regulator provides constant 5.5 VDC to all of the relevant sections of the transceiver such as the VCO/Synthesizer, Receiver, and Regulator sections of the transmitter. Pins 1 and 2 provide the ground connection of the transceiver.

Pins 3 and 4 of J201 are the main power supply to the RF power amplifier. This voltage is set between 6 and 9 VDC with 7.2 VDC being the nominal voltage to guarantee 2 watts +\-0.4 watts of RF power at the antenna connector. All three pins (3,4,and 5) can be tied together on a customer interface board if the maximum voltage limits are always between 6-9 VDC.

The transmit and receive enable pins (pins 6 and 7) of J201 are a logic voltage input to turn on the transmitter or receiver. The necessary voltage is between 4.5 and 13 VDC for the enable mode. Refer to the programming section 3 for the implementation of the transmit and receive enable pins.

The DM-3473 is equipped with a sleep mode pin for implementing current saving features by the customer when a transceiver requires a standby mode. Pin 8 requires a logic level >2.0 VDC to enable the transceiver, this voltage must always be high when the transceiver is in operation. Pin 8 can be grounded to put the radio to sleep. The transceiver will draw less than one milliampere in sleep mode.

CIRCUIT DESCRIPTION

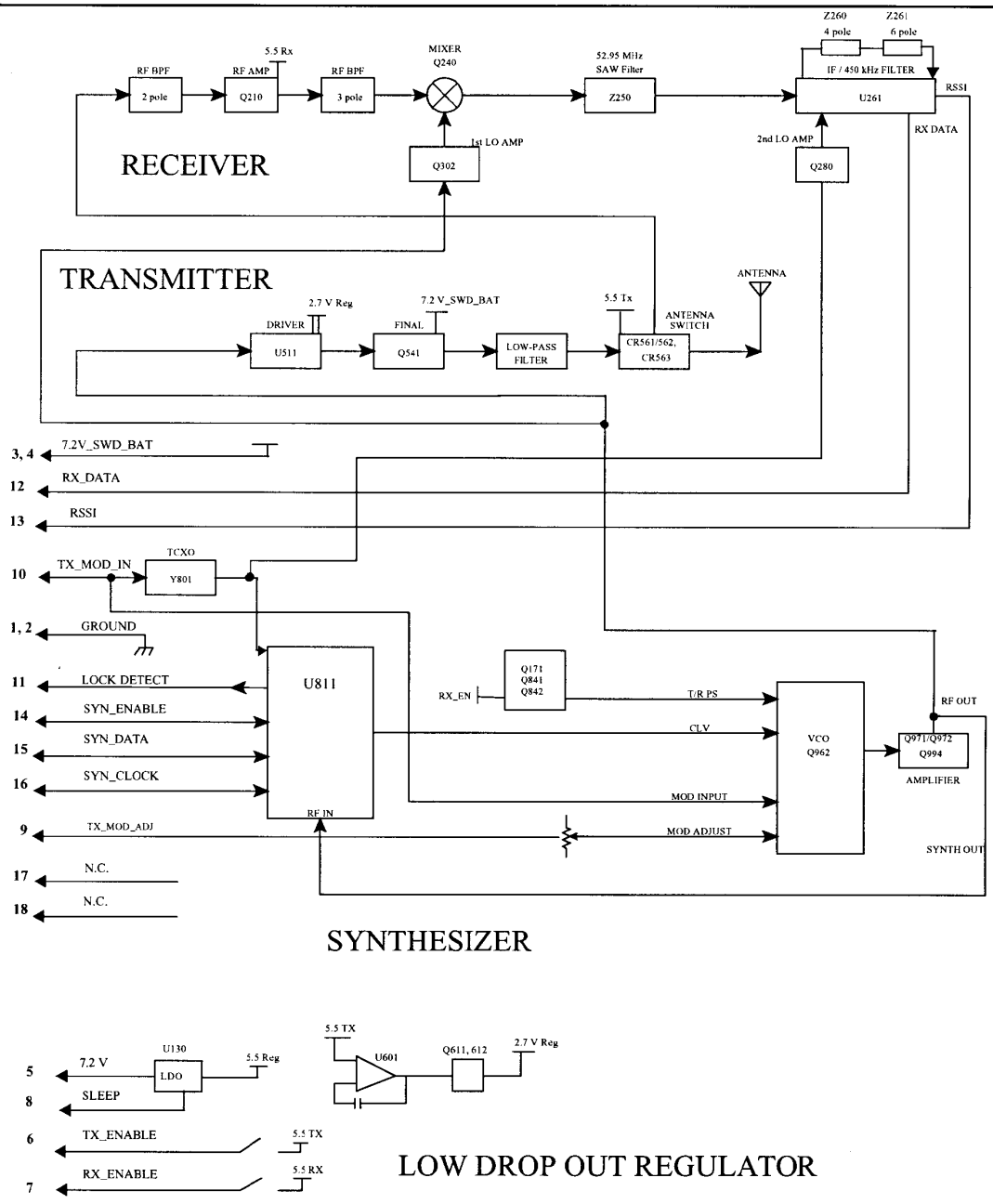

Figure 4-1 DATA TRANSCEIVER BLOCK DIAGRAM

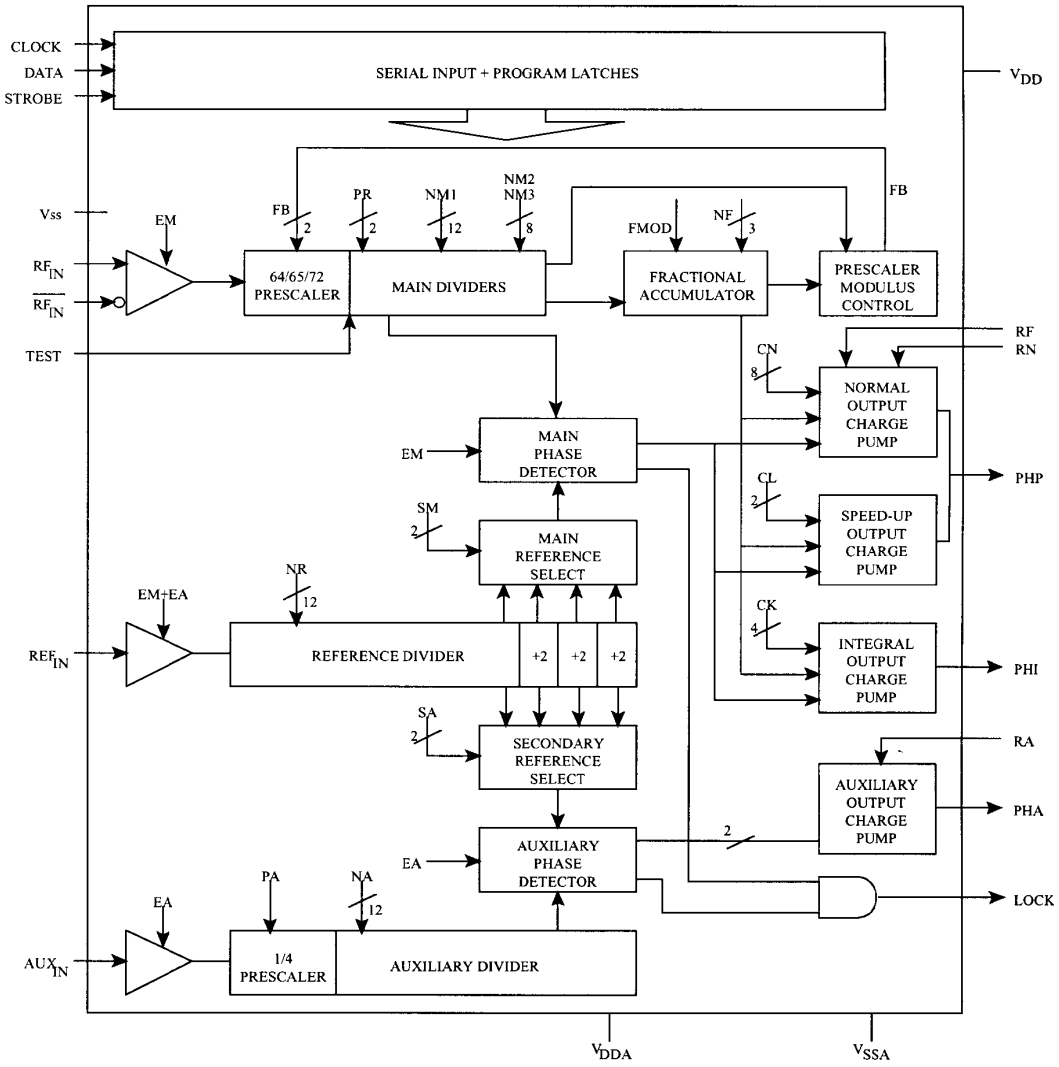

Figure 4-2 U811 SYNTHESIZER BLOCK DIAGRAM

CIRCUIT DESCRIPTION

4.3 SYNTHESIZER/VCO/TX MODULATION

The VCO is an oscillator which can be controlled by an input voltage to oscillate at a desired frequency. The VCO in the 3473 serves either the receiver or the transmitter dependent on the desired operation. The frequency of the VCO for receive mode is 86.85 MHz above the desired receive frequency. For the transmitter the VCO produces the signal corresponding to the desired transmit frequency.

The DC voltage controlling the oscillator frequency is generated by synthesizer IC U811. The VCO control voltage can be measured at test point TP831 on the PCB. When the VCO is locked (>3.5 Vdc on pin 11 of J201) TP831 will measure between 0.5 and 5.00 VDC, dependent on the frequency of operation. An unlocked condition (indicated on pin 11 of J201) is less than 1.5 VDC. The synthesizer determines the lock state of the radio by comparing the scaled VCO frequency to the scaled reference oscillator TCXO of 14.4 MHz.

The VCO is a Colpitts oscillator formed by Q962 along with several capacitors, varactor diodes, and a ceramic resonator. The DC bias to the VCO is provided by transistor Q901 and forms a capacitance multiplier which delivers filtered, noise free supply voltage to the oscillator circuitry. The VCO is followed by gain stages which amplify the signal to approximately 0 dBm and then divide the signal using a splitter and sending it to the receiver or transmitter.

The VCO is capable of oscillating between 403-434 MHz or 450-480 MHz in transmit and 489.85-520.85 MHz or 536.85-566.85 MHz in receive. The course frequency shift in the VCO between receive and transmit is accomplished by shifting in a capacitor to the tank of the oscillator. Pin 7 of J201 (receive enable) performs this function. When transmitting, the receive enable is forced low and a pin diode is turned on by a digital transistor connected to pin 7 which switches capacitance into the oscillator circuit. The reverse happens when returning to receive mode. Refer to section 3 for receive to transmit and transmit to receive load sequences.

There are two parts to the transceiver modulation circuitry. With the placement of the VCO control line voltage low pass filter at approximately 400 Hz, it is necessary to modulate both the VCO and the TCXO. A loop response of 400 Hz is necessary to accomplish the fast lock times of the 3473. If only the VCO were modulated to transmit data, any baseband frequency component below 400 Hz would not be modulated onto the transmit carrier. To accomplish this the transceiver was designed to modulate both the VCO and TCXO, thus creating two parts to the modulation circuit and modulation capability from below 50 Hz up to 5000 Hz.

It is important to note that modulation sensitivity adjustment and modulation deviation limiting are to be supplied in the customer interface equipment, and are required by most regulatory agencies, such as the Federal Communications Commission (FCC) in the United States.

The modulation flatness adjustment (R825) balances the sensitivity of the VCO vs. the TCXO. The radio is set to best modulation flatness in the center of the RF band (418.5 MHz or 465 MHz) when the unit leaves the Dataradio factory. The modulation flatness becomes uneven when nearing the band edges due to changing sensitivity of the TCXO and VCO across a wide range of RF frequencies.

If optimal modulation flatness is desired across the whole RF band of 450-480 or 403-434 MHz, the unit is equipped with an external flatness adjust. Pin 9 of J201 allows the implementation of an analog voltage between 0 and 5 VDC to obtain flat modulation. Linear interpolation of this voltage between the RF band edges will insure flat modulation everywhere in the band. If flat modulation is desired only in a single or small range of grouped frequencies, R825 of the 3473 module can be tuned for flat modulation and pin 9 of the user connector left open.

The frequency stability of the VCO in receive and transmit mode is established by the stability of the reference oscillator. The reference oscillator for the 3473 is 14.4 MHz and is designed to be stable between $\pm$ 1.5 PPM over the entire operating temperature range of -30° to +60° C. Pin 10 of the user interface connector is the modulation input to the VCO and TCXO as described above, however this pin also serves another purpose. A precision 2.5 VDC reference is essential for the TCXO to compensate $\pm$ 1.5 ppm for changes in ambient temperature. Pin 10, in addition to modulating the data, requires a DC component of 2.5 VDC $\pm$ 0.05 VDC.

Channels are selected by programming counters in U811. Section 3 of this manual shows how to program the Phillips SA7025A Frequency Synthesizer for the DM-3473. This programming is performed over a 3-wire serial bus formed by pins 14, 15, and 16 of user interface J201. These pins are labeled Synth Enable, Synth Data, and Synth Clock. This programming is supplied by customer hardware and software interface equipment. A block diagram of the synthesizer/VCO is shown in Figure 4-1 along with a block diagram of the Phillips synthesizer IC SA7025A in Figure 4-2.

4.4 RF POWER AMPLIFIER CIRCUIT DESCRIPTION

The 3473 transmitter produces a nominal RF power output of 2 Watts (+33 dBm) at a supply voltage on pins 3 and 4 of 7.2 VDC. Frequency modulation (FM) of the transmit data input stream occurs in the VCO (see previous section).

The transmitter line-up on the 3473 is a class C conduction type amplifier. A class C amplifier requires that the RF voltage being applied to the amplification device is sufficient as to cause the transistor to "turn-on". This type of design was incorporated to improve efficiency over a class A type amplifier.

There are two major sections to the power amplifier in the 3473. A driver integrated circuit is the first device in the amplification line-up. The VCO is applied through a splitter and matching network to this device for intermediate amplification to +26 dBm (400 mW). The input voltage for this device is approximately 2.7 VDC. This low dropout regulated supply is produced by a dual op amp and a high current series pass PNP transistor Q611.

The power delivered from the driver stage is matched into a high power MOSFET transistor Q541. This device has about 8 dB of gain and amplifies the signal to +34.5 dBm. The RF voltage created from the driver stage is sufficient to turn on the MOSFET. The final is biased on to a quiescent current of Idss=200 mA which is set by R521. C552 is adjusted for balanced output power across the RF band. Present on the output of the final transistor is a low-pass transmitter harmonic filter. To insure the 3473 meets stringent regulatory guidelines a 5 pole filter rejects the harmonics created in the power amplifier.

Three PIN diodes and several matching components are used to implement the antenna switch. In transmit mode, the diodes are all forward biased. A finely tuned coil and capacitor create a quarter wave open which reflects the transmitter power and protects the receiver front end from the transmitter. In receive mode the diodes are off thus creating a 50 ohm impedance path to the front end of the 3473 receiver. Due to passive device losses in the low pass filter and the antenna switch, the output power is reduced to 2 watts. The transmit signal is then fed to the female MCX antenna connector J501.

The 3473 implements a logic level at the user interface connector to enable the transmitter. By applying a logic high to pin 6 the transmitter will enable, assuming the synthesizer and VCO are locked and ready to transmit. Refer to section 3 for the exact receive to transmit load sequence. When the logic level is applied the RF is brought up relatively slow so that spectral spreading of the transmitter does not occur. An RC time constant 'ramps' up the RF power to the final which takes no longer than 2 ms. The ramping is incorporated so that the power of the transmitter does not splatter into channels adjacent to the frequency of operation.

4.5 RECEIVER CIRCUIT DESCRIPTION

The receiver on the 3473 is a FM dual down conversion superheterodyne topology. Dual down conversion means that the receiver has two intermediate frequencies (IF) of 86.85 MHz and 450 kHz. The first local oscillator (LO) is high side injected 86.85 MHz above the desired receive frequency. This is the function of the VCO in receive mode. The design also incorporates two discrete bandpass filters to reject image and other wideband frequencies. A surface acoustic wave (SAW) filter is implemented in the first IF to enhance receiver selectivity. 10 poles of filtering are used in the second IF to further improve selectivity and to set the IF bandwidth of either 12.5 kHz or 25 kHz. Figure 4-1 shows the receiver block diagram for the 3473 radio module.

From the antenna connector the signal is fed to a two pole bandpass filter. This filter sets the initial RF bandwidth of approximately 30 MHz for the receiver. A low noise amplifier (LNA) is matched from the bandpass filter. The LNA transistor Q210 produces about 14 dB of gain and sets the overall sensitivity of the radio. The LNA is followed by a three pole bandpass filter to help reject unwanted out of band RF signals. Both bandpass filters are discrete filter designs comprising of several air wound inductor coils and many surface mount capacitors.

The front end of the receiver is finely tuned into the mixer of the receiver. The mixer is an active design using a dual gate gallium arsenide MESFET labeled Q240. One gate of the FET is fed the RF signal from the front end network, and the other gate is fed the first LO injection from the VCO. To buffer the VCO from the receiver a transistor (Q302) with unity gain is in between the mixer and the VCO. The mixer, for example, converts the RF signal of 450 MHz and the first LO signal of 536.85 MHz to the first IF frequency 86.85 MHz.

From the mixer, the receive signal is delivered to a SAW filter which has a bandwidth of 40 kHz and provides the first narrow band filtering in the receiver. SAW filter technology features low group delay performance for data applications, low distortion at high RF input levels, and fixed tuning. The output of the SAW filter travels to a Phillips SA676 IF IC for down conversion to the second IF frequency, FM limiting, and demodulation to baseband of the data signal. The block diagram of U261 is shown in Figure 4-3.

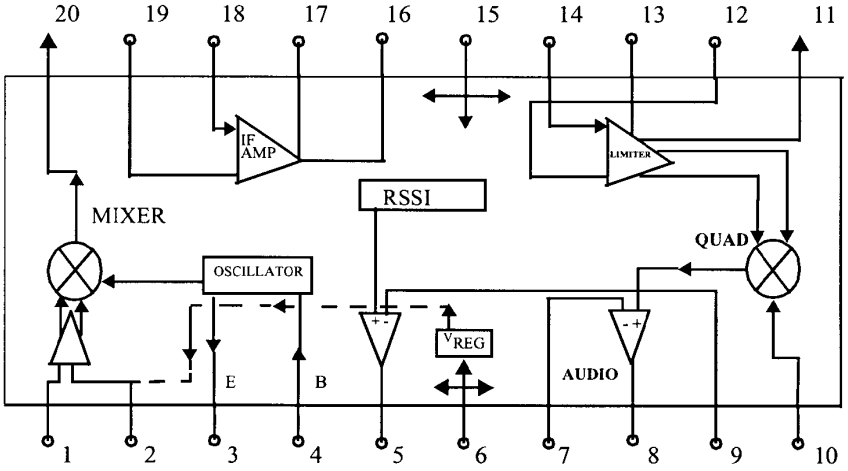

Figure 4-3 U261 BLOCK DIAGRAM

The first IF is input to a mixer for conversion down to the second IF frequency of 450 kHz. The second LO of 86.4 MHz (low side injection) is derived from amplifying and filtering of the TCXO sixth harmonic. Q280 amplifies the TCXO signal and various inductors and capacitors filter the desired frequency component for injection to the IF IC. The 86.85 MHz first IF mixes with the second LO of 86.4 MHz to create the second IF at 450 kHz. A four pole and six pole ceramic bandpass filter set overall channel bandwidth of the radio to either 12.5 kHz or 25 kHz. The channel bandwidth is ordered as such from the part number scheme in Section 1.

Once the second IF is filtered, the signal is then amplified by 100 dB of gain in the Phillips IF chip. A quadrature discriminator demodulates the data signal and is then fed to an operational amplifier also internal to the IC. A quadrature detector has the ability to give true DC coupled data output to pin 12 of the user interface connector. The Phillips IC also has a receive signal strength indicator (RSSI) built in. This output on pin 13 of the interface connector gives a DC voltage which is logarithmically related to the strength of the receive signal. The dynamic range of the RSSI indicator is at least 70 dB. This output can be used by the customer to implement a data carrier detect (DCD) circuit on the interface board to the 3473.

SECTION 8

COMPONENT LAYOUTS

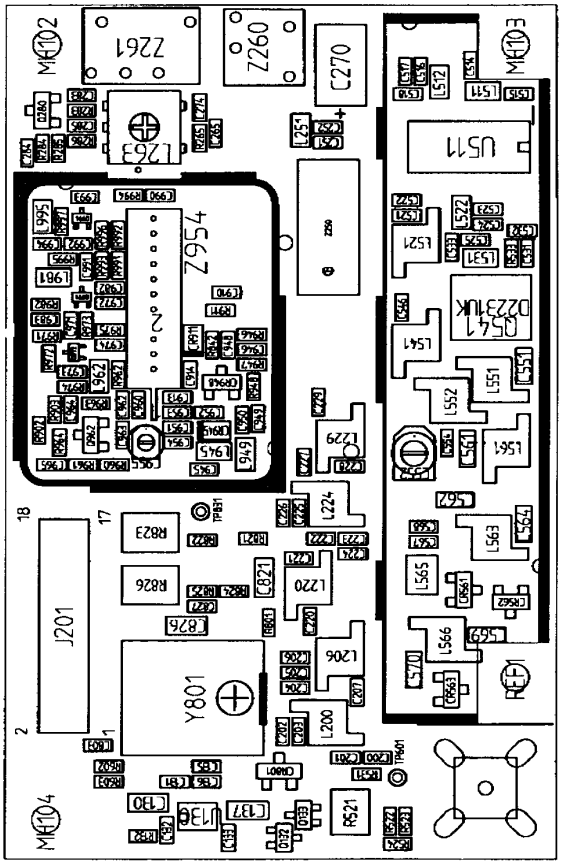

FIGURE 8-1 3473 COMPONENT LAYOUT (TOP SIDE)

SECTION 6

ALIGNMENT PROCEDURE AND PERFORMANCE TESTS

6.1 GENERAL

Receiver or transmitter alignment may be necessary if repairs are made that could affect tuning. Alignment points diagrams are located in Figure 6-3 or component layouts are located in Section 8.

Fabricate test cables by referring to Section 2.2 Interfacing with Data Equipment. This cable should include power and ground, a transmit keying switch that applies 5.5 VDC to the Rx and Tx Enable, data input and data output. The test setup must apply the various supply voltages and load the synthesizer with channel information.

6.2 ALIGNMENT PROCEDURE

6.2.1 VCTCXO SETUP (Y801)

1. Apply 7.2 Vdc +\-0.1 Vdc to pins 3, 4, and 5.

2. Verify 2.5 Vdc +\- 0.05 Vdc is on pin 10.

3. Set Y801 (the VCTCXO) to 14.400000 MHz +\- 6.0 Hz (+\- 0.4PPM)

6.2.2 FREQUENCY AND CONTROL LINE VOLTAGE CHECK

1. Connect the test setup shown in Figure 6-1. Set the power supply for +7.2V DC.

2. Load the synthesizer with the channel frequency.

3. Connect a DC voltmeter at TP831 to measure the VCO control line voltage for a meter reading of ≥ 0.50 - ≤ 5.0VDC for all desired frequencies of operation in both transmit and receive.

6.2.3 2W TRANSMITTER POWER ALIGNMENT

1. Connect the test setup shown in Figure 6-1. A DC ammeter capable of measuring up to 2.0 A should be installed in the supply line.

2. Load the synthesizer with the desired channel frequency.

3. Set the IDSS of the final by shorting TP601. To Ground R521, turn counter-clockwise for minimum transmit current. Note the current and adjust R521 for 200 mA more current.

4. Key the transmitter and make sure that pins 3, 4, and 5 on the RF board are 7.2V.
   (Do not transmit for extended periods.)

5. Adjust C552 for 2 watts output power.

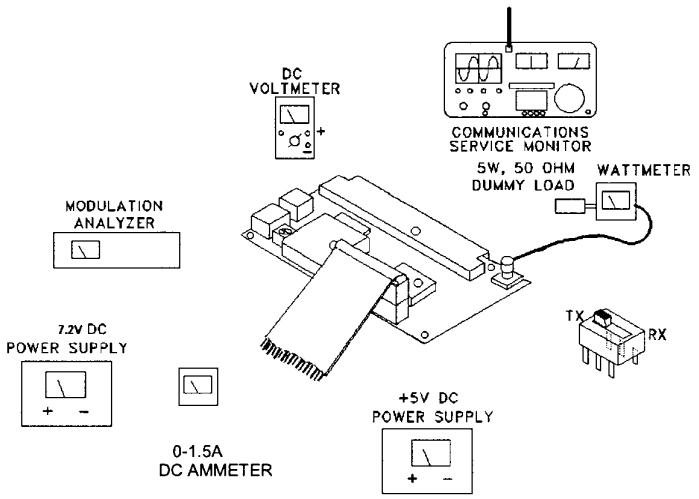

Figure 6-1 TRANSMITTER TEST SETUP

6.2.4 MODULATION FLATNESS ALIGNMENT

1. Transmit into the modulation analyzer at the desired frequency and observe modulation output on the oscilloscope. Set the modulation analyzer high pass filtering off and no less than a 15 kHz low pass filter.

2. Inject a 100 Hz sine-wave on J201, pin 10, biased at 2.5V DC, at the level below according to the bandwidth:

   200 m Vrms for 12.5 kHz BW (-210 Radios)
   400 m Vrms for 25.0 kHz BW (-230 Radios)
   180 m Vrms for 12.5 kHz BW (-510 Radios)
   360 m Vrms for 25.0 kHz BW (-530 Radios)

3. Switch on TX Modulation. Set the modulation analyzer for 15 kHz low pass filtering.

4. Note the transmit deviation _____kHz. The deviation should be between:

   ± 1.2/± 1.8 kHz for 12.5 kHz BW (-X10 Radios)
   ± 2.4/± 3.6 kHz for 25.0 kHz BW (-X30 Radios)

5. Input a 1.0 kHz sine-wave at the same voltage. The transmit deviation should be the same as that noted in Step 4. If not, adjust R826 until the deviation level matches that of Step 4.

6. Remove transmit modulation and unkey the transmitter.

Note: The modulation flatness can also be set flat by adjusting the voltage on pin 9 of J201 between 0-5 VDC.

6.2.5 FRACTIONAL CHANNEL SPUR ADJUSTMENT

1. Refer to Section 3.4.4 for the default CN values for the appropriate band radio (-2Y0 or -5Y0) to load into the synthesizer.

2. To determine if your desired frequency is a fractional channel, divide the frequency by 6.25 kHz. The number will be a whole integer. Divide the channel frequency by 12.5 kHz. If the number is not a whole integer, the frequency is a fraction channel frequency.

3. To optimize the performance of the receiver on a fractional channel, input an unmodulated (desired) frequency. Monitor the output of J201, pin 12 with an oscilloscope. Adjust R823 for a minimum level of 6.25 kHz recovered audio.

4. To optimize the performance of the transmitter on a fractional channel, monitor the de-modulated transmit signal of a modulation analyzer and adjust R823 for minimum level of 6.25 kHz recovered audio.

5. Receive and transmit performance can be further optimized by adjusting the CN value up or down for minimum recovered 6.25 kHz audio signal.

6.2.6 RECEIVER ALIGNMENT

C A U T I O N: ***Do not key the transmitter with the generator connected! Severe generator damage may result.***

1. Connect the test setup shown in Figure 6-2. Adjust the power supply for +7.2V DC.

2. Measure the receive current drain. (current should be <60 mA.)

3. Load the synthesizer with the channel frequency.

4. Set the RF signal generator for this frequency with a 1 kHz tone (modulated output shown below) at a level of -47 dBm (1000 μV) and inject into J501.

1.5 kHz deviation (-X10 12.5 kHz BW Radio)
3.0 kHz deviation (-X30 25.0 kHz BW Radio)

NOTE: Maintain these deviation levels throughout the test when measuring AC levels, SINAD and % distortion.

5. Adjust L263 for maximum Vrms at the receive audio output.

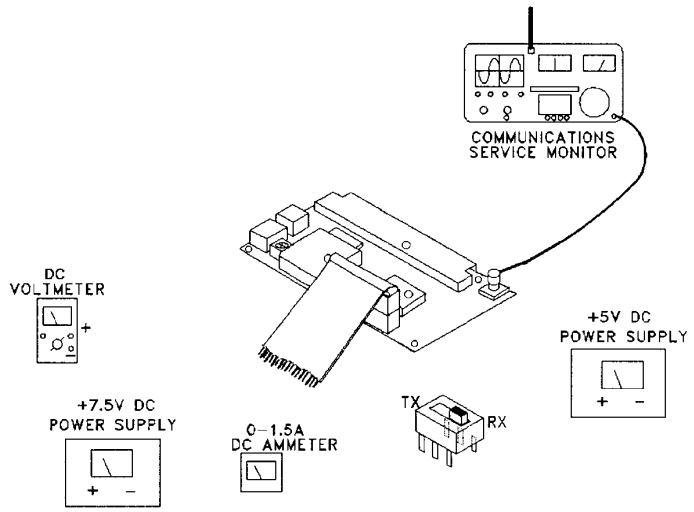

Figure 6-2 RECEIVER TEST SETUP

6 Record the RMS audio voltage level _____RMS. (Typically 150 mV ±50 mV.) Record the DC Bias level of the audio out _____Vdc. (Typically 2.5 Vdc ± 0.5 Vdc)

7. Record the percent distortion _____%. (Typically <3%.)(psophometrically weighted)

8. Adjust the RF input level until 12 dB SINAD is measured. (Typically < -116 dBm).

9. Adjust the generator RF level to -120 dBm and measure DC (RSSI) voltage on J201, pin 12 ___Vdc at -120 dBm.

10. Adjust the generator RF level to -60 dBm and measure DC (RSSI) voltage on J201, pin 12 ___Vdc at -60 dBm.

11. The RSSI voltage at -60 dBm minus the (RSSI) voltage -120 dBm should be >0.7 VDC and the RSSI voltage at -120 dBm ≤ 1.1 Vdc.

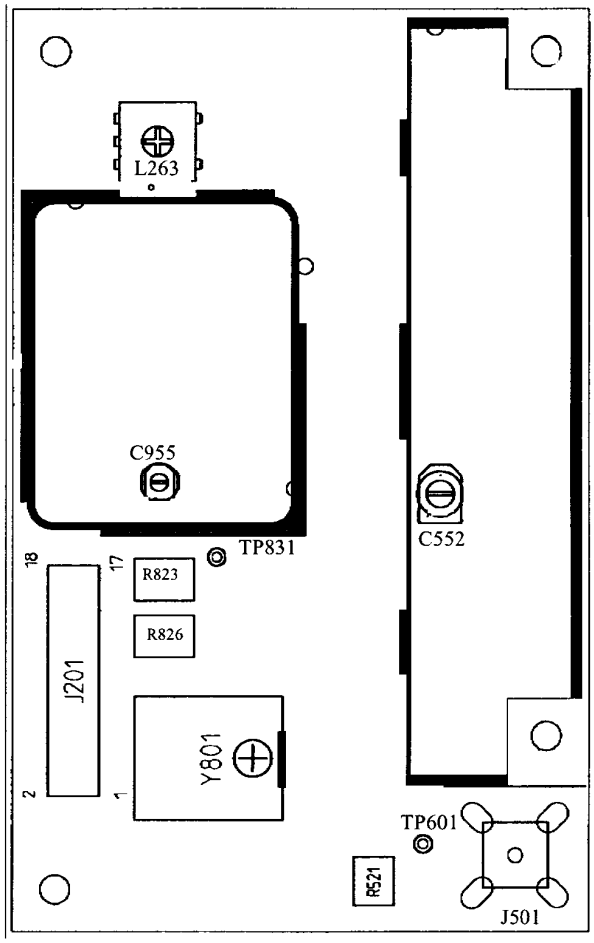

Figure 6-3 ALIGNMENT POINTS DIAGRAM

SECTION 2

INSTALLATION

2.1 PRE-INSTALLATION CHECKS

Field alignment should not be required before the 3473 is installed. However, it is a good practice to check the performance to ensure that no damage occurred during shipment. Performance tests are located in Section 6.

2.2 INTERFACING WITH DATA EQUIPMENT

2.2.1 The DM-3473 User Interface (J201) is a Samtec 18-pin dual-row connector socket with a 2 mm pitch, vertical mount. It is made of a black liquid crystal polymer. The contact material is phosphor bronze. The current capacity per pin is 1 Amp maximum at 80° C. The insertion depth is .084 to .170 inches with .015 inch wipe. For pin orientation, see Section 8.

2.2.2 CONNECTOR PIN ASSIGNMENTS

Table 2-1 PIN ASSIGNMENTS

PIN	ASSIGNMENT	DESCRIPTION
1	**Ground**	
2	**Ground**	
3	**7.2 VDC Switched Battery**	
4	**7.2 VDC Switched Battery**	Pins 3 & 4 are identical and must be doubled up on customer supplied interface for supply current restrictions. Voltage supply is 6-9 VDC with 7.2VDC nominal for 2 Watt output power. Maximum current is 1.5 Amps or 750 mA per pin.
5	**7.2 VDC Regulated**	This pin must always be regulated between 6-9 VDC for onboard regulation. If 2 Watts is the desired output power, then pins 3,4, & 5 can be tied together on a customer supplied interface board and regulated to 7.2 VDC. Maximum current is 750 mA.
6	**Tx_Enable**	Transmit enable pin. This is a logic level to enable the transmitter and is logic high (4.5 - 13VDC)
7	**Rx_ Enable**	Receive enable pin. This is a logic level to enable the receiver and is logic high (4.5 - 13VDC). This pin also performs the VCO Tx to Rx course frequency shift.

Table 2-1 PIN ASSIGNMENTS

PIN	ASSIGNMENT	DESCRIPTION
8	**Sleep Mode**	This pin puts the transceiver into a sleep mode drawing <1mA. This pin is a logic level to enable/disable the transceiver. Enable high is 2.0V to pin 5 voltage. Disable low or sleep mode is <.60 VDC. Note: The synthesizer channel load information must be re-loaded when coming out of sleep mode.
9	**Tx_MOD_ADJ**	This pin can be used to adjust the modulation balance of the transmitter across the RF band (403-434 MHz or 450-480 MHz). A voltage is applied to the pin from 0-5VDC at the desired RF frequency of operation and is tied directly to a VCO varactor to tune the modulation flatness. Internally, the transceiver is tuned flat for the center of the RF band (418.5 MHz and 465 MHz) with this pin open. *The use of an op-amp is recommended to interface to this pin or a source with the resistance ≤ 1 k ohms.*
10	**Tx_MOD_IN**	Transmit modulation input. This pin must have a DC coupled, regulated 2.5 ± 0.05 VDC supply to bias the TCXO in transmit and receive and also be temperature compensated. This pin is tied directly to the VCO for modulating the radio in transmit mode. *See Section 1: General Specifications for modulation capability.*
11	**Lock Detect**	The synthesizer lock detect pin indication: ≥4VDC = lock ≤1.5 VDC = unlock
12	**Rx_DATA_OUT**	This output is the DC coupled wideband output of the receiver baseband detected data. The nominal output is 2.5VDC bias with 150mVrms audio out with 60% rated deviation and a 1 kHz tone. *NOTE: The nature of the receiver will output inverted audio.*
13	**RSSI Output**	Receiver Signal Strength Indicator. The receiver's detector outputs a DC voltage logarithmically related to the strength of the received signal. With -60 to -120 dBm at the RF input the voltage will be V (high) - V (low) ≥0.7 VDC and V (low) ≤ 1.1 Vdc. This output can be used to implement a data detect circuit (DCD) on the customer supplied interface board.
14	**SYNTH_ENABLE**	This is part of the 3 pin serial interface to load the synthesizer. See Section 3 to implement pins 14, 15, & 16.
15	**SYN_DATA**	3 pin serial interface which carries the raw data of A, B, and D Words to the synthesizer following the Phillips SA7025 loading protocol. (The C-Word is not necessary on the DM-3473.) See Section 3.
16	**SYN_CLOCK**	3 pin serial interface pin which requires the synthesizer clock. The synthesizer maximum clock frequency is 1 MHz. See Section 3.
17	**NO CONNECT**	
18	**NO CONNECT**	