DESCRIPTION OF CIRCUIT

The Wireless LAN Card is comprised of 5 parts:
• 2.4GHz Power Amplifier and Detector
• HFA3683 2.4GHz RF/IF Converter and Synthesizer
• HFA3783 AGC Quadrature Modem and Synthesizer
• HFA3861 Baseband Processor with Rake Receiver
• HFA3841 Media Access Controller

The IF is a linear design with AGC. This permits the use of equalizers in the BBP. An IF overload detector and a selectable low gain LNA mode work with the BBP to extend dynamic range without sacrificing sensitivity.
The PA incorporates an integral power detector that is monitored by the BBP to control the IF gain to maintain constant output levels.
The baseband processor uses CCK modulation and a Rake architecture to reduce the effects of multipath distortion. This reduces the error rates in typical office environments to improve overall data throughput. An optional fast acquisition mode further improves throughput.
The MAC utilizes a processor optimized for control of the WLAN protocol. It supports the 11Mbps data rate with low power consumption.

• Compliant to IEEE 802.11 DSSS Standard at 1 and 2 MBPS
• Compliant to DRAFT IEEE 802.11 Extension at 5.5MBPS and 11MBPS
• Power Consumption Reduced By Nearly 50%
• Rake Architecture for Improved Multipath Performance
• AGC IF for Linear Operation
• IF Overload Detector
• Low Gain Mode in the LNA for High Level Inputs
• Gain Control Loop for RF and IF Integrated into BBP
• All Parts Operate at 3VDC
• DC Coupling at the Baseband Interface
• Low Noise Figure (1.8dB)
• PA Includes Integral Detector
• Transmit Level Control Provided
• Integral Digital Filtering for Baseband Output
• Differential Interfaces at IF and Baseband for Noise Immunity
• Short Preamble Mode for Higher Throughput
• Single IF Filter for Transmit and Receive

2.4GHz Power Amplifier and Detector

The HFA3983 is a 2.4GHz monolithic SiGe Power Amplifier designed to operate in the ISM Band. It features two low voltage single supply stages. Cascaded, they deliver a 18dBm (Typ) of an output power for the typical DSSS signal (ACPR, 1st

Side Lobe < -30dBc, 2nd Side Lobe < -50dBc). In addition, the device includes a 2.4GHz detector which is accurate over a 15dB of dynamic range with ± 1dB. Therefore, an accurate ALC function can be implemented.

HFA3683 2.4GHz RF/IF Converter and Synthesizer

The HFA3683A is a monolithic SiGe half duplex RF/IF transceiver designed to operate in the 2.4GHz ISM band. The receive chain features a low noise, gain selectable amplifier (LNA) followed by a down-converter mixer. An up-converter mixer and a high performance preamplifier compose the transmit chain.
The remaining circuitry comprises a high frequency Phase Locked Loop (PLL) synthesizer with a three wire programmable interface for local oscillator applications. A reduced filter count is realized by multiplexing the receive and transmit IF paths and by sharing a common differential matching network. Furthermore, both transmit and receive RF amplifiers can be directly connected to mixers as image reject filters are integrated.

HFA3783 AGC Quadrature Modulator/Demodulator and Synthesizer

The HFA3783 is a highly integrated and fully differential SiGe baseband converter for half duplex wireless applications. It features all the necessary blocks for quadrature modulation and demodulation of "I" and "Q" baseband signals. It has an integrated AGC receive IF amplifier. The AGC has 70dB of voltage gain and better than 70dB of gain control range. The transmit output also features gain control with 70dB of range. The receive and transmit IF paths can share a common differential matching network to reduce the filter component count required for single IF half duplex transceivers. A pair of 2nd order antialiasing filters with an integrated DC offset cancellation architecture is included in the receive chain for baseband operation down to DC. In addition, an IF level detector is included in the AGC chain for threshold comparison. Up and down conversion are performed by doubly balanced mixers for "I" and "Q" IF processing. These converters are driven by a broadband quadrature LO generator with frequency of operation phase locked by an internal 3 wire interface synthesizer and PLL. The device requires low LO levels from an external VCO and a PLL reference signal up to 44MHz.

HFA3861 Baseband Processor with Rake Receiver

The HFA3861B Direct Sequence Spread Spectrum (DSSS) baseband processor has on-board A/D's and D/A for analog I and Q inputs and outputs, for which the HFA3783 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with Complementary Code Keying to provide a variety of data rates. Built-in flexibility allows the HFA3861B to be configured through a general purpose control bus, for a range of applications. Both Receive and Transmit AGC functions

with 7-bit AGC control obtain maximum performance in the analog portions of the transceiver.

1) Transmitter Description

The HFA3861B transmitter is designed as a Direct Sequence Spread Spectrum Phase Shift Keying (DSSS PSK) modulator. It can handle data rates of up to 11Mbps (refer to AC and DC specifications). The various modes of the modulator are Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps. The major functional blocks of the transmitter include a network processor interface, DPSK modulator, high rate modulator, a data scrambler and a spreader. CCK is essentially a quadra-phase form of M-ARY Orthogonal Keying. The preamble is always transmitted as the DBPSK waveform while the header can be configured to be either DBPSK, or DQPSK, and data packets can be configured for DBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or CCK switchover, as required. For the 1 and 2Mbps modes, the transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and spreads it with the BPSK PN sequence. The baseband digital signals are then output to the external IF modulator. For the CCK modes, the transmitter inputs the data and partitions it into nibbles (4 bits) or bytes (8 bits). At 5.5Mbps, it uses two of those bits to select one of 4 complex spread sequences from a table of CCK sequences and then QPSK modulates that symbol with the remaining 2 bits. Thus, there are 4 possible spread sequences to send at four possible carrier phases, but only one is sent. This sequence is then modulated on the I and Q outputs. The initial phase reference for the data portion of the packet is the phase of the last bit of the header. At 11Mbps, one byte is used as above where 6 bits are used to select one of 64 spread sequences for a symbol and the other 2 are used to QPSK modulate that symbol. Thus, the total possible number of combinations of sequence and carrier phases is 256. Of these only one is sent.

2) Header/Packet Description

The HFA3861B is designed to handle packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3861B generates its own preamble and header information. It uses two packet preamble and header configurations. The first is backwards compatible with the existing IEEE 802.11-1997 1 and 2Mbps modes and the second is the optional shortened mode which maximizes throughput at the expense of compatibility with legacy equipment. In the long preamble mode, the device uses a synchronization preamble of 128 symbols along with a header that includes four fields. The preamble is all 1's (before entering the scrambler) plus a start frame delimiter (SFD). The actual transmitted pattern of the preamble is randomized by the scrambler. The preamble is always transmitted as a DBPSK waveform (1Mbps). The duration of the long preamble and header is 192us. In the

short preamble mode, the modem uses a synchronization field of 56 zero symbols along with an SFD transmitted at 1Mbps. The short header is transmitted at 2Mbps. The synchronization preamble is all 0's to distinguish it from the long header mode and the short preamble SFD is the time reverse of the long preamble SFD. The duration of the short preamble and header is 96us.

Start Frame Delimiter (SFD) Field (16 Bits) - This field is used to establish the link frame timing. The HFA3861B will not declare a valid data packet, even if it PN acquires, unless it detects the SFD. The HFA3861B receiver is programmed to time out searching for the SFD via CR 10 BITS 4 and 5. The timer starts counting the moment that initial PN synchronization has been established on the preamble.

Signal Field (8 Bits) - This field indicates what data rate the data packet that follows the header will be. The HFA3861B receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK, or CCK demodulation at the end of the preamble and header fields.

Service Field (8 Bits) - The MSB of this field is used to indicate the correct length when the length field value is ambiguous at 11Mbps. See IEEE STD 802.11 for definition of the other bits. Bit 2 is used by the HFA3861B. To indicate that the carrier reference and the bit timing references are derived from the same oscillator.

Length Field (16 Bits) - This field indicates the number of microseconds it will take to transmit the payload data (PSDU). The external controller (MAC) will check the length field in determining when it needs to de-assert RX_PE.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the three header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The HFA3861B receiver will indicate a CCITT - CRC 16 error via CR24 bit 2 and will lower MD_RDY and reset the receiver to the acquisition mode if there is an error. The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (frame check sequence). It is the ones compliment of the remainder generated by the modulo 2 division of the protected bits by the polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

The protected bits are processed in transmit order. All CRC calculations are made ahead of data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complemented and the residual shifted out MSB first. The following Configuration Registers (CR) are used to program the preamble/header functions.

CR 4 - Defines the preamble length minus the SFD in symbols. The 802.11 protocol requires a setting of 128d = 80h for the mandatory long preamble and 56d = 38h for the optional short preamble.

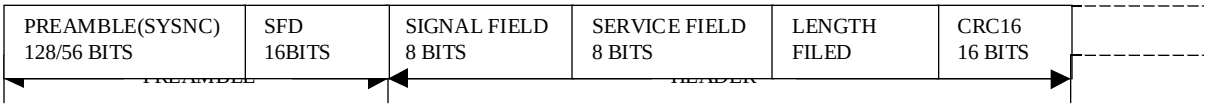
CR 10 Bits 4, 5 - Define the length of time that the demodulator searches for the SFD before returning to acquisition.

CR 5 Bits 0, 1 - These bits of the register set the Signal field to indicate what modulation is to be used for the data portion of the packet.

CR 6 - The value to be used in the Service field.

CR 7 and 8 - Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol and is in microseconds required to transmit the data at the chosen data rate. The packet consists of the preamble, header and

MAC protocol data unit (MPDU). The data is transmitted exactly as received from the control processor. Some dummy bits will be appended to the end of the packet to insure an orderly shutdown of the transmitter. This prevents spectrum splatter. At the end of a packet, the external controller is expected to de-assert the TX_PE line to shut the transmitter down. Set the scrambler CR36E37 seed valve for the transmitter.



3)Demodulator Description

The receiver portion of the baseband processor, performs A/D conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, or CCK symbols. The demodulator includes a frequency tracking loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes (where appropriate) and descrambles the data. The data is output through the RX Port to the external processor. The baseband processor, HFA3861B uses differential demodulation for the initial acquisition portion of the message processing and then switches to coherent demodulation for the MPDU demodulation. The HFA3861B is designed to achieve rapid settling of the carrier tracking loop during acquisition. Rapid phase fluctuations are handled with a relatively wide loop bandwidth which is then stepped down as the packet progresses. Coherent processing improves the BER performance margin as opposed to differentially coherent processing for the CCK data rates.

The baseband processor uses time invariant correlation to strip the PN spreading and phase processing to demodulate the resulting signals in the header and DBPSK/DQPSK demodulation modes. In processing the DBPSK header, input samples from the I and Q A/D converters are correlated to remove the spreading sequence. The peak position of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to maintain phase lock. The carrier is de-rotated by the carrier tracking loop. The demodulated data is differentially decoded and descrambled before being sent to the header detection section. In the 1Mbps DBPSK mode, data demodulation is performed the same as in header processing. In the 2Mbps DQPSK mode, the demodulator demodulates two bits per symbol and differentially decodes these bit pairs. The bits are then
serialized and descrambled prior to being sent to the output. In the CCK modes, the receiver removes carrier frequency offsets and uses a bank of correlators to detect the modulation. A biggest picker finds the largest correlation in the I and Q Channels and determines the sign of those correlations. For this to happen, the demodulator must know the starting phase which is determined by referencing the data to the last bit of the header. Each symbol demodulated determines 1 or 2 nibbles of data. This is then serialized and descrambled before being passed to the

output. Chip tracking in the CCK modes is chip decision directed. Carrier tracking is via a lead/lag filter using a digital Costas phase detector.

HFA3841 Media Access Controller

The HFA3841 Wireless LAN Medium Access Controller directly interfaces with the HFA3861B Baseband Processors. Protocol and PHY support are implemented in firmware to allow custom protocol and different PHY transceivers. The HFA3841 is designed to provide maximum performance with minimum power consumption. External pin layout is organized to provide optimal PC board layout to all user interfaces.

Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgement, fragmentation and de-fragmentation, and automatic beacon monitoring are handed without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers.