REXENSE

802.15.4/ ZigBee Module Datasheet

REX3

ZHEJIANG REXENSE TECHNOLOGY CO., LTD.

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VERSION HISTORY

V1.0.0	2011/06/4	1st issue of preliminary document
V1.0.1	2012/05/22	Add the section of *Agency Certifications*

Table of Contents

1. Introduction

1.1 Summary

REX3 is an ultra-compact, low-power, high-sensitivity 2.4 GHz IEEE 802.15.4/ ZigBee Module based on the innovative Rexense's hardware platform. It is designed for wireless sensing, control and data acquisition applications. Rexense 802.15.4/ ZigBee Modules eliminate the need for costly and time-consuming RF development, and shorten time to market for a wide range of wireless applications.

1.2 Applications

Rexense 802.15.4/ ZigBee Module is compatible with robust IEEE 802.15.4/ ZigBee stack that supports a self-healing, self-organizing mesh network, while optimizing network traffic and minimizing power consumption. Rexense offers two stack configurations: Custom and Transparent (currently supports STM32W RexBee module only). Custom software can be provided to support reliable, scalable, and secure wireless applications running on Rexense 802.15.4/ ZigBee Modules. Transparent software allows programming of the module via serial AT-command interface.

The applications include, but are not limited to:

- Building automation & monitoring
  - Lighting controls
  - Wireless smoke and CO detectors
  - Structural integrity monitoring
- HVAC monitoring & control
- Inventory management
- Environmental monitoring
- Security
- Water metering
- Industrial monitoring
  - Machinery condition and performance monitoring
  - Monitoring of plant system parameters such as temperature, pressure, flow, tank level, humidity, vibration, etc.
- Automated meter reading (AMR)

1.3 Key Features

- Ultra compact size (31.60*20.70*3.90mm for REX3 module)
- High RX sensitivity (-99 dBm)
- Outperforming link budget (105dB)
- Wide Communication Distance: up to 400m (Line of Sight)
- Up to 7dBm output power
- Very low power consumption:
  - 0.4μA in Sleep mode
  - 27mA in RX mode
  - 36mA in TX mode
- Ample memory resources
  - STM32W: 128K bytes Flash; 8K bytes RAM
  - EM351/EM357: 128K/192K bytes Flash; 12K bytes RAM
- Wide range of interfaces (both analog and digital):
  - 24 spare GPIO, 4 spare IRQ lines
  - 6 ADC lines
  - UART with CTS/RTS control
  - USART
  - TWI
  - SPI
  - Capability to write own MAC address into the Flash
  - Optional antenna reference designs
  - IEEE 802.15.4 compliant transceiver
  - 2.4 GHz ISM band
  - Custom embedded software, including serial bootloader and AT command set

1.4 Benefits

- Small physical footprint and low profile for optimum fit in even the smallest of devices
- Best-in-class RF link range
- Extended battery life
- Easy prototyping with 4-layer PCB
- Ample memory for user software application
- Mesh networking capability
- Easy-to-use low cost Evaluation Kit
- Single source of support for HW and SW
- Worldwide license-free operation

1.5 Abbreviations and Acronyms

ADC	Analog-to-Digital Converter
API	Application Programming Interface
DC	Direct Current
DTR	Data Terminal Ready
DIP	Duap In-line package
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HAL	Hardware Abstraction Layer
HVAC	Heating, Ventilating and Air Conditioning
HW	Hardware
TWI	Inter-Integrated Circuit
IEEE	Institute of Electrical and Electrionics Engineers
IRQ	Interrupt Request
ISM	Industrial, Scientific and Medical radio band
JTAG	Digital interface for debugging of embedded device, also known as IEEE 1149.1 standard interface
MAC	Medium Access Control layer
MCU	Microcontroller Unit. In this document it also means the processor, which is the core of 802.15.4/ ZigBee Module
NWK	Network layer
OEM	Original Equipment Manufacturer
OTA	Over-The-Air upgrade
PCB	Printed Circuit Board
PER	Package Error Ratio
PHY	Physical layer
RAM	Random Access Memory
RF	Radio Frequency
RTS/CTS	Request to Send/ Clear to Send
RX	Receiver
SMA	Surface Mount Assembly
SPI	Serial Peripheral Interface
SW	Software
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
ZDK	ZigBee Development Kit
ZigBeePRO	Wireless networking standards targeted at low-power applications
802.15.4	The IEEE 802.15.4-2003 standard applicable to low-rate wireless PAN

1.6 Related Documents

[1] IEEE Std 802.15.4-2003 IEEE Standard for Information technology - Part 15.4 Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

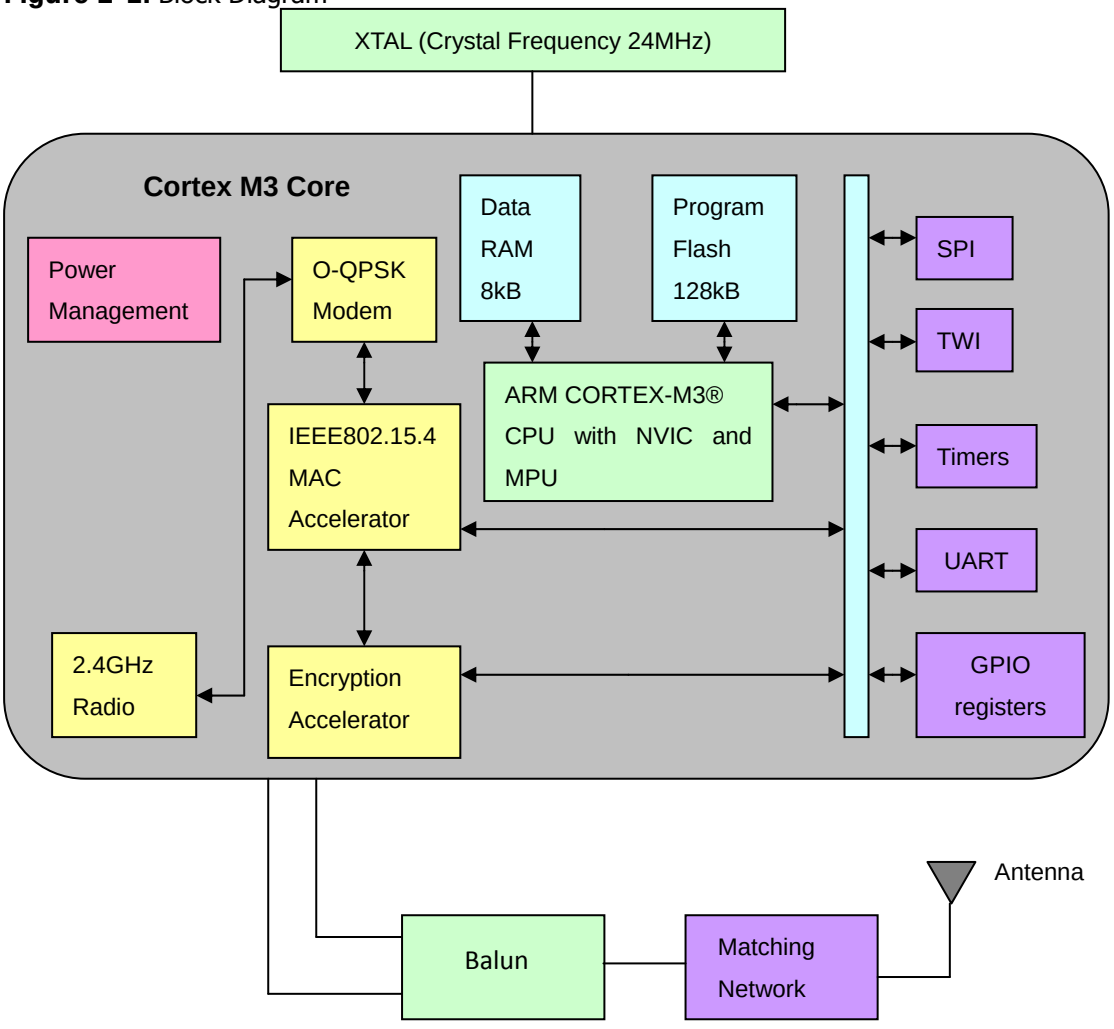
[2] ZigBee Specification. ZigBee Document 053474r17, October 19, 2007

2. Product Overview

2.1 Overview

REX3 is a low-power, high-sensitivity IEEE 802.15.4/ ZigBee-compliant module. This multi-functional state-of-art module occupies ultra-small space, which is comparable to a typical size of a single chip. Based on a solid combination of Rexense's latest MCU Wireless hardware platform, Rexense 802.15.4/ ZigBee Module offers superior radio performance, ultra-low power consumption, and exceptional ease of integration.

Figure 2-1. Block Diagram



REX3 Rexense 802.15.4/ ZigBee Module complies with the FCC (Part 15), IC and ETSI (CE) rules applicable to the devices radiating in uncontrolled environment.

REX3 Rexense 802.15.4/ ZigBee Module fully satisfies the requirements of the "Directive 2002/95/EC of the European Parliament and the Council of 27January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" (RoHS).

To jumpstart evaluation and development, Rexense also offers a complete set of evaluation and development tools. The ZigBee Development Kit comes with everything you need to develop and test your own applications.

3. Specifications

3.1 Electrical Characteristics

3.1.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Parameters	Min	Max
Voltage on any pin, except RESET with respect to Ground	-0.3V	VDD_PADS 0.3
DC Current total I/O Pins		40 mA
Total current into V_{DD}/V_{DDA} power lines (source)		150 mA
Input RF Level		+10 dBm

Note:

Absolute Maximum Ratings are the values beyond which damage to the module may occur.

Under no circumstances must the absolute maximum ratings given in this table be violated. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the module.

This is a stress rating only. Functional operation of the module at these or other conditions, beyond those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1.2 Test Conditions

Table 3-2. Test conditions (unless otherwise stated), VCC = 3.3V, Tamp = 25°C

Parameters	Range	Unit
Supply Voltage, VCC	2.1 to 3.6	V
Current Consumption: RX mode	29	mA
Current Consumption: TX mode	43	mA
Current Consumption: Radio is turned off, MCU is active 50% of the time	9.0	mA
Current Consumption: Power-sleep mode	0.4	μA

3.1.3 RF Characteristics

Table 3-3. RF Characteristics

Parameters	Condition	Range	Unit
Frequency Band		2400~2483.5	MHz
Numbers of Channels		16	
Channel Number		0B~1A	Hex
Channel Spacing		5	MHz
Transmitter Output Power		-32 to +7	dBm
Receiver Sensitivity	PER=1%	-99	dBm
On-Air Data Rate		250	kbps
TX Output/ RX Input Nominal Impedance	For unbalanced output	50	Ω

3.1.4 Microcontroller Characteristics

Table 3-4. Microcontroller Characteristics

Parameters	Condition	Range	Unit
On-chip Flash Memory size		128/192K	bytes
On-chip RAM size		8/12K	bytes
Operation Frequency		24	MHz

3.1.5 Module Interfaces characteristics

Table 3-5. Module Interfaces characteristics

Parameters	Condition	Range	Unit
UART Maximum Baud Rate		230400	bps
ADC Resolution/ Conversion Time	In single conversion mode	12/4096	Bits/μs
ADC Input Resistance		>1	MΩ
ADC Reference Voltage (VREF)		1.2	V
ADC Input Voltage		0 - VREF	V
I2C Maximum Clock		400	kHz
GPIO Output Voltage (High/Low)	-8/ 4 mA	2.8/ 0.9	V
Real Time Oscillator Frequency		32.768	kHz

3.2 Physical/Environmental Characteristics

Table 3-6. Physical/Environmental Characteristics

Parameters	Value	Comments
Size	31.60*20.70*3.90mm	
Weight	3.0g	
Operating Temperature Range	-40°C to +85°C	
Operating Relative Humidity Range	no more than 80%	

Note: 1. Minor degration of clock stability may occur.

3.3 Pin Configuration

Figure 3-1. REX3 Outline drawings (in mm)

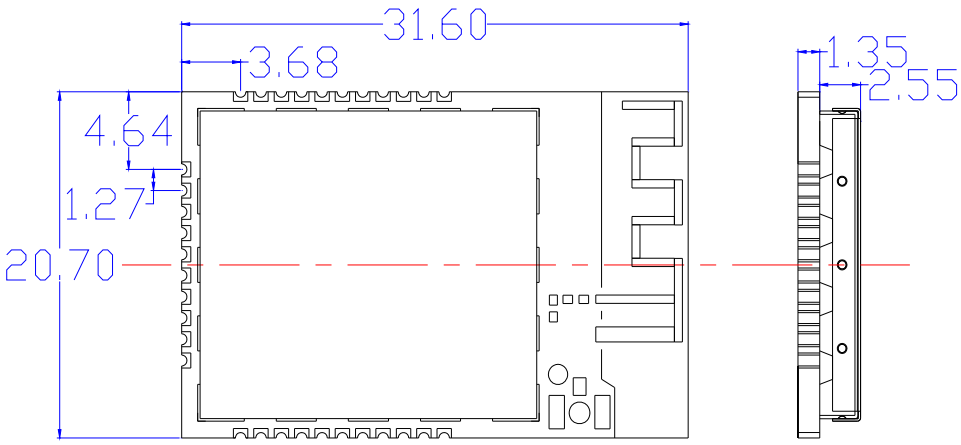


Figure 3-2. Recommended Footprint

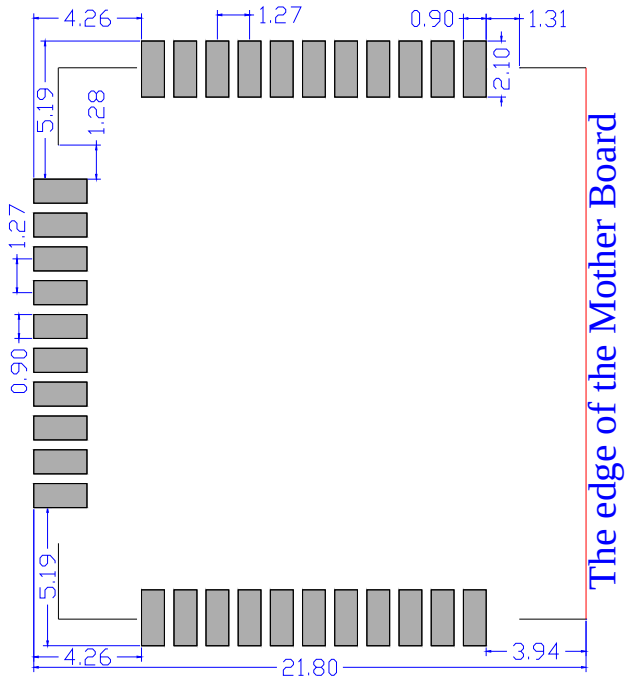


Figure 3-3. Pin Configuration

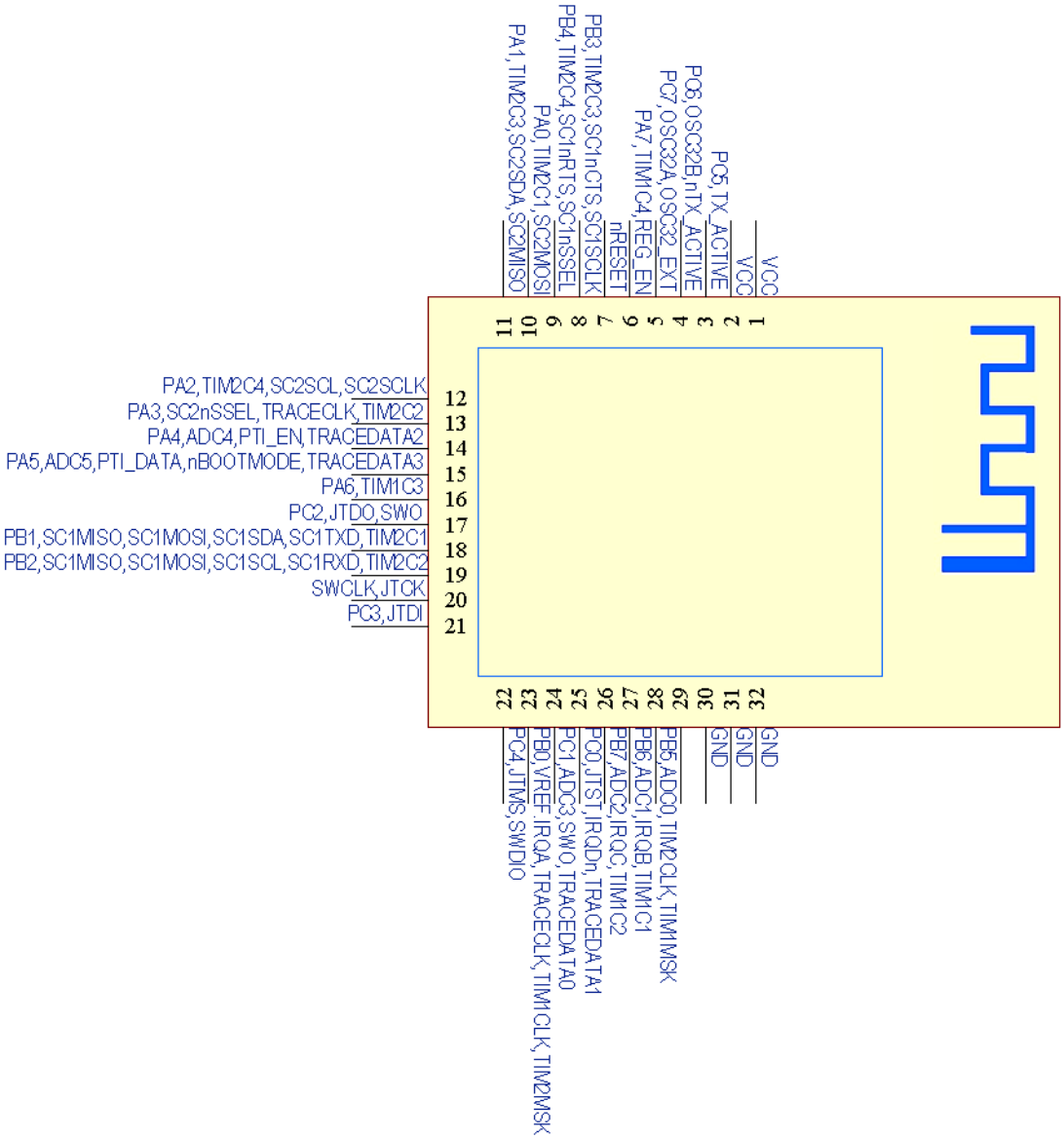


Table 3-7. Pin descriptions

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
1		3.3V	I	DC3.3V supply
2				
3	11	PC5	I/O	Digital I/O;

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		TX_ACTIVE	O	Logic-level control for external Rx/Tx switch. The MCU baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in Tx mode. Select alternate output function with GPIO_PCCFGH[7:4]
4	13	PC6	I/O	Digital I/O;
		OSC32B	I/O	32.768 kHz crystal oscillator Select analog function with GPIO_PCCFGH[11:8]
		nTX_ACTIVE	O	Inverted TX_ACTIVE signal (see PC5) Select alternate output function with GPIO_PCCFGH[11:8]
5	14	PC7	I/O	Digital I/O
		OSC32A	I/O	32.768 kHz crystal oscillator. Select analog function with GPIO_PCCFGH[15:12]
		OSC32_EXT	I	Digital 32 kHz clock input source
6	18	PA7	I/O High current	Digital I/O. Disable REG_EN with GPIO_DBGCFG[4]
		TIM1_CH4	O	Timer 1 Channel 4 output Enable timer output with TIM1_CCER Select alternate output function with GPIO_PACFGH[15:12] Disable REG_EN with GPIO_DBGCFG[4]
			I	Timer 1 Channel 4 input. (Cannot be remapped.)
		REG_EN	O	External regulator open drain output. (Enabled after reset.)
7	12	nRESET	I	Active low chip reset (internal pull-up)
8	19	PB3	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[15:12]
			I	Timer 2 channel 3 input. Enable remap with TIM2_OR[6].
		UART_CTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCFG[5] Select UART with SC1_MODE

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4] Select SPI with SC1_MODE Select alternate output function with GPIO_PBCFGL[15:12]
			I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
9	20	PB4	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGH[3:0]
			I	Timer 2 channel 4 input. Enable remap with TIM2_OR[7].
		UART_RTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[7] Enable with SC1_UARTCFG[5] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGH[3:0]
		SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
10	21	PA0	I/O	Digital I/O
		TIM2_CH1	O	Timer 2 channel 1 output Disable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[3:0]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
		SC2MOSI	O	SPI master data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[4] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[3:0]

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
			I	SPI slave data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
11	22	PA1	I/O	Digital I/O
		TIM2_CH3	O	Timer 2 channel 3 output Disable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 3 input. Disable remap with TIM2_OR[6].
		SC2SDA	I/O	TWI data of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[7:4]
		SC2MISO	O	SPI slave data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[7:4]
			I	SPI master data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
12	24	PA2	I/O	Digital I/O
		TIM2_CH4	O	Timer 2 channel 4 output Disable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[11:8]
			I	Timer 2 channel 4 input. Disable remap with TIM2_OR[7].
		SC2SCL	I/O	TWI clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[11:8]

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		SC2SCLK	O	SPI master clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[11:8]
			I	SPI slave clock of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
13	25	PA3	I/O	Digital I/O
		SC2nSSEL	I	SPI slave select of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
		TRACECLK	O	Synchronous CPU trace clock Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[5] Enable trace interface in ARM core Select alternate output function with GPIO_PACFGL[15:12]
		TIM2_CH2	O	Timer 2 channel 2 output Disable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[15:12]
			I	Timer 2 channel 2 input. Disable remap with TIM2_OR[5].
14	26	PA4	I/O	Digital I/O
		ADC4	Analog	ADC Input 4. Select analog function with GPIO_PACFGH[3:0].
		PTI_EN	O	Frame signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
		TRACEDATA2	O	Synchronous CPU trace data bit 2. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[3:0].
15	27	PA5	I/O	Digital I/O
		ADC5	Analog	ADC Input 5. Select analog function with GPIO_PACFGH[7:4].

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		PTI_DATA	O	Data signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4].
		nBOOTMODE	I	Embedded serial bootloader activation out of reset. Signal is active during and immediately after a reset on NRST.
		TRACEDATA3	O	Synchronous CPU trace data bit 3. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIO_PACFGH[7:4]
16	29	PA6	I/O High current	Digital I/O
		TIM1_CH3	O	Timer 1 channel 3 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PACFGH[11:8]
			I	Timer 1 channel 3 input (Cannot be remapped.)
17	33	PC2	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTDO	O	JTAG data out to debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35)
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[11:8] Enable Serial Wire mode (see JTMS description, Pin 35) Internal pull-up is enabled
18	30	PB1	I/O	Digital I/O
		SC1MISO	O	SPI slave data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select slave with SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		SC1MOSI	O	SPI master data out of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select master with SC1_SPICR Select alternate output function with GPIO_PBCFGL[7:4]
		SC1SDA	I/O	TWI data of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[7:4]
		SC1TXD	O	UART transmit data of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[4] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGL[7:4]
		TIM2_CH1	O	Timer 2 channel 1 output Enable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
19	31	PB2	I/O	Digital I/O
		SC1MISO	I	SPI master data in of Serial Controller 1 Select SPI with SC1_MODE Select master with SC1_SPICR
		SC1MOSI	I	SPI slave data in of Serial Controller 1 Select SPI with SC1_MODE Select slave with SC1_SPICR
		SC1SCL	I/O	TWI clock of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[11:8]
		SC1RXD	I	UART receive data of Serial Controller 1 Select UART with SC1_MODE
		TIM2_CH2	O	Timer 2 channel 2 output Enable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[11:8]

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
			I	Timer 2 channel 2 input. Enable remap with TIM2_OR[5].
20	32	SWCLK	I/O	Serial Wire clock input/output with debugger Selected when in Serial Wire mode (see JTMS description, Pin 35)
		JTCK	I	JTAG clock input from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-down is enabled
21	34	PC3	I/O	Digital I/O Either Enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description)
		JTDI	I	JTAG data in from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 35) Internal pull-up is enabled
22	35	PC4	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTMS	I	JTAG mode select from debugger Selected when in JTAG mode (default mode) JTAG mode is enabled after power-up or by forcing NRST low Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
		SWDIO	I/O	Serial Wire bidirectional data to/from debugger Enable Serial Wire mode (see JTMS description) Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
23	36	PB0	I/O	Digital I/O
		VREF	Analog O	ADC reference output. Enable analog function with GPIO_PBCFGL[3:0].
		VREF	Analog I	ADC reference input. Enable analog function with GPIO_PBCFGL[3:0]. Enable reference output with an ST system function.
		IRQA	I	External interrupt source A.
		TRACECLK	O	Synchronous CPU trace clock. Enable trace interface in ARM core. Select alternate output function with GPIO_PBCFGL[3:0].
		TIM1CLK	I	Timer 1 external clock input.

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		TIM2MSK	I	Timer 2 external clock mask input.
24	38	PC1	I/O	Digital I/O
		ADC3	Analog	ADC Input 3 Enable analog function with GPIO_PCCFGL[7:4]
		SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
		TRACEDATA0	O	Synchronous CPU trace data bit 0 Select 1-, 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
25	40	PC0	I/O High current	Digital I/O Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pin 35) and disable TRACEDATA1
		JRST	I	JTAG reset input from debugger Selected when in JTAG mode (default mode, see JTMS description) and TRACEDATA1 is disabled Internal pull-up is enabled
		IRQD (1)	I	Default external interrupt source D
		TRACEDATA1	O	Synchronous CPU trace data bit 1 Select 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[3:0]
26	41	PB7	I/O High current	Digital I/O
		ADC2	Analog	ADC Input 2 Enable analog function with GPIO_PBCFGH[15:12]
		IRQC (1)	I	Default external interrupt source C
		TIM1_CH2	O	Timer 1 channel 2 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[15:12]
			I	Timer 1 channel 2 input (Cannot be remapped)
27	42	PB6	I/O High current	Digital I/O
		ADC1	Analog	ADC Input 1 Enable analog function with GPIO_PBCFGH[11:8]
		IRQB	I	External interrupt source B

Module Pin No.	QFN48 Pin No.	Signal	Direction	Description
		TIM1_CH1	O	Timer 1 channel 1 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[11:8]
			I	Timer 1 channel 1 input (Cannot be remapped)
28	43	PB5	I/O	Digital I/O
		ADC0	Analog	ADC Input 0 Enable analog function with GPIO_PBCFGH[7:4]
		TIM2CLK	I	Timer 2 external clock input
		TIM1MSK	I	Timer 2 external clock mask input
29		NC	-	No connect
30		GND	-	Ground
31				
32				

3.4 Power Mode Configuration

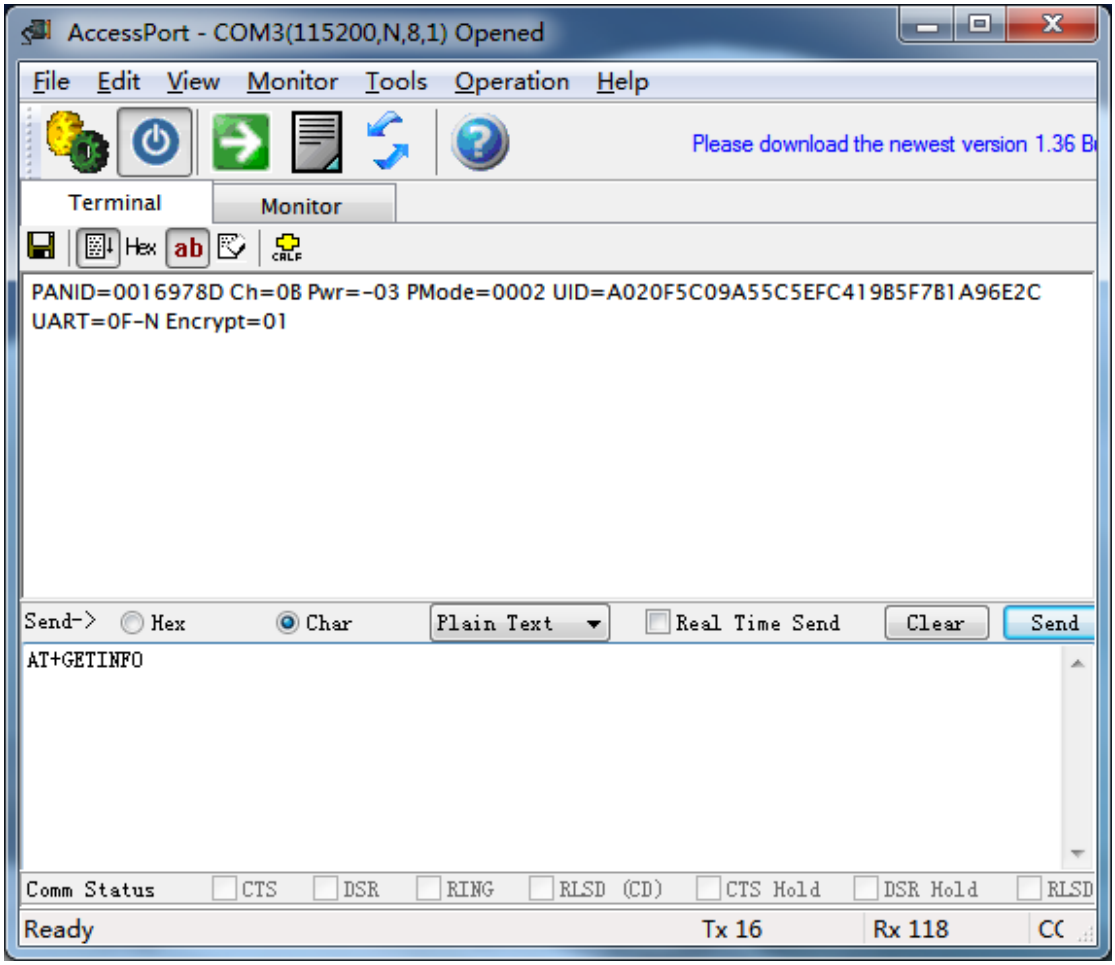
This part helps users to configure the power mode of Rexense 802.15.4/ ZigBee Module (currently only supports STM32W RexBee Module) through UART.

Users can refer to our AT commands manual to complete the UART configuration through serial port debugging software (such as AccessPort). The default UART baud rate of COO and HHU is set as 115200-8-N-1; Router set as 9600-8-N-1. The normal function of UART communication can be checked with command "AT+VER". For more detailed AT commands, please refer to www.rexense.com .

Acquire the current configuration information

Users can acquire the current configuration information of the module before UART debugging with command 'AT+GETINFO'.

Figure 3-3. AT+GETINFO



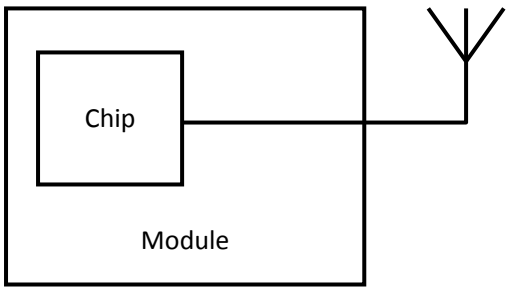
In Figure 3-3, parameters related with power mode configuration include:

Pwr=-03: The TX power of the chip is -3dBm;

PMode=0002: The wireless module works in **External Power Amplifier Mode**;

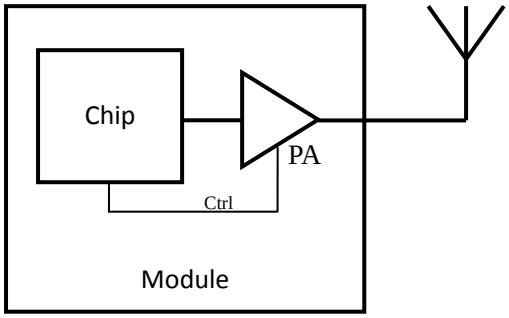
★ Important Note:

- **For standard Rexense 802.15.4/ ZigBee Module**, the TX power of the wireless chip means the TX power of the module. It is recommended that the TX power set as +07dBm to have better communication performance.



- **For enhanced Rexense 802.15.4/ ZigBee Module,** the TX power of the wireless

chip amplified by the power amplifier (PA) means the TX power of the module. It is recommended that the TX power set as -03dBm or -5dBm;



The TX power of the wireless chip can be configured with the command "AT+ SETPWR".

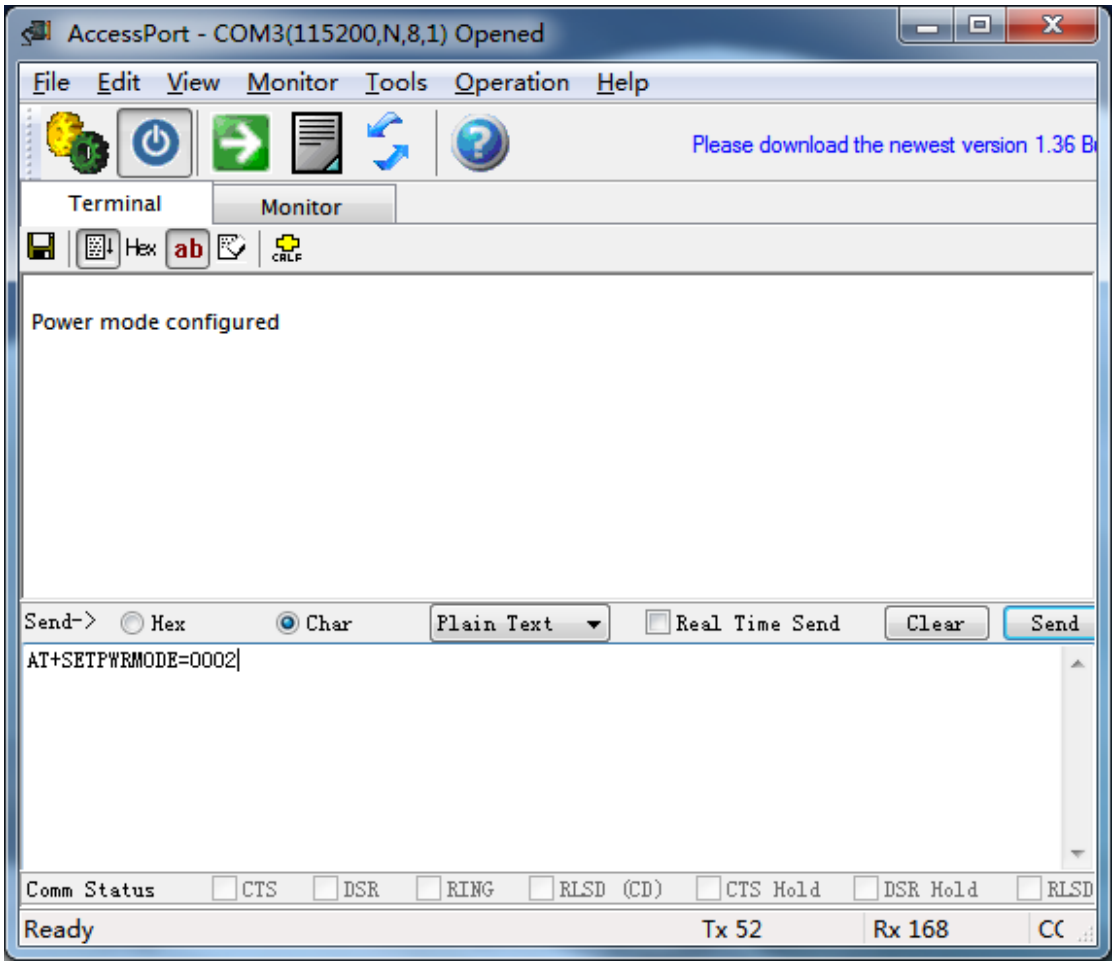
2. There are two power modes for Rexense 802.15.4/ ZigBee Module, standard power mode and external PA mode. As enhanced Rexense 802.15.4/ ZigBee Module works in external PA mode, user need to use command "AT+SETPWRMODE" to configure the power mode of the Rexense 802.15.4/ ZigBee Module.

- Standard Rexense 802.15.4/ ZigBee Module works in **standard power mode** configured by the command below:

AT+SETPWRMODE=0000

- Enhanced Rexense 802.15.4/ ZigBee Module works in **external PA mode** configured by the command below:

AT+SETPWRMODE=0002



External Antenna Configuration

For **enhanced Rexense 802.15.4/ ZigBee Module**, there are two antenna options;

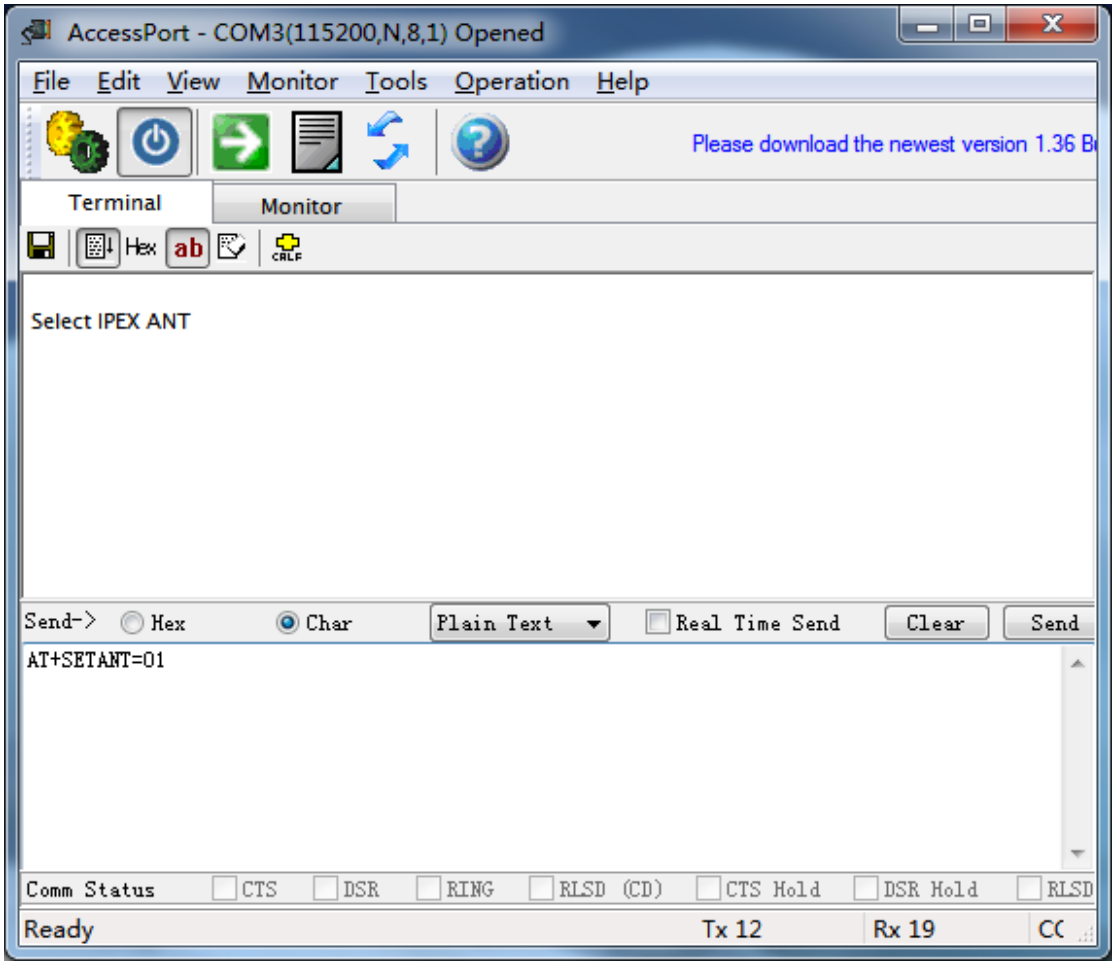
1. On-board PCB antenna;
2. U.FL (IPEX) Jack

- AT Command for on-board PCB antenna (please refer to 3.5.1 for more detailed information of PCB antenna):

AT+SETANT=00

- If U.FL jack is used, it's necessary to use the antenna cable and the SMA antenna at the same time. (please refer to 3.5.3 for more detailed information of U.FL jack). The AT command for U.FL jack:

AT+SETANT=01

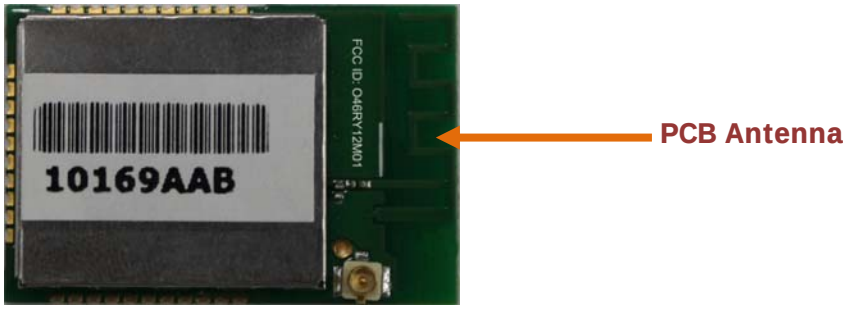


3.5 Antenna Specifications

There're 3 antenna options for the Standard Rexense 802.15.4/ ZigBee Module (REX3), as shown below.

3.5.1 PCB Antenna

Figure 3-4. PCB Antenna



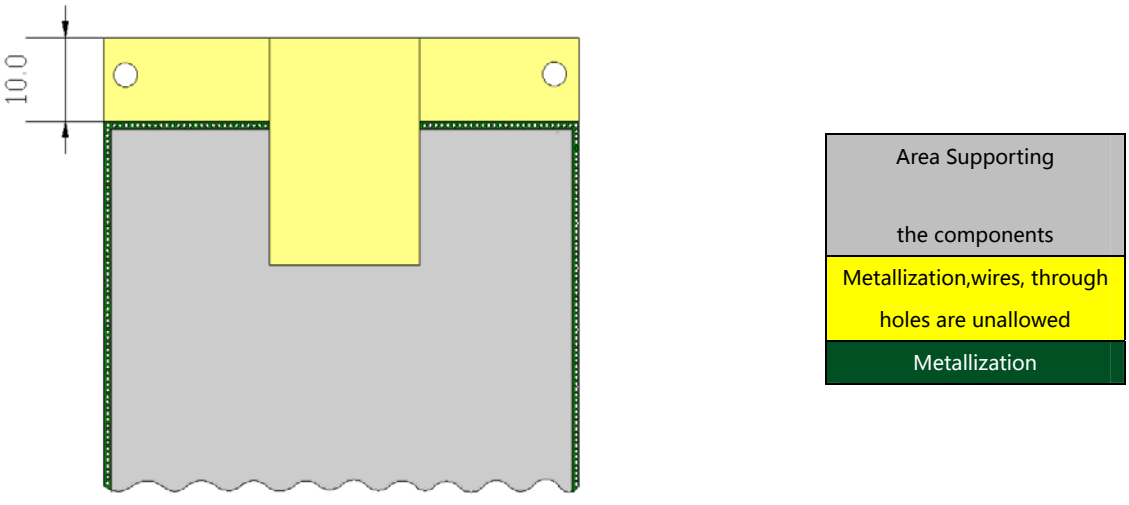
When PCB antenna output is selected, the following points should be noted:

1. Please avoid installing the module in a complete metal enclosure.

2. Please avoid placing high profile components next to antenna.

3. Rexense 802.15.4/ ZigBee Module should not be placed next to consumer electronics which might interfere with ZigBee's RF frequency band.

Figure 3-5. PCB Layout of the Proposed Antenna Selection

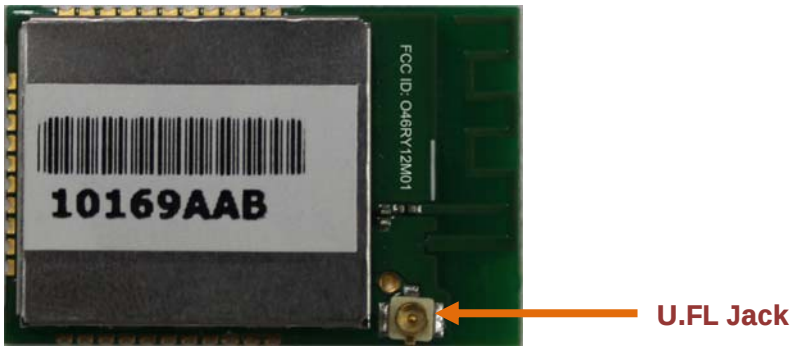


The board design should prevent propagation of microwave field inside the board material. Electromagnetic waves of high frequency may penetrate the board thus making the edges of the board radiate, which may distort the antenna pattern.

To eliminate this effect, metalized and grounded holes must be placed around the board's edges.

3.5.2 U.FL Jack to SMA Antenna

Figure 3-6. U.FL Jack



Note: when the U.FL (IPEX) jack is used, it's necessary to use the antenna cable and the SMA antenna at the same time. Please see the pictures for them as below.

Figure 3-7. Antenna Cable

Antenna cable (AN12/ AN8): cable length (12cm/ 8cm) and insertion loss (1dBi)

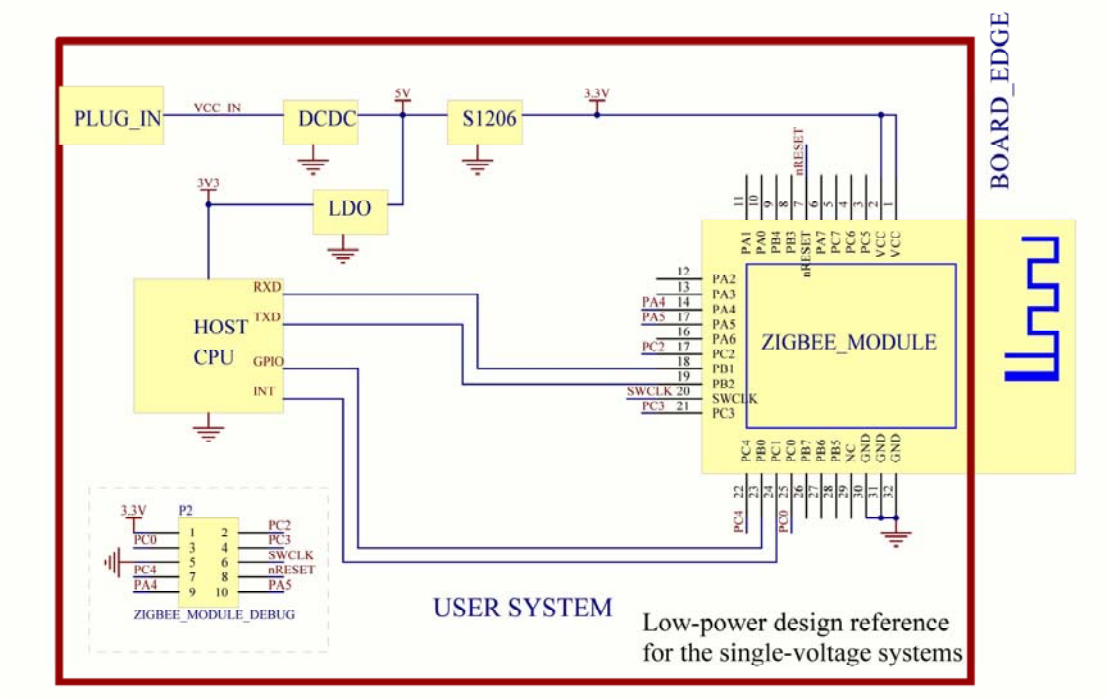
Figure 3-8. SMA Antenna

SMA antenna (AN2400): gain (2dBi)

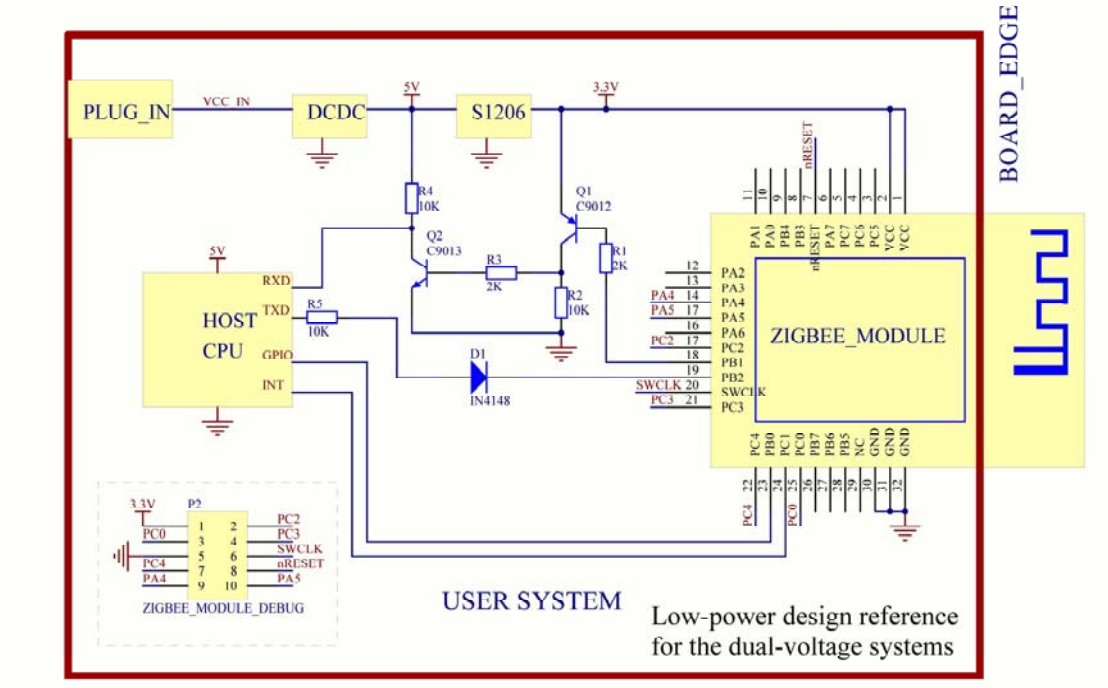
Figure 3-9. Assembled Picture

3.6. Module Circuit Reference Design

3.6.1 Module Reference Design (Single Voltage)



3.6.2 Module Reference Design (Dual-Voltage)



3.7 Module Test Instructions

Figure 3-10. Standard JTAG Connection (1)

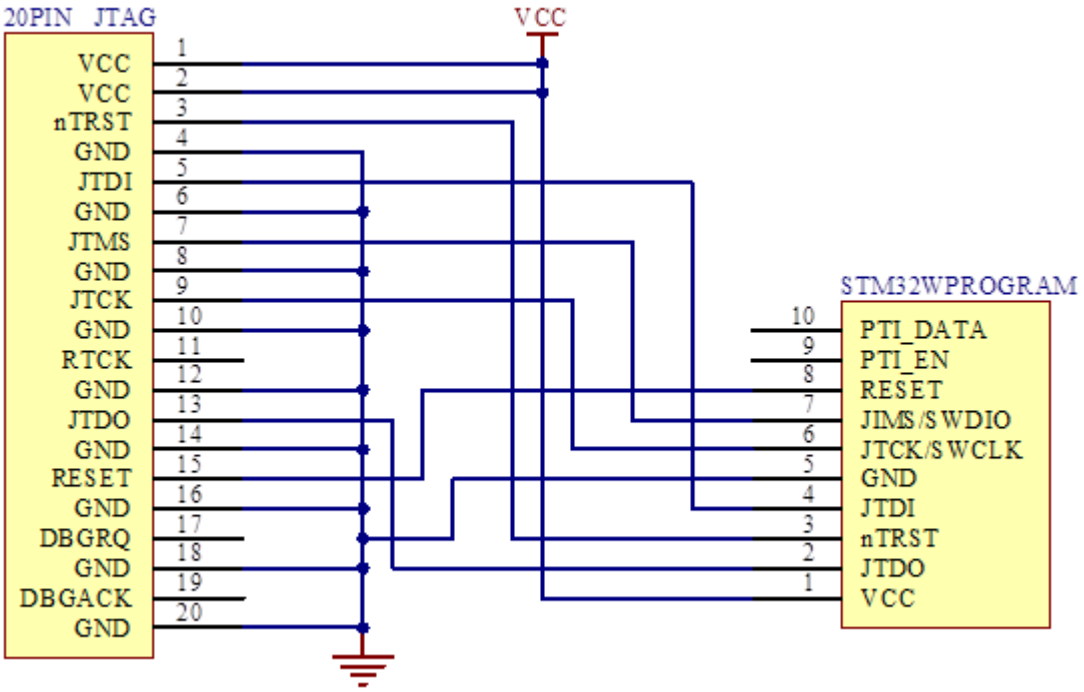
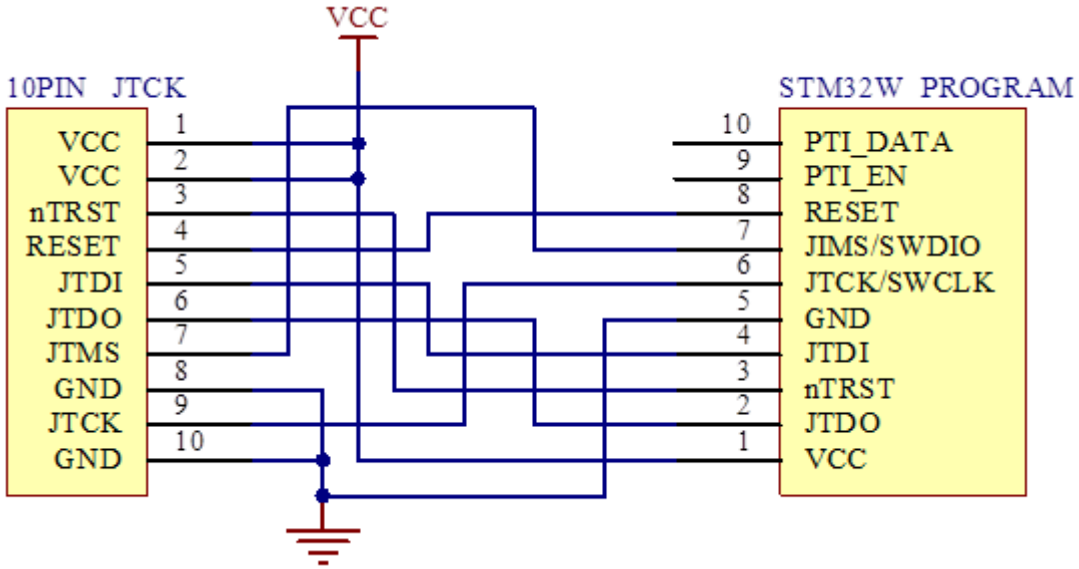


Figure 3-11. Standard JTAG Connection (2)



As shown in the above two figures, the first figure shows 20-pin JTAG interfaces and module debugging& programming interfaces ; the second figure shows 10-pin JTAG interfaces and module debugging and programming interfaces. So far, standard JTAG

connection is not supported for our products. Instead, we recommend the use of SWD connection shown as follows.

Figure 3-12. SWD connection (1)

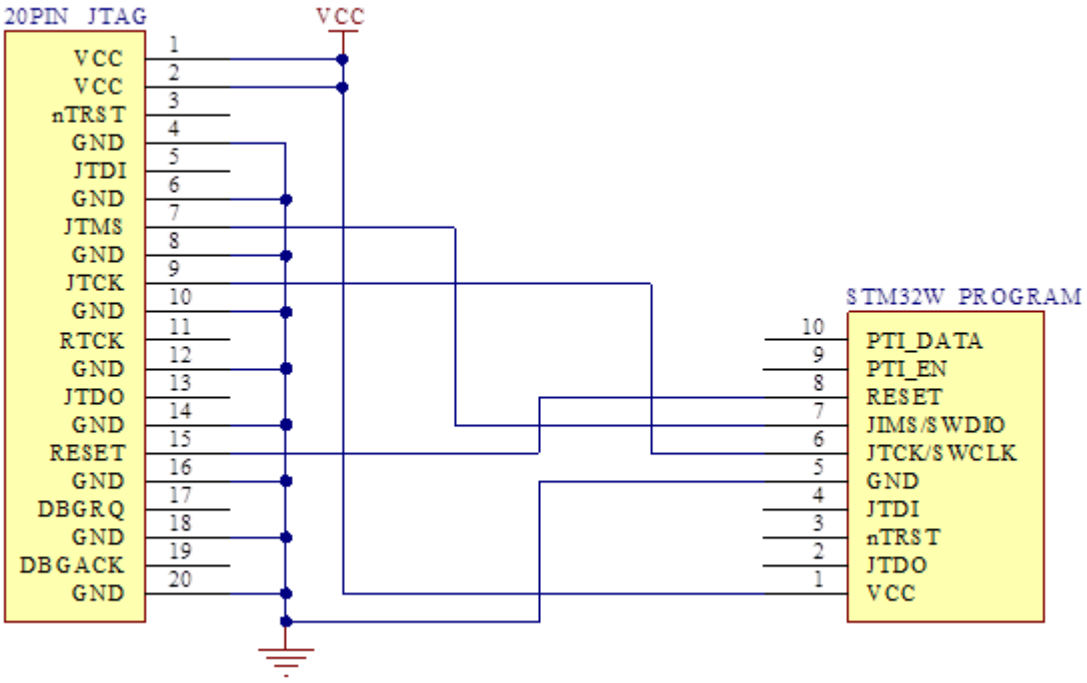


Figure 3-13. SWD connection (2)

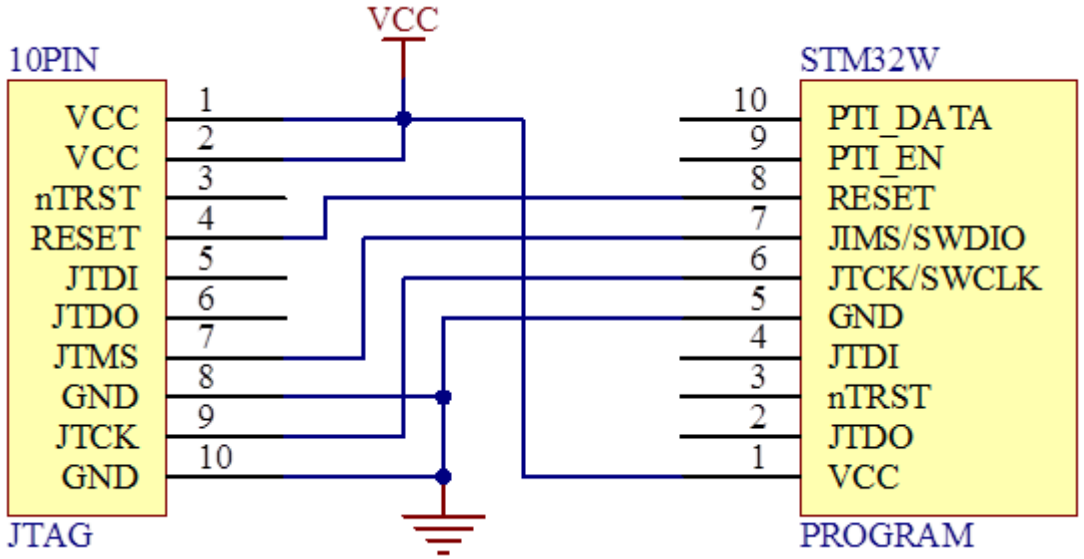
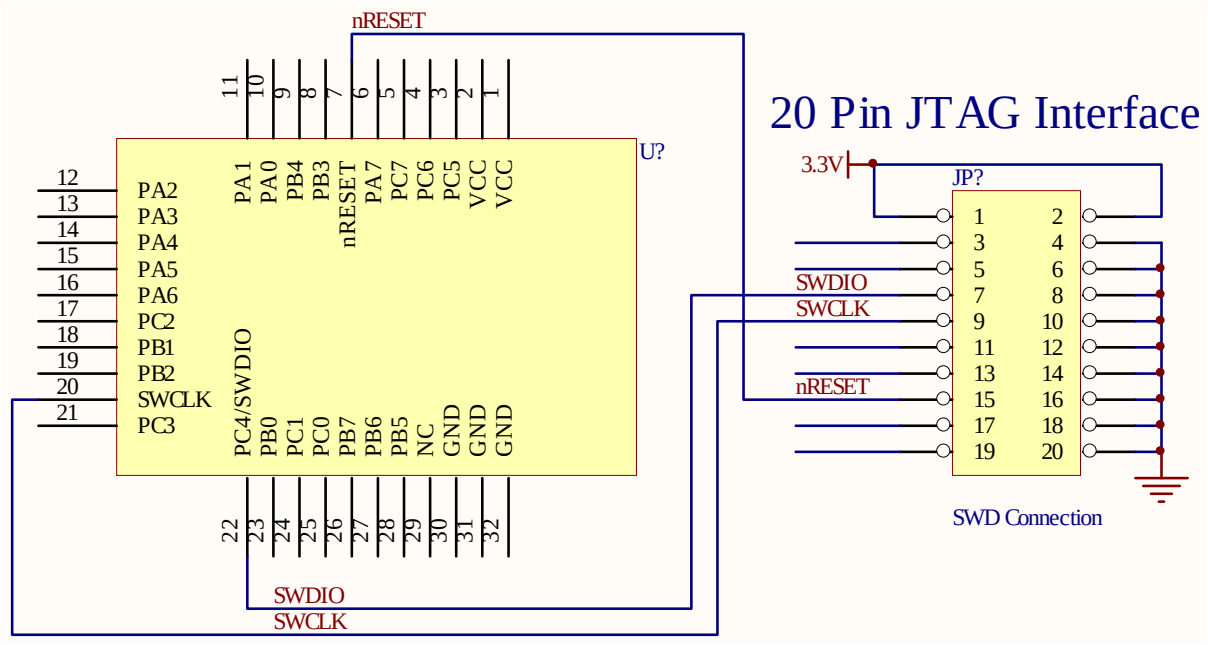


Table 3-8. The relation between the MCU debugging & programming interfaces and JTAG interfaces

20-pin JTAG Interface Pin Number (Name)	10-pin JTAG Interface Pin Number (Name)	10-pin module D&P Interface JTAG Pin Number (Name)	10-pin module D&P Interface SWD Pin Number (Name)
1(VCC)	1\2(VCC)	1(VCC)	1(VCC)
2(VCC)	——	——	——
3(nTRST)	3(nTRST)	3(nTRST)	——
4(GND)	——	——	——
5(JTDI)	5(JTDI)	4(JTDI)	——
6(GND)	——	5(GND)	5(GND)
7(JTMS)	7(JTMS)	7(JTMS)	7(SWDIO)
8(GND)	8(GND)	——	——
9(JTCK)	9(JTCK)	6(JTCK)	6(SWCLK)
10(GND)	10(GND)	——	——
11(RTCK)	——	——	——
12(GND)	——	——	——
13(JTDO)	6(JTDO)	2(JTDO)	——
14(GND)	——	——	——
15(RESET)	4(RESET)	8(RESET)	8(RESET)
16(GND)	——	——	——
17(DBGRQ)	——	——	——
18(GND)	——	——	——
19(DBGACK)	——	——	——
20(GND)	——	——	——
——	——	9(PTI_EN)	9(PTI_EN)
——	——	10(PTI_DATA)	10(PTI_DATA)

Figure 3-14. Module Program and Debug Interface Connection



3.8 Test Result of RF Performance

Figure 3-15. Receiving Sensitivity

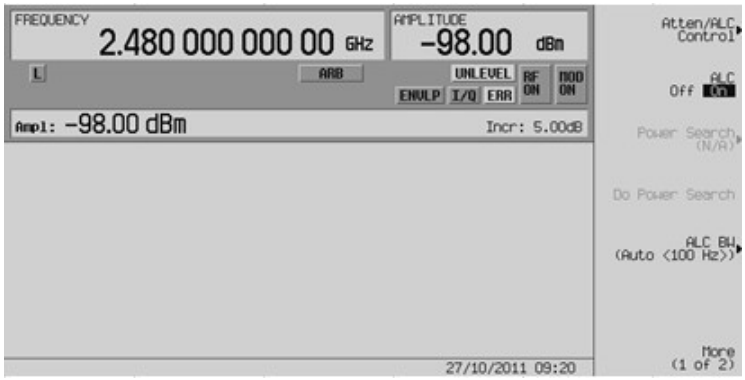


Figure 3-16. Carrier Signal Testing

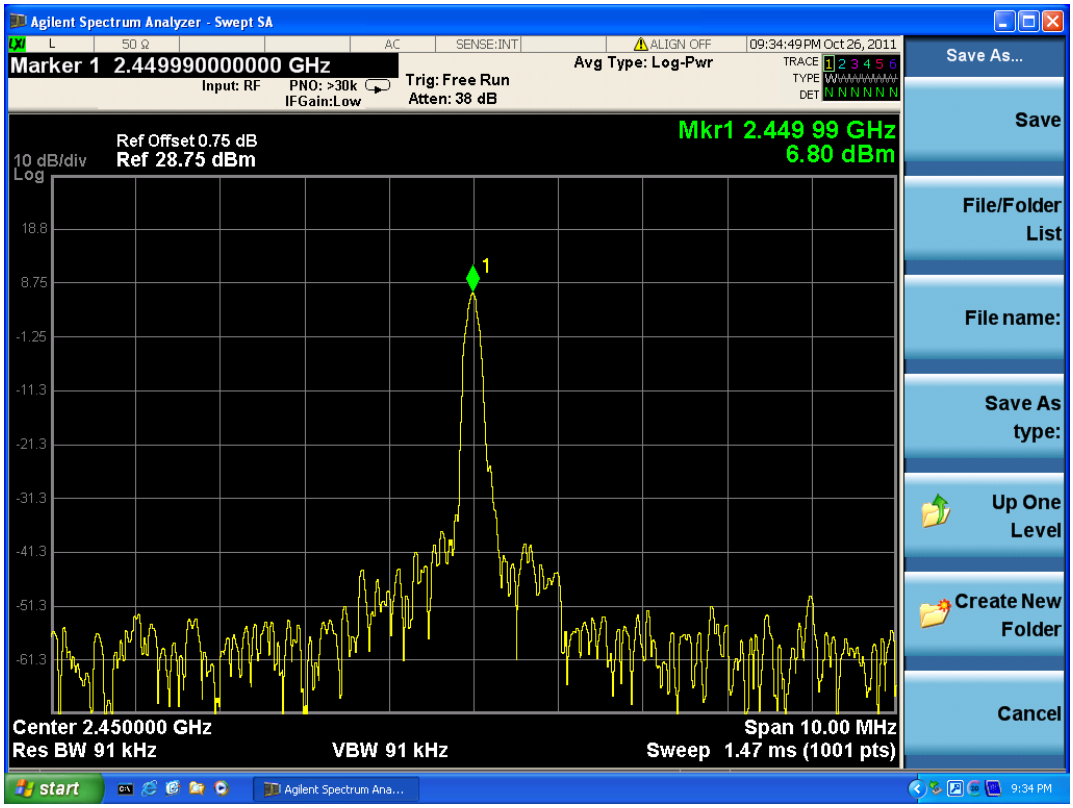


Figure 3-17. Modulating Signal Testing


Agilent Spectrum Analyzer - Swept SA
Marker 1 2.449470000000 GHz
Input: RF
PNO: >30k
IFGain:Low
Trig: Free Run
Atten: 38 dB
Avg Type: Log-Pwr
Avg|Hold:>100/100
09:40:50 PM Oct 26, 2011
Ref Offset 0.75 dB
10 dB/div
Log
Ref 28.00 dBm
Mkr1 2.449 47 GHz
5.084 dBm
18.0
8.00
-2.00
-12.0
-22.0
-32.0
-42.0
-52.0
-62.0
Center 2.450000 GHz
Res BW 91 kHz
VBW 910 kHz
Span 10.00 MHz
Sweep 1.13 ms (1001 pts)
Save As...
Save
File/Folder List
File name:
Save As type:
Up One Level
Create New Folder
Cancel
start
Agilent Spectrum Ana...
9:40 PM

4. Agency Certifications

FCC Certification

This equipment complies with Part 15 of the FCC rules and regulations.

To fulfill FCC Certification requirements, an OEM manufacturer must comply with the following regulations:

1. The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:

Example of label required for OEM product containing REX3 802.15.4/ ZigBee Module

> **Contains FCC ID: O46RY12M01**
> The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Any similar wording that expresses the same meaning may be used.

2. To be used with the REX3 802.15.4/ ZigBee Module, the external antennas have been tested and approved which are specified in *Approved Antenna List*. The REX3 802.15.4/ ZigBee Module may be integrated with other custom design antennas which OEM installer must authorize following the FCC 15.21 requirements.

WARNING: The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

IMPORTANT: This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19).

The internal/external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

IMPORTANT: Modifications not expressly approved by this company could void the user's authority to operate this equipment (FCC section 15.21).

For a Class B digital device or peripheral, the instructions furnished the user shall include the following or similar statement, placed in a prominent location in the text of the manual:

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This

equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

Approved Antenna List

REX3 802.15.4/ ZigBee Module has been tested and approved for use with the antennas listed in the table below.

Table 4-1. Approved Antenna List

Part Number	Manufacturer	Description	Gain (dBi)	Min. Separation (cm)
AN2400	Off the shelf	Omni, with SMA-J connector, frequency range 2.4-2.5 GHz	2	20

5. Contact Us

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