FCC ID: O3U-98163

Technical Description :

The brief circuit description is listed as follows :
- L201 and associated circuit act as Antenna and Antenna Matching Circuit for the head reader.
- L202 and associated circuit act as Antenna and Antenna Matching Circuit for the hand reader.
- U201(HL5233), X201 and associated circuit act as RFID reader (head reader) and 13.56 MHz Oscillator.
- U202(HL5233), X202 and associated circuit act as RFID reader (hand reader) and 13.56 MHz Oscillator.
- U101(RSC-4128) acts as MCU and Speech Recognition Processor.
- U102(K8D3216UBC) acts as NOR-type Flash Memory.
- U103 and U104 act as Logic Gates.
- U105(AT24C04N) acts as EEPROM.
- U301(74HC374) acts as 3-State Octal D-type Flip-Flop.
- U302(74HC373) acts as 3-State Octal D-type Latch.
- U2 acts as Audio Amplifier.
- Q302 to Q307 and associated circuit act as Eye Motor Driver.
- Q308 to Q313 and associated circuit act as Mouth Motor Driver.
- CN101 acts as cartridge Connector.

Antenna Used :

Two loop antennas have been used.

HL5233
HF RFID Reader IC
Preliminary Version, March, 2003

Features

- Low standby current.
- Low power consumption.
- Simple application circuit.
- Stable performance.
- The system and oscillator can be enable separately.
- 3 kinds of decoder outputs.
- Level hold mode and one-shot trigger mode.
- High active and low active output selectable.

Applications

- Toy RFID.
- Asset control.
- Contactless entry control.
- Education.

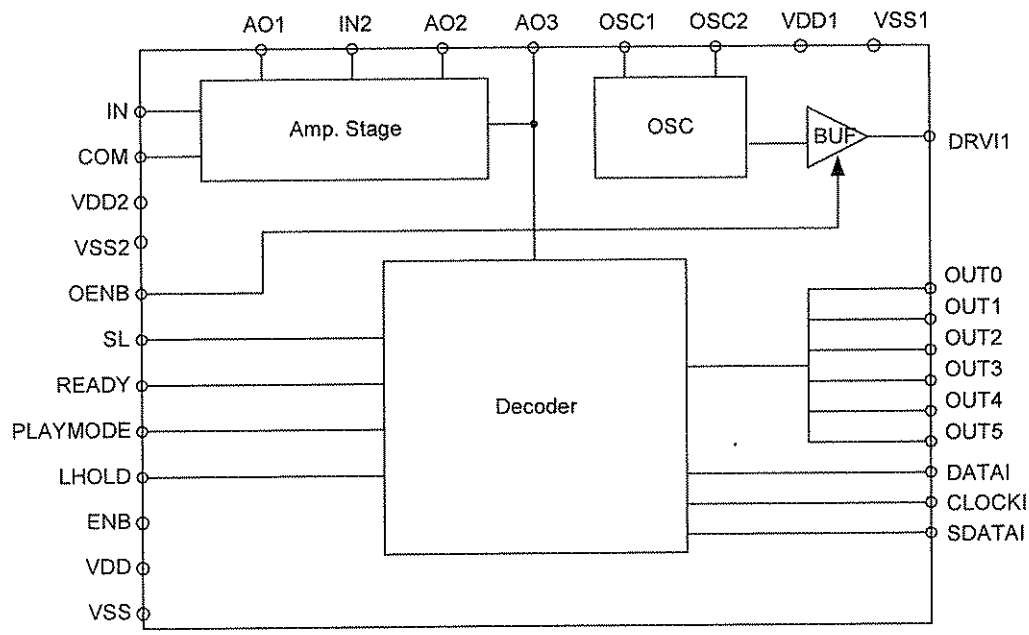
General Description

HL5233 is a CMOS IC used to perform the function of a RFID Reader. A RFID contains two parts: RFID TAG (HL5230) and RFID Reader (HL5233). HL5233 contains of a 13.56MHz crystal oscillator, a 13.56MHz output buffer, a preamplifier and data decoder. The output buffer drives an antenna which can transmits RF signal to the RFID TAG.

If TAG is close enough to the Reader, the encoder of TAG will send out a data train. The data train is used to modulate the RF signal in the TAG, and the amplitude of RF signal in the Reader will be modulated also. Preamplifier is used to amplify the modulating signal. The decoder is used to decoder the encoded data transmitted from TAG.

There are three kinds of output data: Synchronous, Asynchronous and Direct drive outputs. In order to interface to most of power Speech IC, the data rate of the outputs is slower than the data rate of the RFID TAG.

Block Diagram



Absolute Maximum Ratings

Power Supply 5V
Input Voltage ..... VSS-0.3V to VDD+0.3V
Operating Temperature ..... 0°C to 60°C
Storage Temperature ..... -65°C to 125°C

Electrical Characteristics

SYSTEM	DESCRIPTION	TEST CONDITION	LIMIT			UNIT
			MIN.	TYP.	MAX.	
VDD	Supply Voltage		3	4.5	5	V
VIL	Input Voltage Low	VDD=4.5V			0.3*VDD	V
VIH	Input Voltage High	VDD=4.5V	0.7*VDD			V
VOSC	Oscillator Starting Voltage			2.2		V
IOP1	Operating Current 1	VDD=4.5V		19*		mA
IOP2	Operating Current 2 (Driver Off)	VDD=4.5V		0.4		mA
IST	Stand-by Current	VDD=4.5V		0.5		uA

* IOP depends on external coil.

Functional Description

There are three major function provided by HL5233: support a 13.56MHz driver, to transform DATA Bit rate for easy interface with MCU or power Speech IC and to provide direct decoder output.

After received the modulating signal from the RFID TAG, the modulating signal is amplified and filtered by preamplifier. There is decoder and error detector built in the HL5233. The decoded output can be sent to output pin directly, or encoded again at a slower bit rate. When PLAYMODE = 1, there are 8 direct output provided. Besides the 3 bits which is used as decoder inputs, there is 1 bit, which is used as parity check bit. The output will be activated only when parity is correct. In HL5233 even parity is used, Bit0~Bit2 is used as decoder input and Bit7 is parity Bit.

OENB is coil driver enable pin. When OENB=0, coil driver is off, while others circuit still work.

SENSORY®

RSC-4128
Speech Recognition Processor

Data Sheet

General Description

The RSC-4128 represents Sensory's next generation speech and analog I/O mixed signal processor. The RSC-4128 is designed to bring advanced speech I/O features to cost sensitive embedded and consumer products. Based on an 8-bit microcontroller, the RSC-4128 integrates speech-optimized digital and analog processing blocks into a single chip solution capable of accurate speech recognition; high quality, low data-rate compressed speech; and advanced music. Products can use one or all features in a single application.

The RSC-4128 supports Sensory Speech™ 7 technology, which includes advanced speech algorithms that add features and improve performance. Capable of running both new HMM and enhanced neural network technologies, accuracy in all kinds of noise is dramatically improved. New Speaker Verification technology is perfect for voice password security applications that must work in noisy environments. New high quality compressed speech technology reduces data rates by 5 times. New 8 voice MIDI-compatible music includes drum tracks, effectively increasing instruments beyond 8. Simultaneous music and speech rounds out the Sensory Speech™ 7 technology.

The RSC-4128 also supports the revolutionary capability of creating speaker independent recognition sets by simply typing in the desired recognition vocabulary! A few keystrokes creates a recognition set in seconds without the wait or cost of recording sessions to train the recognizer, speeding time to sales.

A new and unique Audio Wakeup feature listens while the RSC-4128 is in power down mode. When an audio event such as a clap or whistle occurs, Audio Wakeup will wakeup the RSC-4128 for speech or application tasks. Audio Wakeup is perfect for battery applications that require continuous listening and long battery life.

In addition to improved recognition performance, the RSC-4128 provides further on-chip integration of features. A complete speech I/O application can be built with as few additional parts as a clock crystal, speaker, microphone, and few resistors and capacitors.

Moreover, the RSC-4128 provides an unprecedented level of cost effective system-on-chip (SOC) integration, enabling many applications that require DSP and/or audio processing. The RSC-4128 may be used as a general-purpose mixed signal processor platform for custom algorithms, technologies and applications.

Features

Full Range of Sensory Speech™ 7 Capabilities

- Enhanced Word Spotting capability (10 SI or 4 SD words) in parallel
- Noise robust Speaker Independent, Dependent & Continuous Listening recognition
- Speaker Verification (SVWS) – Noise robust voice biometric security
- High quality, 3.7-7.8 kbps speech synthesis & sound effects with Sensory "SX" synthesis technology
- 8 voice MIDI-compatible music synthesis coincident with speech; drum track feature enables additional voices
- Voice record & playback
- Audio Wakeup from sleep

Integrated Single-Chip Solution

- 8-bit microcontroller
- ROMless, 128KByte and 256KByte ROM options
- 16 bit ADC, 10 bit DAC and microphone pre-amplifier
- Independent, programmable Digital Filter engine
- 4.8 KBytes total RAM (256Bytes "user" application RAM)
- Five timers (3 GP, 1 Watchdog, 1 Multi Tasking)
- Twin-DMA, Vector Math accelerator, and Multiplier
- Built-in Analog Comparator Unit (4 inputs)
- External memory bus: 20-bit Address(1Mbyte), 8-bit Data
- On chip storage for SD, SV, templates (10 templates)
- Code security through no ROM dump capability
- Uses low cost 3.58MHz crystal (internal PLL)
- Low EMI design for FCC and CE requirements
- 24 configurable I/O lines with 10 mA (typical) outputs
- Fully nested interrupt structure with up to 8 sources
- Optional Real Time Clock

Long Battery Life

- 2.4 – 3.6V operation
- 12mA (typical) operating current at 3V
- 2 low power modes; 1 µA typical sleep current

Full Suite of Quick & Powerful Tools

- Quick Text-to-SI (T2SI) text entry to build noise robust SI recognition sets – low cost & push-button – no recording!
- Quick Synthesis for push-button speech compression
- Integrated Development Environment, C Compiler, Debugger & In Circuit Emulator from Phyton, Inc.

RSC-4128 Overview

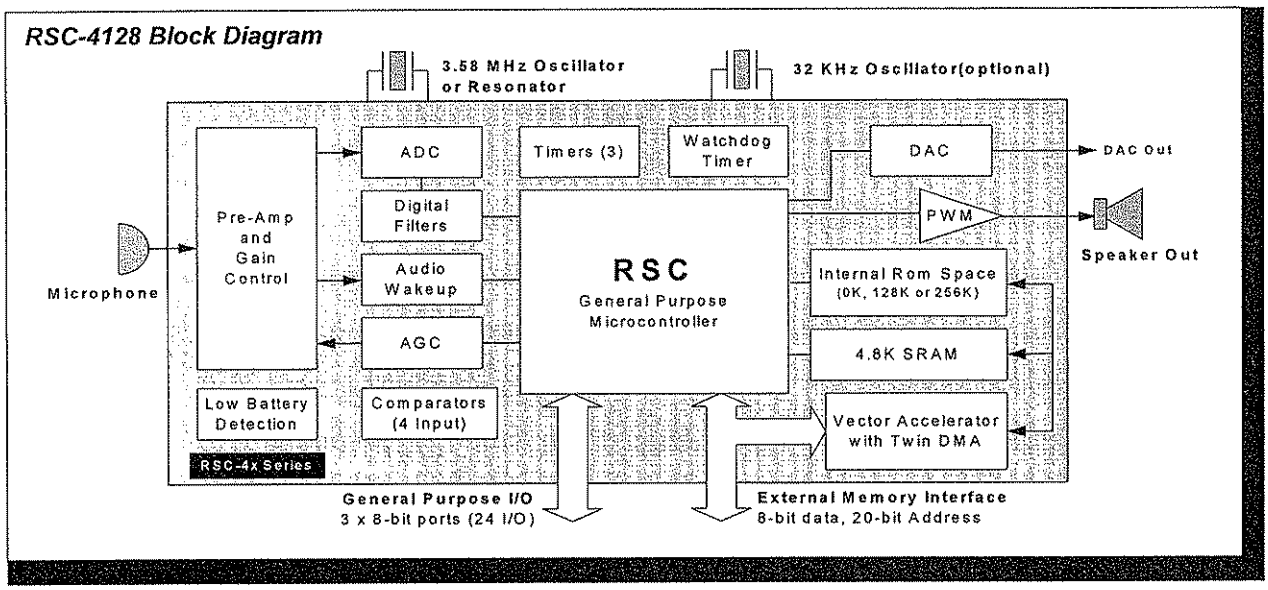
The RSC-4128 is a member of the Interactive Speech™ line of products from Sensory. It features a high-performance 8-bit microcontroller with on-chip ADC, DAC, preamplifier, RAM, ROM (except on ROM-less version), and optimized audio processing blocks. The RSC-4128 is designed to bring a high degree of integration and versatility into low-cost, power-sensitive applications. Various functional units have been integrated onto the CPU core in order to reduce total system cost and increase system reliability.

The RSC-4128 operates in tandem with Sensory Speech™ 7 firmware, an ultra compact suite of recognition and synthesis technologies. This reduced software footprint enables, for example, products with over 150 seconds of compressed speech, multiple speaker dependent and independent vocabularies, speaker verification, and all application code built into the RSC-4128 as a single chip solution. Revolutionary Text-to-Speaker-Independent (T2SI) technology allows the creation of SI recognition sets by simply entering text.

The CPU core embedded in the RSC-4128 is an 8-bit, variable-length-instruction microcontroller. The instruction set is similar to the 8051 microcontroller, and has a variety of addressing mode, *MOV* and 16 bit instructions. The RSC-4128 processor avoids the limitations of dedicated A, B, and DPTR registers by having completely symmetrical sources and destinations for all instructions.

The RSC-4128 provides a high level of on-chip features and special DSP engines, providing a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. The full suite of industry standard tools for easy product development makes the RSC-4128 an ideal platform for consumer electronics.

RSC-4128 Block Diagram



Speech Technologies

Speech Recognition

The RSC-4128 is designed to support HMM (Hidden Markov Modeling) as well as Neural Network technologies provided in Sensory Speech™ 7 firmware, to perform speaker independent (SI) speech recognition. Speaker independent recognition requires on-chip or off-chip ROM to store the words to be recognized.

Speaker dependent (SD) recognition requires programmable memory to store personalized speech templates. This programmable memory may be on-chip SRAM or off-chip Serial EEPROM, Flash Memory, or SRAM.

The RSC-4128 has several additional speech recognition features as described below:

- *Speaker Independent* recognition requires no user training. The RSC-4128 can recognize up to 20 words in an active set (number of sets is limited only by internal ROM or external memory size). Text-to-SI (T2SI) recognition, based on HMM technology, allows creation of SI recognition sets in seconds by simply typing in the vocabulary desired, with no costs or delays associated with recording and training the recognizer.
- *Speaker Dependent* recognition allows the user to create names for products or customize vocabularies. Up to 100 words can be recognized in an active set (number of sets is limited only by internal ROM or external memory size). The RSC-4128 can store up to 10 SD words in on-chip SRAM.
- *Continuous Listening* allows the chip to continuously listen for a specific trigger word. With this feature, a product "activates" when a specific word is spoken, framed by quiet before and after. Continuous listening provides the lowest false fire rate for trigger words.
- *Word Spotting* allows the chip to continuously recognize for up to 10 SI or 5 SD words at a time. In word spotting mode, the word(s) to be recognized may be spoken in the middle of speech.

Speaker Verification

The RSC-4128 also supports Sensory's speaker verification (SV) technology – the most successful biometric security on the market. After a speaker trains the chip on a specific word or words, the chip is able to identify whether a particular word is spoken by the original speaker. The RSC-4128 can store up to 10 SV templates on-chip, or more with external programmable memory.

Speech and Music Synthesis

The RSC-4128 provides high-quality speech synthesis using state-of-the-art frequency domain techniques in Sensory's new "SX" synthesis technology. Typical data rates for SX are approximately 6000 bits per second. One may select various data rates from approximately 3.7 to 7.8Kbps to manage speech quality versus allotted memory.

Speech, music and sound effects may also be produced using the RSC-4128 8 bit, 58Kbps or 4 bit, 30Kbps compression technologies.

The RSC-4128 provides high-quality, eight-voice, wave table music synthesis which allows multiple, simultaneous instruments for harmonizing. The RSC-4128 uses a MIDI-like system to generate music. One or more of the eight voices may be speech playback instead of music. One or more of the eight voices may be a drum track comprising multiple drums. In effect, this allows the number of simultaneous instruments to exceed 8.

Speech and music synthesis requires on-chip or off-chip ROM to store data for synthesis playback. Easy to use tools allow the developer to record and compress their own voice talents and create with the push of a button, or to create their own MIDI scores and instruments.

Record and Playback

The RSC-4128 can perform speech record and playback (sometimes called "voice memo") at various compression levels depending on the quantity and quality of playback desired. Data rates less than 14,000 bits per second are achievable while maintaining very high quality reproduction. The record and playback technology also performs silence removal to improve sound quality and reduce memory requirements.

RSC-4128 Architecture

The RSC-4128 is a highly integrated speech and analog I/O mixed signal processor that combines:

- 8-bit microcontroller with enhanced instructions and interrupt control, superior register architecture, independent Digital Filter engine and "L1" Vector Math Accelerator
- On-chip ROM and RAM (4.8 Kbytes), and the ability to address off-chip RAM, ROM, EPROM or Flash.
- Input microphone preamp and 16 bit Analog-to-Digital Converter (ADC) for speech and audio/analog input
- 10 bit Digital-to-Analog Converter (DAC), and 10 bit Pulse Width Modulator (PWM) to directly drive a speaker or other analog device
- Low power Audio Wakeup from power down mode, when a selected audio event, such as clap or whistle, occurs

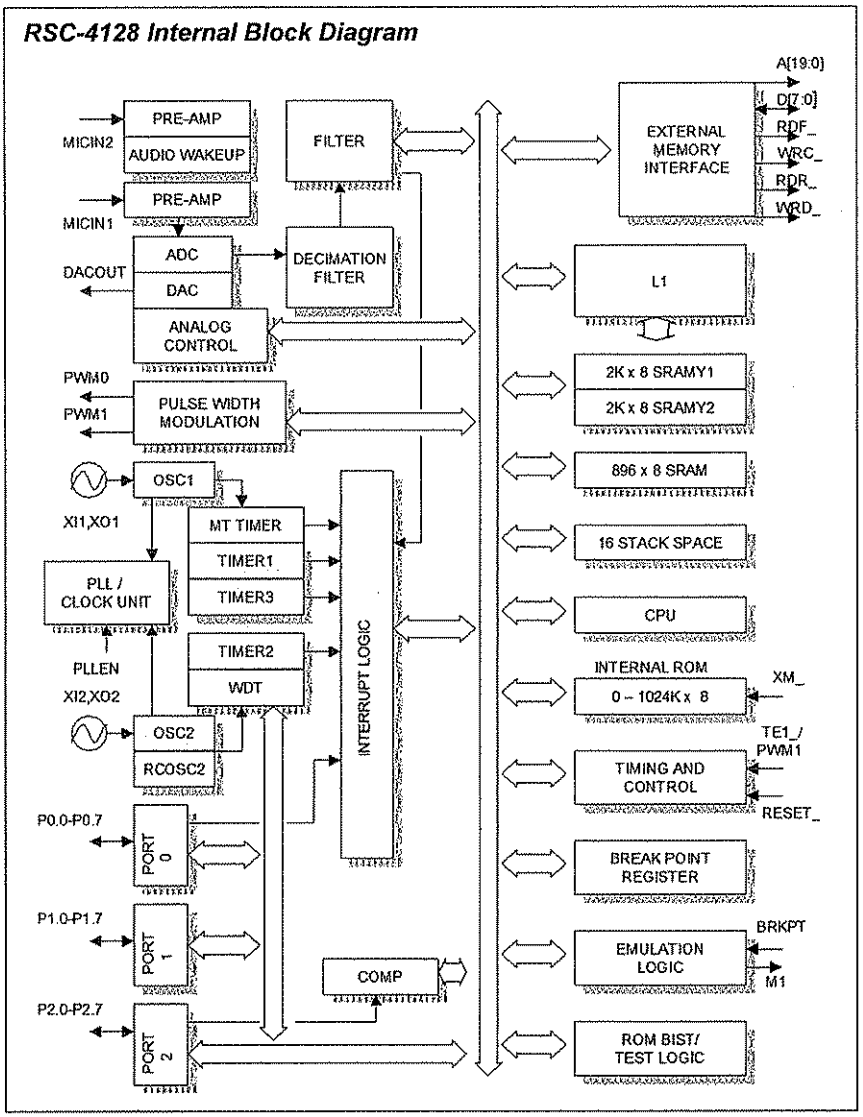
The RSC-4128 has 20-bit address and 8-bit data busses for interfacing with external memory. It includes an -XM input pin capable of enabling or disabling the internal ROM.

NOTE: Neither the -XM input pin nor the extended memory busses are available on 64-lead LQFP packaged versions of the RSC-4128 with internal ROM. These are available on the die and 100 LQFP versions.

Three bi-directional ports provide 24 configurable, general-purpose I/O pins to communicate with or control external devices with a variety of source and sink currents. Up to 4 of these I/O may be used as programmable Analog Comparator inputs. 16 may be used as I/O wakeup.

The RSC-4128 has a high frequency (14.32 MHz) clock as well as a low frequency (32,768 Hz) clock. The processor clock can be selected from either source, with a selectable divider value. The device performs speech recognition when running at 14.32 MHz. The RSC-4128 also supports programmable wait states to allow the use of slower memory.

RSC-4128 Internal Block Diagram



OSC1 is a very low-cost 3.58 MHz crystal oscillator which is used by a 4X PLL to generate the 14.32MHz clock. The OSC2 oscillator provides the options of using an external crystal or its own internal RC devices (no external components required for the internal RC mode).

There are three programmable, general-purpose 8-bit counters / timers – Timers 1 and 3 are derived from OSC1, and Timer2 from OSC2. There is also a Watchdog timer that may be used to exit an undesired condition in program flow, and Multi-tasking timer to allow chip operations to share resources in parallel.

A single chip speech I/O solution may be created with the RSC-4128. An external microphone passes an audio signal to the preamplifier and ADC to convert the incoming speech signal into digital data. Speech features are extracted using the Digital Filter engine. The microcontroller CPU processes these speech features using speech recognition algorithms in firmware, with the help of the "L1" Vector Accelerator and enhanced instruction set. The resulting speech recognition results may be used to control the consumer product application code, or to output speech or audio in the form of a dialog with the user of the consumer product. If desired, the output speech or audio signal from the RSC-4128 is generated by a DAC for external amplification into a speaker, or a PWM capable of directly driving a speaker at typical consumer product volumes. A typical product will require about $0.30 - $1.00 (in high volume) of additional components, in addition to the RSC-4128.

The RSC-4128 also provides a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. A typical general purpose application will require about $0.30 - $0.50 (in high volume) of additional components, in addition to the RSC-4128.

32M Bit (4M x8/2M x16) Dual Bank NOR Flash Memory

FEATURES

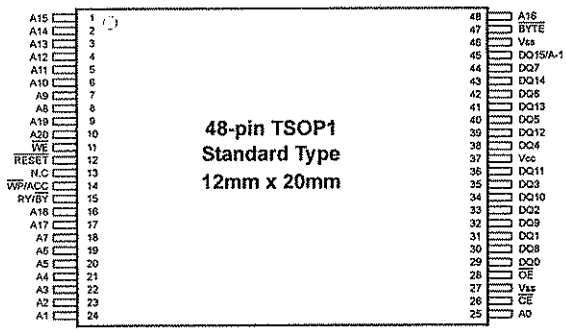
- Single Voltage, 2.7V to 3.6V for Read and Write operations
- Organization
  4,194,304 x 8 bit (Byte mode) / 2,097,152 x 16 bit (Word mode)
- Fast Read Access Time : 70ns
- Read While Program/Erase Operation
- Dual Bank architectures
  Bank 1 / Bank 2 : 8Mb / 24Mb
- Secode(Security Code) Block : Extra 64K Byte block
- Power Consumption (typical value @5MHz)
  - Read Current : 14mA
  - Program/Erase Current : 15mA
  - Read While Program or Read While Erase Current : 25mA
  - Standby Mode/Auto Sleep Mode : 5μA
- $\overline{WP}$/ACC input pin
  - Allows special protection of two outermost boot blocks at V_{IL}, regardless of block protect status
  - Removes special protection of two outermost boot block at V_{IH}, the two blocks return to normal block protect status
  - Program time at V_{HH} : 9μs/word
- Erase Suspend/Resume
- Unlock Bypass Program
- Hardware $\overline{RESET}$ Pin
- Command Register Operation
- Block Group Protection / Unprotection
- Supports Common Flash Memory Interface
- Industrial Temperature : -40°C to 85°C
- Endurance : 100,000 Program/Erase Cycles Minimum
- Data Retention : 10 years
- Package : 48 Pin TSOP1 : 12 x 20 mm / 0.5 mm Pin pitch
  48 Ball TBGA : 6 x 8.5 mm / 0.8 mm Ball pitch

GENERAL DESCRIPTION

The K8D3216U featuring single 3.0V power supply, is a 32Mbit NOR-type Flash Memory organized as 4Mx8 or 2M x16. The memory architecture of the device is designed to divide its memory arrays into 71 blocks to be protected by the block group. This block architecture provides highly flexible erase and program capability. The K8D3216U NOR Flash consists of two banks. This device is capable of reading data from one bank while programming or erasing in the other bank. Access times of 70ns, 80ns and 90ns are available for the device. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in units of 8 bits (Byte) or 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7 sec. The device requires 15mA as program/erase current in the standard and industrial temperature ranges.

The K8D3216U NOR Flash Memory is created by using Samsung's advanced CMOS process technology. This device is available in 48 pin TSOP1 and 48 ball TBGA packages. The device is compatible with EPROM applications to require high-density and cost-effective nonvolatile read/write storage solutions.

PIN CONFIGURATION

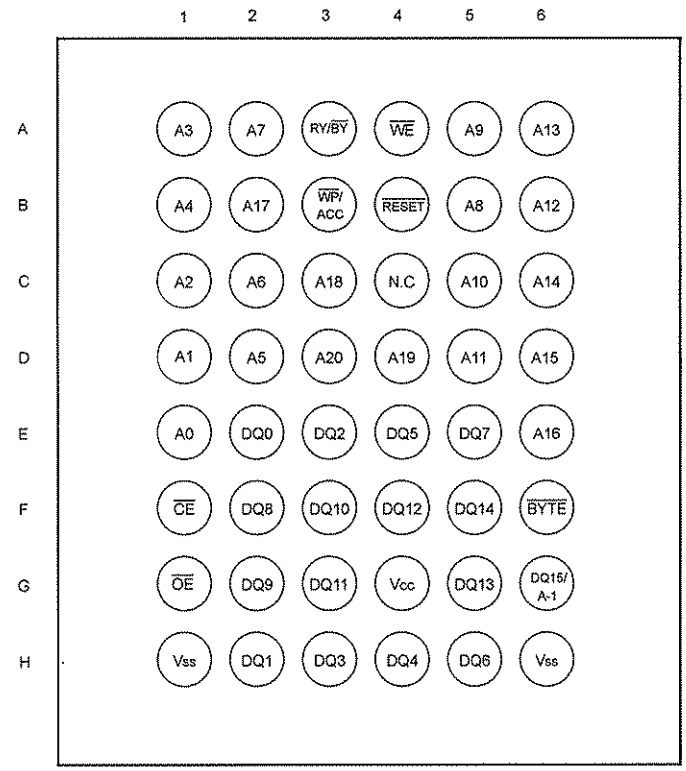


Note :
Please refer to the package dimension.

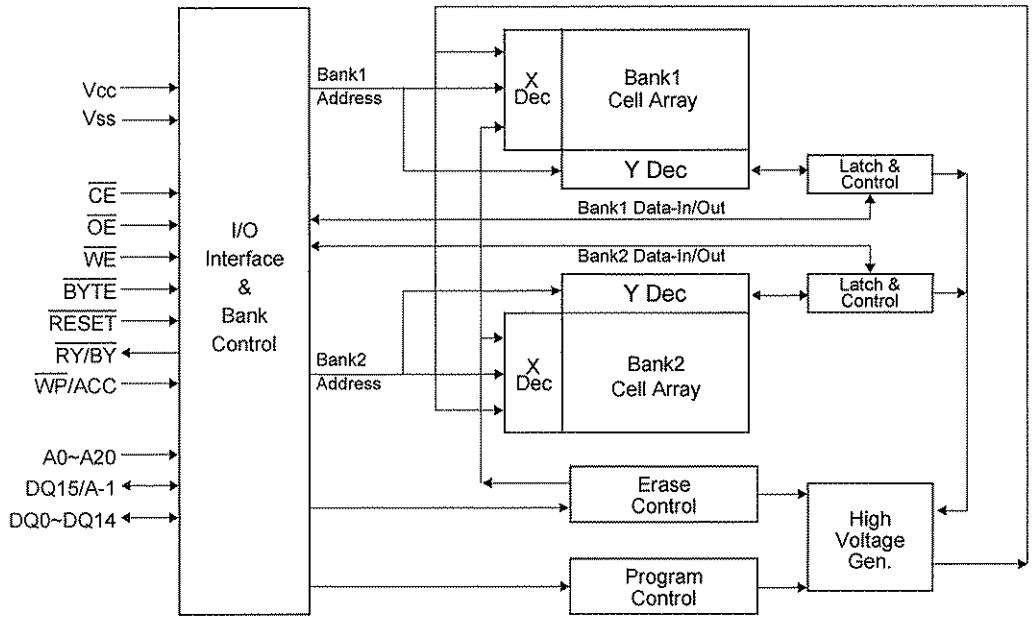
PIN DESCRIPTION

Pin Name	Pin Function
A0 - A20	Address Inputs
DQ0 - DQ14	Data Inputs / Outputs
DQ15/A-1	DQ15 Data Input / Output A-1 LSB Address
$\overline{BYTE}$	Word / Byte Selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
RY/$\overline{BY}$	Ready/Busy Output
$\overline{WE}$	Write Enable
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
Vcc	Power Supply
Vss	Ground
N.C	No Connection

48 Ball TBGA TOP VIEW (BALL DOWN)



FUNCTIONAL BLOCK DIAGRAM



Features

- Low-voltage and Standard-voltage Operation
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 100 kHz (1.8V) and 400 kHz (2.5V, 2.7V, 5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes are Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Automotive Grade, Extended Temperature and Lead-free/Halogen-free Devices Available
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP, 5-lead SOT23, 8-lead TSSOP and 8-ball dBGA2™ Packages

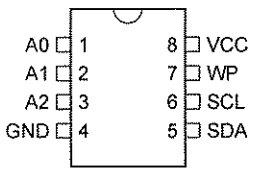
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP, 5-lead SOT23 (AT24C01A/AT24C02/AT24C04), 8-lead TSSOP and 8-ball dBGA2 packages and is accessed via a 2-wire serial interface.

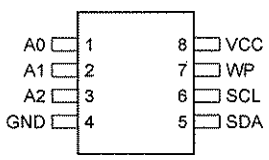
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect
GND	Ground
VCC	Power Supply

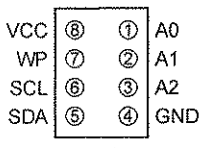
8-lead TSSOP



8-lead SOIC

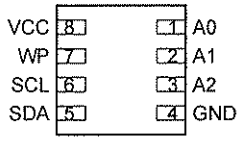


8-ball dBGA2



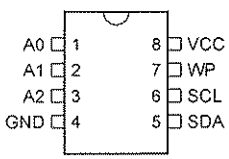
Bottom View

8-lead MAP

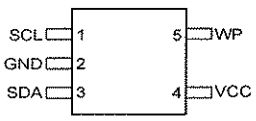


Bottom View

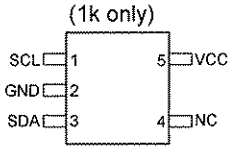
8-lead PDIP



5-lead SOT23



5-lead SOT23 Rotated (R) (1k only)



2-wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08(1)
AT24C16(2)

Note: 1. This device is not recommended for new designs. Please refer to AT24C08A.

2. This device is not recommended for new designs. Please refer to AT24C16A.

0180Q–SEEPR–1/04

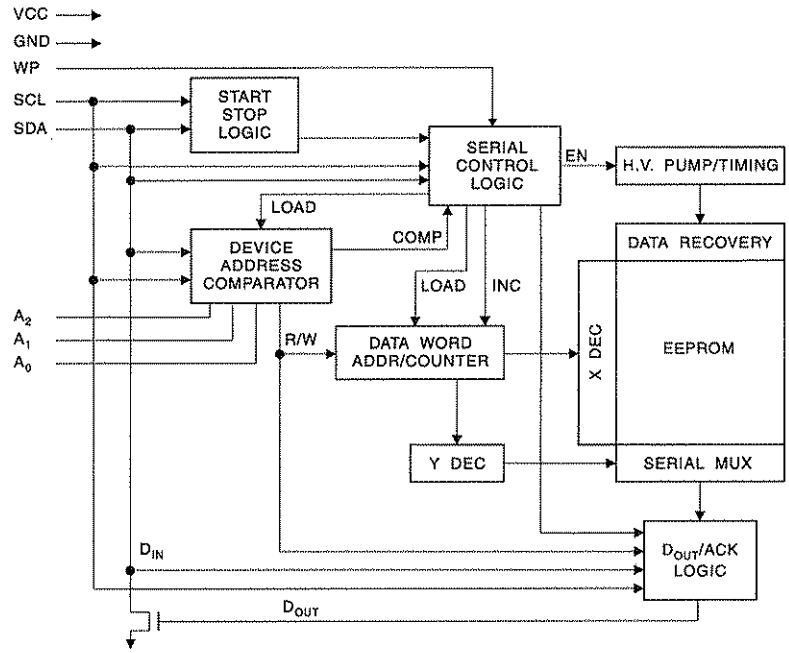
In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

Absolute Maximum Ratings

Operating Temperature	-55° C to +125° C
Storage Temperature	-65° C to +150° C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



FAIRCHILD SEMICONDUCTOR®

September 1983
Revised May 2005

MM74HC373
3-STATE Octal D-Type Latch

General Description

The MM74HC373 high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

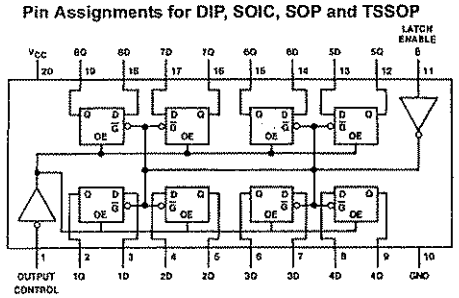
Ordering Code:

Order Number	Package Number	Package Description
MM74HC373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
Q_0 = Level of output before steady-state input conditions were established.
Z = High Impedance

FAIRCHILD SEMICONDUCTOR™

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MM74HC374
3-STATE Octal D-Type Flip-Flop

General Description

The MM74HC374 high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

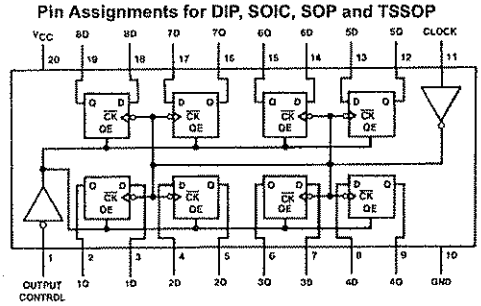
Ordering Code:

Order Number	Package Number	Package Description
MM74HC374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW-to-HIGH
Z = High Impedance State
Q_0 = The level of the output before steady state input conditions were established

