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Operational Description For The AR200

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Amendment List

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1 PRODUCT DESCRIPTION

The Advantra Model AR200 is a Telemetry module. This product is to be compatible with the so-called 2.6 requirements.

The module has two connections. One connection is the antenna port, the other connection is the data port / power supply. The host device will talk to the module over this data port and will instruct to execute some commands. A brief summary of those commands:

- Set the device in radio mode or Modem mode.
- Pass Modem data.
- Configure the Radio.
- Transmit a message.

In all those cases the device can reply. The only case the device can initiate a transaction is when the radio receives a message. This message will immediately be output to the host.

2 FEATURES

Software Updates	No
Software Configuration	GOTAP and via programming interface.
Out of range indicator	Readable with command.
Diagnostics	About menu item displays Serial number, Operator defined string, ReFLEX™ diag numeric values. E.g. BER, sig. strength, frequency. As required by Development.
Password Protection	As defined in GOTAP
Canned responses	No
Miscellaneous responses	No

3 THIS MANUAL COVERS

This manual covers the following:

- **Technical Specification of the product**. At a glance guide to the product specifications in normal and in extreme environment conditions.

- **Detailed technical description of the device**. Full technical description and theory of operation.

4 TECHNICAL SPECIFICATIONS

4.1 Normal Operating Conditions

Temperature	15^0C to 35^0C (+59^0F to + 95^0F)
Ambient Relative Humidity	20 to 75%
Supply Voltage	5V +/- 5%

Free Fall	IEC 68-2-32
Bump	IEC 68-2-29 Test EB

4.2 Extreme Operating Conditions

Temperature	0^0C to +55^0C (+32^0F to +131^0F)
Ambient Relative Humidity	75to 95 % (Non Condensing)

4.3 Electrical Specifications

Supply Min Voltage	4.75V
Supply Nominal Voltage	5V
Supply Max Voltage	5.25V
Frequency Stability 0^0 / +55^0 (+32^0F to +131^0F)	$\pm$ 0.5 ppm
TX Frequency Range	896 to 902 MHz
RX Frequency Range	929 to 932, 935 to 942 MHz
Channel Separation	12.5 kHz
RX Sensitivity	Better than –118 dBm
RX Bit Rate	800, 1600, 3200, 6400
TX Bit Rate	800, 1600, 6400, 9600
TX Peak Frequency Deviation	$\pm$ 2.4 kHz
TX RF Power	32 dBm

5 GENERAL CIRCUIT DESCRIPTION

The Boomerang consists the following circuits: Transceiver circuit, microprocessor and power supply circuit.

5.1 Transceiver circuit

5.1.1 Receiver

Dual conversion Superhetrodyne design with a first IF frequency of 45 MHz and a 450 kHz second IF.

5.1.2 Transmitter

Directly modulated VCO, followed by a buffer amplifier, fet amplifier and power amplifier.

5.1.3 Synthesiser

Phase Lock Loop and Reference Oscillator crystal to control the frequencies of the TX and RX VCO.

5.2 Microprocessor

5.2.1 Microprocessor, Flash memory

The micro-controller is a Mitsubishi M30624FGLGP, which has 256k bytes of Flash program memory and 20k of RAM built in.

5.2.2 Configuration Interface

Provides the servicing centre with serial communications for programming certain functions within the module.

5.2.3 Flash Programming Interface

Provision for Flash programming to enable product software upgrades is located onto the data port.

5.3 Power Supply

The power supply is connected through a connector on the module. The following levels are used throughout the device with their nominal voltage levels:

Signal	Voltage Level
Power	5 VDC +/-5%
+V1	5 VDC +/- 5%
+V2	5 VDC +/- 5%
VDD	3.3 VDC +/- 5%
VCC	5 VDC +/- 5%
VIF	2.5 VDC +/- 7%

6 THEORY OF OPERATION

6.1 Receiver Circuit

6.1.1 RF Output port

The RF output power is available on the SMA connector. A simple PIN diode switch, D5-D6, controls the antenna signal paths between receive and transmit circuits.

6.1.2 Receiver LNA, 1st Mixer

In receive mode, a one-stage Q13 low noise amplifier (LNA) amplifies the inbound ReFLEX™ signal. A SAW filter F1 filters the output of the LNA; this provides image selectivity and protection from interference from out of band signals. After the SAW filter, the inbound ReFLEX™ signal is applied to the 1st mixer, Q16, where it is mixed with the 1st local oscillator to produce a product at the first IF frequency of 45 MHz.

6.1.3 45 MHz Channel Filter, 2nd Mixer

The inbound signal, at the collector of Q16, which is now at 45MHz, is then applied to a crystal channel filter F2, before being applied to the 2nd mixer, IC1. The crystal filter is selected to provide adequate protection to the second mixer from adjacent and adjacent $\pm$ n channel signals. The crystal filter also provides necessary selectivity at the receiver 2nd local oscillator image frequency.

6.1.4 IF amplifier

IC1 is a Fujitsu TA31149FN. This IC incorporates a number of functions including a 1volt linear regulator, 2nd mixer, limiting IF amplifier, quadrate detector, bit rate filter, FSK comparator and RSSI function. The 2nd mixer, converts the inbound 45 MHz signal to a final IF frequency of 450 kHz. This signal is then applied to a ceramic channel filter F5 where most of the receivers adjacent channel filtering is achieved. After filtering, the signal is amplified by a limiting IF amplifier and demodulated.

6.1.5 Demodulation

Is achieved with the quadrate detector within the IF IC which uses an off chip ceramic discriminator, Y2. The demodulated signal is then applied to a bit rate filter and finally a four level FSK comparator, which in turn outputs [RX_MSB] and [RX_LSB] data to the decoder.

6.1.6 AGC

The IF amplifier IC's RSSI function (Received Signal Strength Indicator) is used to provide AGC by controlling the gain of the receiver LNA amplifier. This is used to give the product exceptional high-level intermodulation performance.

6.1.7 AFC

ReFLEX™ specification requires very accurate control of the receiver inbound and transmitter outbound channel frequency. The design requirement is for a frequency accuracy of better than 0.5 ppm. To achieve this, the architecture employs a semi-closed loop AFC routine controlled by software. During the inbound ReFLEX FRAME sync period, the IF demodulator AFC output is read by an A to D converter on the decoder board assembly. This value is then stored. If specific conditions are valid, i.e. frame sync reception error free, a correction value is then applied to the crystal reference oscillator D to A [TD1] in the next receiver FRAME period.

6.2 Synthesiser Circuit

6.2.1 Synthesiser

IC2 is an analogue device ADF4117 phase lock loop (PLL) IC. This is used to synthesise both transmit and receive frequencies. The frequency of the VCO is the inbound ReFLEX channel frequency minus the first IF frequency of 45MHz. The Frequency generation is therefore based around a 900 MHz VCO Q3, The output of the VCO is buffered with Q14.

6.2.2 Reference Oscillator

Q2 and associated crystal Y1 generate the 15.15 MHz reference signal for the synthesiser. The design of the device is a crystal saving design; i.e. the reference oscillator is also used to produce the second local oscillator signal for the receiver 2nd mixer. The third harmonic of the crystal at 45.450MHz is injected into IC1 where it is mixed with the first IF of 45 MHz to produce the final IF frequency of 450 kHz.

6.3 Transmitter Circuit

6.3.1 Transmitter

To generate the ReFLEX outbound channel acknowledgement, the 1st local oscillator output is amplified and then applied to the transmitter power amplifier U8. The outbound channel transmitter power requirement is typically +32dBm. The output power is controlled by U6-D.

Modulation

Of the transmitter is achieved by two point modulation, where modulation is applied to both VCO, D1 and reference oscillator D2 in phase but at different amplitudes. This technique is used to provide a true 4 level FSK signal.

6.4 Power Supplies

6.4.1 Transceiver power supplies

6.4.1.1 VCC

Supplies power to the basic functions of the Transceiver Assembly circuits.

6.4.1.2 +V1

+V1 is the filtered input voltage and supplies the LNA and TX buffer.

6.4.1.3 VDD

VDD is been taken from the 3V REF witch is buffered with U6-A. It supplies the micro.

6.4.1.4 Synthesiser Supplies

The synthesiser is supplied from VCC while the charge pump is charged from +V1.

6.4.2 Reset

6.4.2.1 Reset

R48, R50, R109, R45, R46, R44, R43, R47, U6-B, C6, C62 and C53 hold the RESET line into the micro-controller (IC402) low for a period after VDD has been established. When the software for what reason crash no watchdog signal is applied to Q11 and the circuit provides a reset to the micro.

A voltage comparator made with Q4 gives the micro a signal when the input supply voltage is outside the range. This ensures the micro-controller is put into a defined state if its supply voltage falls outside the guaranteed operating range.

7 MICROCONTROLLER

The micro-controller (U1) is a Mitsubishi M30624FGLGP, which has 256k bytes of Flash program memory and 20k of RAM built in.

7.1 Micro-controller properties

7.1.1 Supplies

The micro-controller runs from the VDD supply via Q10.

7.1.2 Clocks

Two oscillator circuits control the micro-controller operation: a 38.4kHz watch crystal and a 9.22MHz (nom) resonator circuit.

Note: Always ensure that account is made of the capacitive loading effect of oscilloscope probes when measuring clock frequencies of the micro-controller.
X10 probes are recommended.

Y4 forms the oscillator. Under normal operation, (when the product is not in Factory test mode) the oscillator is switched on and off by the micro-controller as required.

The crystal oscillator; Y5, R40 C55 and C54 is enabled by software shortly after a reset and remains turned on for as long as the device is powered.

7.1.3 DACs

There are two internal 8-bit Digital to Analogue converters DA0 (signal TD0) and DA1 (Signal TD1), which are used for modulation and fine frequency control of the transceiver. DA0 controls the VCO and DA1 controls the reference oscillator.

Lines D8, D9, D10, P13, and P14 driving resistors R41, R59, R60, R61, R62 and R63 form a discrete 4 bit Digital to Analogue converter that is used to control the ramp up and down of the output power from the power amplifier (PA) at the beginning and end of a transmission.

7.1.4 ADCs

The micro-controller has eight Analogue-to-Digital inputs, three of which are used to monitor signals within the product.

Name / Pin	Monitored signal
AN1 / Pin 93	A voltage representing the temperature
AN2 / Pin 92	AFC / AFC control voltage from the transceiver board
AN0 / Pin 95	Receive Signal Strength from transceiver board

7.2 FLASH Programming Port

The program memory within the micro-controller can be accessed and changed via the same connection as the data port.

7.2.1 Flash Programming Interface

These connections are accessible through the data port. External resistors pull pin 44 and pin 39 on the micro-controller high and low respectively to the force the micro into programming mode when F_CNVSS is pulled high. This is a hardware function within the chip.

7.2.1.1 Flash Programming Pins

Conn. Pin	Signal	Function
4,10	GND	Ground
14	CNVSS	Programming Mode control
15	VDD	Supply
13	/MR (RESET)	Programmer control of micro-controller reset
2	TXD1	Serial programming data FROM micro-controller
1	RXD1	Serial programming data TO micro-controller
16	P65 (SCLK)	Serial clock to micro-controller
8	CTS (BUSY)	Busy indication FROM micro-controller

7.2.2 Serial Data FLASH

All configuration settings for the device are stored in a 26kbit serial data flash U3 (AT24C16).
U3 is run from the VDD supply.

7.2.2.1 Interface

U3 has a 3 wire serial interface (SDA, SCL, WP), which is connected, directly to one of the serial ports on the micro-controller.

Signal	Function
SCL	Serial Clock.
SDA	Serial data FROM and TO the serial data flash.
WP	When held low by the micro' data cannot be written to the serial data flash.

7.2.3 Serial Communications

A serial communication port is provided for programming configuration data and testing modules in the factory. The interface is connected to an asynchronous serial port on the micro-controller.

7.3 Led Alert

A led alert is available on pin 12 of the connector. This pin is connected to pin 20 of the micro-controller, which can turn the led into four modes. The led on, off, slow blinking and fast blinking.

8 ALIGNMENT

During the alignment process, the product stores alignment and calibration variables in data Flash. These variables are unique to the transceiver / decoder assembly and prohibit the replacement of individual board assemblies. Therefore alignment can only be carried out at the place of manufacture.

9 APPENDICES

9.1 Pin Connections

12nc for the PCB A100 000 07000
Package marking none

Pin	Connection name
1	RX1
2	TX1
3	POWER
4	GND
5	RX0
6	TX0
7	RTS
8	CTS
9	POWER
10	GND
11	WDD
12	LED
13	/MR
14	CNVSS
15	VDD
16	P65