3.2 Transceiver Description

An electronically tuned small loop antenna is used for both receiver and transmitter functions. Switching of the antenna between receive and transmit is done automatically when the transmitter power supply is enabled. The switching circuit is designed in such ways so that no bias current is required during receive. Because the ReFLEX outbound channels are 35MHz lower than the inbound receive channels, the antenna is arranged in such a way as to be electronically tuned to the lower outbound channels during the transmit mode of the product.

The receiver is a double superhetrodyne design with a first IF frequency of 45 MHz and a second IF frequency of 450 kHz. Frequency generation is based around a synthesised 450 MHz VCO which is multiplied, then buffered to produce the 1st local oscillator. The design is a crystal saving design; i.e. the crystal reference oscillator for the synthesiser is also used to produce the second local oscillator signal for the receiver 2nd mixer. The frequency of the VCO is the product of 1/2 * (the inbound ReFLEX channel frequency minus the first IF frequency). Operating the VCO at a fraction of the final frequency is done for two reasons, the cost and technical risks associated with screening are reduced, and lower frequency synthesisers are generally more efficient which is an important consideration for battery operated portable equipment.

In receive mode, a two-stage low noise amplifier (LNA) amplifies the inbound ReFLEX signal. The output of the LNA is then filtered by a SAW filter, which provides image selectivity and protection from interference from out of band signals. After the SAW filter the inbound ReFLEX signal is applied to the 1st mixer, where it is mixed with the 1st local oscillator to produce a product at the first IF frequency of 45 MHz. The inbound signal, which is now at 45MHz, is then applied to a crystal channel filter before being applied to the 2nd mixer. The crystal filter is selected to provide adequate protection to the second mixer from adjacent and adjacent + n channels signals, such as encountered in high intermodulation areas. The crystal filter also provides necessary selectivity at the receiver 2nd local oscillator image frequency.

The IF amplifier IC is a Samsung KA8515. This IC incorporates a number of functions including a 1 volt linear regulator, 2nd mixer, limiting IF amplifier, quadrature detector, bit rate filter, FSK comparitor and RSSI function. The 2nd mixer, converts the inbound 45 MHz signal to a final IF frequency of 450 kHz. This signal is then applied to a ceramic channel filter where most of the receivers adjacent channel filtering is achieved. After filtering the signal is amplified by a limiting IF amplifier and demodulated.

Demodulation is achieved with the quadrature detector which uses an off chip ceramic discriminator. The demodulated signal is then applied to a bit rate filter and finally a four level FSK comparitor, which in turn outputs [MSB] and [LSB] data to the decoder.

ReFLEX specification requires very accurate control of the receiver inbound and transmitter outbound channel frequency. The design requirement is for a frequency accuracy of better than 0.5 ppm. To achieve this, the architecture employs a semi-closed loop AFC routine controlled by software. During the inbound ReFLEX FRAME sync period, the IF demodulator AFC output is read by an A to D converter on the decoder board assembly. This value is then stored and used to compare against a calibrated 450 kHz IF signal which is internally generated within the product. The calibration [TEST] routine is carried out at the end of every nth receive FRAME. ('n' is programmable via op-comms). The error correction value is then applied to the crystal reference oscillator D to A [TD1] in the next receiver FRAME period.

To generate the ReFLEX outbound channel acknowledgement, the 1st local oscillator output is switched to a transmitter buffer amplifier where it is amplified and then applied to the transmitter power amplifier. The outbound channel transmitter power requirement is typically +30dBm. To achieve this power level from a single cell battery, the transmitter takes its energy from a 4.7 Farad capacitor, this is charged to a nominal 2.5 volts via a DC/DC converter on the decoder assembly.

Modulation of the transmitter is achieved by two point modulation, where modulation is applied to both VCO and reference oscillator in phase but at different amplitudes. This technique is used to provide a true FSK signal, which has a DC component.

4.19 Antenna Transmit / Receive switch

Frequency	884 – 942 MHz
Insertion loss, receive	<0.5dB
Isolation, transmit	>15dB
Insertion loss, transmit	<0.5dB
Isolation, receive	>15dB
Zin (Source from VCO)	50 Ohm
Zout (receive mode)	50 Ohm
Zout (transmit mode)	50 Ohm
Supply	VDIG
Current, receive mode	<100uA
Current, transmit mode	<100uA
Current idle mode	0uA
Inputs:	-TXE (inverse TXE)

4.20 Antenna

Resonant Frequency (RX)	Adjustable, 929-942MHz
Resonant Frequency (TX)	893MHz nom. (frequency adjusted via pin switch).
VSWR receive mode	<1.5:1
VSWR Transmit. Mode	<1.5:1
Loaded Q	35 typ.
Control Inputs	TX_PSU @ 4mA
Efficiency, compared to ref. dipole	TBA

5. RF/DECODER INTERFACE

5.1 IFE

Functions:
Receiver 1 volt power supply enable. Port = input, Z in = 50k.
AFC op-amp supply (10uA typ.)
Synthesiser charge pump and pre-scaler supply reference.

5.2 S_DAT

Synthesiser programming data. Port = input, Z in = CMOS

5.3 S_CLK

Synthesiser programming clock. Port = input, Z in = CMOS

5.4 S_EN

Synthesiser programming enable. Port = input, Z in = CMOS

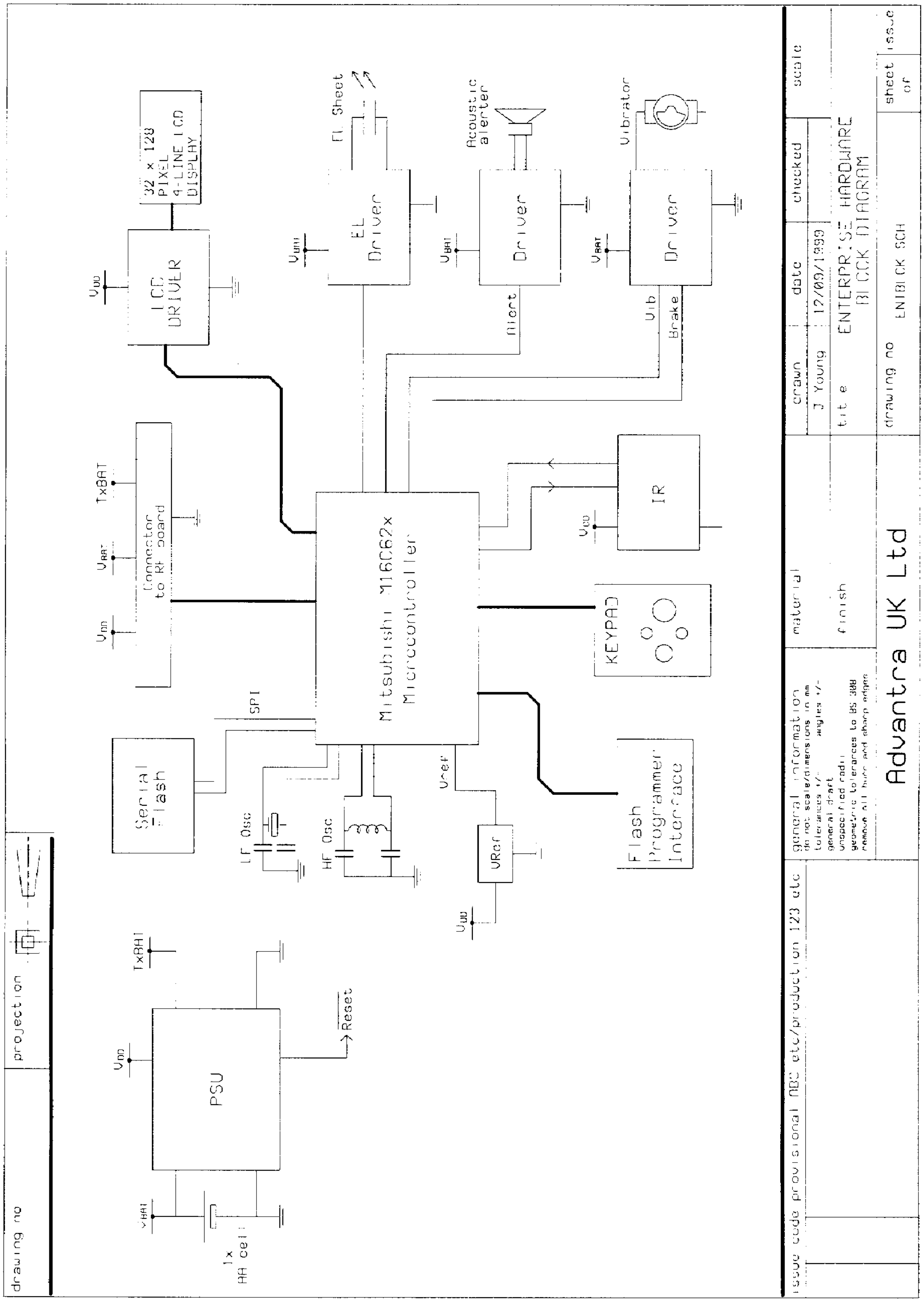
5.5 FLC

Synthesiser fast lock. Port = schmit trigger input, active high. Z in = CMOS

5.6 BFC

Bit rate filter select. Port = input. Z in = CMOS. Active state:

0 = High Bit Rate
1 = Low Bit Rate


32 x 128
PIXEL
4-LINE LCD
DISPLAY
LCD
DRIVER
EL Sheet
EL
Driver
Acoustic
alerter
Driver
Vibrator
Driver
Alert
Vib
Brake
Connector
to RF board
TxBAT
Mitsubishi M16C62x
Microcontroller
IR
KEYPAD
SPI
Serial
Flash
LF Osc
HF Osc
Vref
VRef
Flash
Programmer
Interface
PSU
Reset
1x
AA cell
drawing no
projection
issue code provisional ABC etc/production 123 etc
general information
material
finish
drawn
J Young
date
12/09/1999
checked
scale
title
ENTERPRISE HARDWARE
BLOCK DIAGRAM
drawing no
ENTBLCK SCH
sheet
of
issue
Advantra UK Ltd