FCC ID: O2DFUNRISE-61T

Technical Description :

The brief circuit description is listed as follows :
- U1 ET13X221, Y1, D2 and associated circuit act as VCO and PLL.
- Q2 and associated circuit act as High Frequency Amplifier.
- U3 ATS308T and associated circuit act as Encoder.
- Q1, D1 and associated circuit act as Voltage Regulator.
- SW2 and associated circuit act as Frequency Band Selector.

Antenna Used :

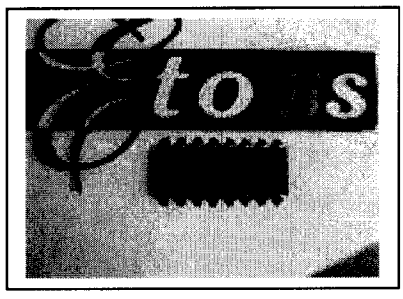
An extendable antenna has been used.

Descriptions

The ET13X221 single-chip solution is an integrated circuit intended for use as a low cost FSK transmitter to establish a frequency-agile RF link. The device is designed to provide 10-channel transmitter. The chip is intended for linear (FM) or digital (FSK) modulated applications in the wireless Mouse and Keyboard. The single chip transmitter operates down to 2.2 V and is expressly designed for low power consumption. The synthesizer has a typical channel spacing of approximately 30KHz to allow narrow-band applications.

Feature

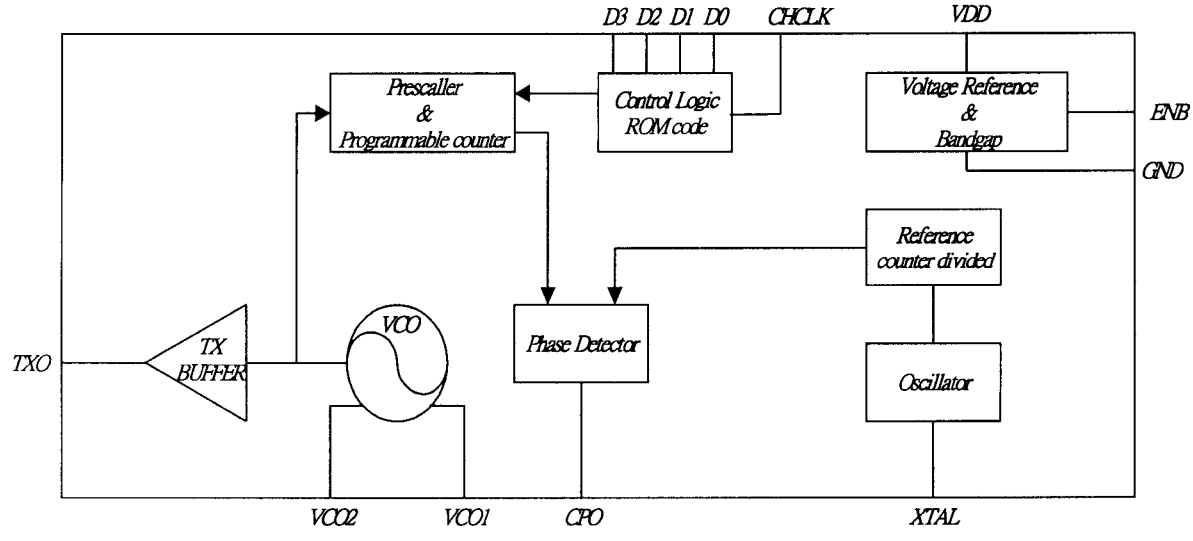
Single-Chip RF Transmitter
Include oscillation circuit with external X-TAL.
On-Chip Phase-Locked Loop (PLL)
Power Down mode
2.2 to 3.6V supply range



Application

Wireless Mouse
Wireless Keyboard
Wireless Communication Products

Block Diagram



Function Description

The ET13X221 single-chip solution is a CMOS technology integrated circuit intended for use as a low cost FSK transmitter to establish a frequency-agile RF link. The device is designed to provide 10-channel transmitter.

VCO

The circuit employed LC-tank structure to achieve low-phase noise characteristic where L is an off-chip high-Q inductor and C is provided by a varactor with different tuning ranges and converting baseband data.

PLL

The PLL includes 64/65 prescaler, charge pump, PFD, N、A swallow counters, R-counter for the multi-channel applications. The channels selected via mechanical switches of parallel BCD input or provided here can be easily set by an input pin CHCLK which directly selects the addresses of the ROM table.

D0 – D3/CHCLK

These input provide the BCD code for selecting the one of ten channels to be locked in both transmit and receive loop. When address data other than 1 – 10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to CHCLK connect to ground and D0 – D3 are shown in Table A. The D0 – D3 inputs have internal pull up devices.

Table A – VCO FREQUENCY AND DIVID RATIO
Oscillator Frequency 4.0MHz, Ref. Divider 800

Channel	VCO Frequency	TXO Frequency	Tx Divider (5.0KHz Ref)	Input D3	D2	D1	D0
1	26.985MHz	26.985MHz	5397	0	0	0	1
2	27.015 MHz	27.015 MHz	5403	0	0	1	0
3	27.045 MHz	27.045 MHz	5409	0	0	1	1
4	27.075MHz	27.075MHz	5415	0	1	0	0
5	27.105 MHz	27.105 MHz	5421	0	1	0	1
6	27.135 MHz	27.135 MHz	5427	0	1	1	0
7	27.165 MHz	27.165 MHz	5433	0	1	1	1
8	27.195 MHz	27.195 MHz	5439	1	0	0	0
9	27.225MHz	27.225MHz	5445	1	0	0	1
10	27.255MHz	27.255MHz	5451	1	0	1	0
	27.255MHz	27.255MHz	5451	1	0	1	1
	27.255MHz	27.255MHz	5451	1	1	0	0
	27.255MHz	27.255MHz	5451	1	1	0	1
	27.255MHz	27.255MHz	5451	1	1	1	0

1: open
0: ground

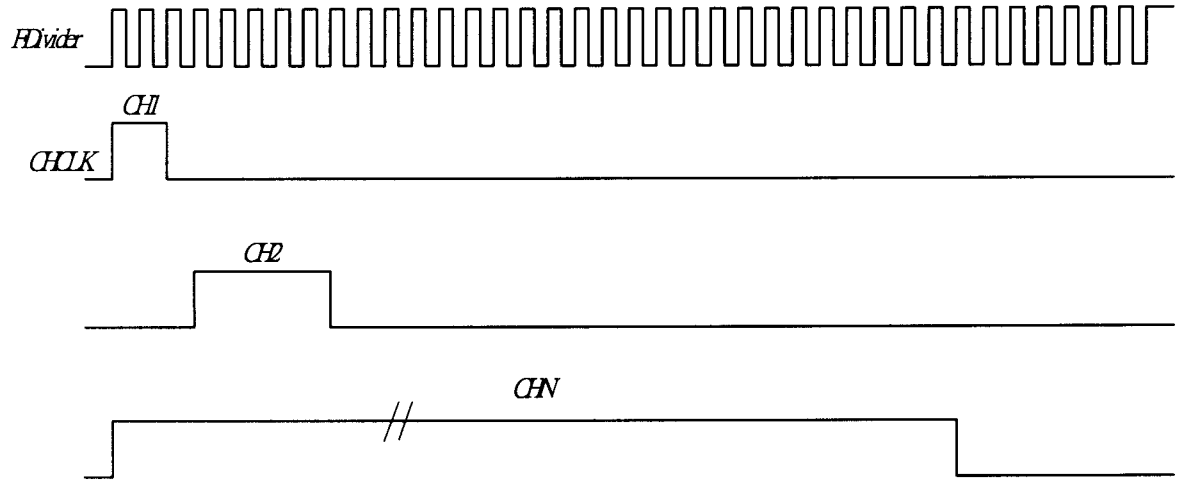
When all parallel BCD input are left open or connect to ground, the channel set by rising edge of clock at Pin 1 CHCLK with MCU. The initial channel when power on (internal power on reset) set to channel 10.

TX output driver

The TX output driver includes a pre-driver and an open-drain output stage. The off-chip loading network can be a parallel RLC tuned resonant circuit which deliveres maximum 0dBm output to the load at 3V supply.

Timing Diagram

Channel DATA by $F_{DIVIDER}$ Clock



Channel clock timing : The channel clock tolerance of the CHCLK signal shall be within ± 150μS.

Channel	CHCLK	Channel	CHCLK
1	600μS	6	3.6mS
2	1.2mS	7	4.2mS
3	1.8mS	8	4.8mS
4	2.4mS	9	5.4mS
5	3.0mS	10	6.0mS