InterAir™ Wireless

INSTALLATION MANUAL

ABOUT THIS MANUAL

This section discusses the objective, audience, and contents of this Installation Manual.

OBJECTIVE

This manual explains how to install, maintain and troubleshoot InterAir™ Wireless network access server equipment at subscriber sites.

AUDIENCE

This manual is designed for the person responsible for installing and maintaining the InterAir™ Wireless network. It includes procedures that should be performed only by trained and qualified personnel.

FCC INFORMATION

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.
NOTE: *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*
Warning: Changes or modifications not expressly approved by InterAir™ Wireless could void the user's authority to operate the equipment.

CONTENTS

Chapter 1 INTRODUCTION describes the equipment, features and specifications of the InterAir™ Wireless network.

Chapter 2 INSTALLATION PLANNING describes safety recommendations, site requirements, required tools and equipment, and includes an installation checklist.

Chapter 3 INSTALLATION PROCEDURES provides procedures for installing network equipment, including the antenna and outdoor unit (ODU), the indoor unit (IDU), power supply and wiring connections. It also provides instructions for system startup and configuration, and troubleshooting the installation.

Chapter 4 MAINTENANCE provides instructions for operating and maintaining the InterAir™ Wireless network. It includes remove/replace procedures and parts lists.

Chapter 5 TROUBLESHOOTING describes troubleshooting network operation, including interpretation of IDU front panel LEDs, and correcting problems detected by the network manager.

Appendix A

DIGITAL, FAST ACQUISITION, SPREAD SPECTRUM BURST PROCESSOR

STEL-2000A+45 (45 MHz)

STEL-2000A+20 (20 MHz)

ASIC
Custom
Products
Division

STANFORD
TELECOM®

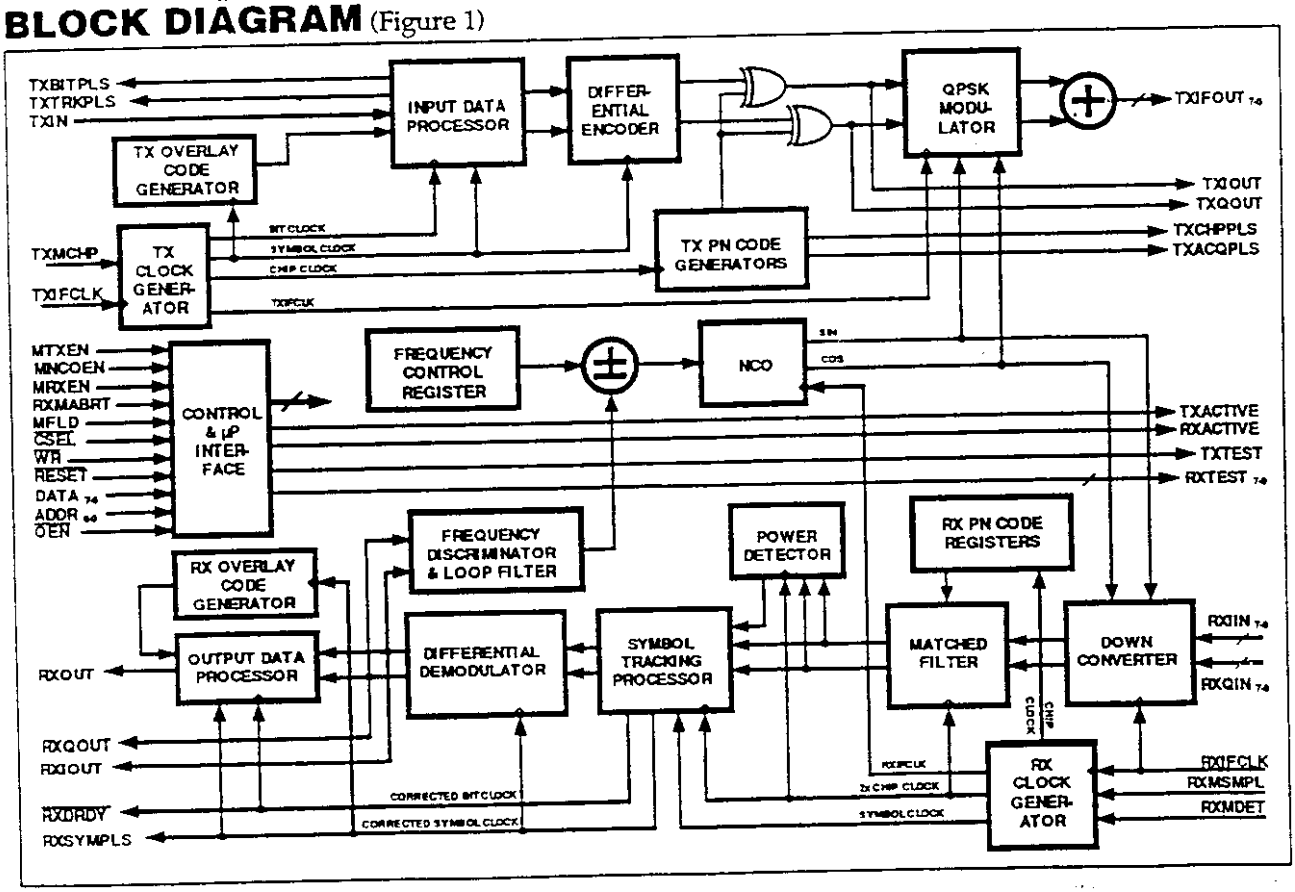
FEATURES

- Complete direct sequence spread spectrum burst transceiver in a single CMOS I.C.
- Programmable functionality supports many different operational modes
- Supports PN chip rate of over 11 Mchips/sec. in transmit and receive modes (STEL-2000A+45 only)
- Acquires within one symbol duration using digital PN Matched Filter
- Two independent PN sequences, each up to 64 chips long, for distinct processing of the acquisition/preamble symbol and subsequent data symbols
- Power management features
- Optional spectral whitening code generation
- Full or half duplex operation
- 100-Pin PQFP packaging

BENEFITS

- High performance and high reliability with reduced manufacturing costs
- Ideal for a wide range of wireless applications including data acquisition systems, transaction systems and wireless Local Area Networks (WLANs)
- Supports data rates up to 2.048 Mbps in compliance with FCC regulations (STEL-2000A+45 only)
- Fast response and very low overhead when operating in burst modes
- Allows high processing gain to maximize the acquisition probability, then reduced code length for increased data rate
- Low power consumption
- Randomizes data to meet regulatory requirements
- Permits dual frequency (Frequency Division Duplex) or single frequency (Time Division Duplex) operation
- Small footprint, surface mount

BLOCK DIAGRAM (Figure 1)



GENERAL DESCRIPTION

The STEL-2000A is a programmable single-chip spread spectrum transceiver. The device performs all the digital processing required to implement a fast acquisition direct sequence (i.e., pseudonoise- or PN-modulated) spread spectrum full- or half-duplex system using differentially encoded BPSK, QPSK, or $\pi/4$ QPSK. A block diagram of the STEL-2000A is shown in Figure 1, while the package style and pin configuration are shown in Figure 2. The STEL-2000A is available in two speed grades; the STEL-2000A+20 (20 MHz maximum clock frequency), and the STEL-2000A+45 (45.056 MHz maximum clock frequency). The 45 MHz version features a high thermal conductivity package for superior heat dissipation, allowing the device to operate continuously at this speed.

The STEL-2000A integrates the capabilities of a digital downconverter, PN matched filter, and DPSK demodulator into a single receiver, where the receiver input is the analog-to-digital converted I.F. signal. STEL-2000A transmit functions include a differential BPSK/QPSK encoder, PN modulator (spreader), and BPSK/QPSK modulator, where the transmitter output is a sampled digitally modulated signal ready for external digital-to-analog conversion (or, if preferred, the spread baseband signal may be output to an external modulator). These transceiver functions have been designed and integrated for the transmission and reception of bursts of spread data. In particular, the PN Matched Filter has two distinct PN coefficient registers (rather than a single one) in order to speed and improve signal acquisition performance. The STEL-2000A is thus optimized to provide reliable, high-speed wireless data communications.

The STEL-2000A operates with symbol-synchronous PN modulation in both transmit and receive modes. Symbol-synchronous PN modulation refers to operation where the PN code is aligned with the symbol transitions and repeats once per symbol. By synchronizing a full PN code cycle over a symbol duration, acquisition of the PN code at the receiver simultaneously provides symbol synchronization, thereby significantly improving overall acquisition time.

The receiver clock rate (RXIFCLK frequency) must be at least four times the receive PN spreading rate and is limited to a maximum speed of 45.056 MHz (STEL-2000A+45 only, 20 MHz in the STEL-2000A+20). As a result, the maximum supported PN chip rate is 11.264 Mchips/second (5 Mcps in the STEL-2000A+20), where a "chip" is a single "bit" of the PN code. Since PN modulation is symbol-synchronous in the STEL-2000A, the data rate is defined by the PN chip rate and length of the PN code; i.e., by the number of chips per symbol. When operating with BPSK modulation, the maximum data rate for a PN code of length N is 11.264/N Mbps (STEL-2000A+45 only, 5/N Mbps in the STEL-2000A+20). When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the maximum data rate for a PN code of length N is 22.528/N Mbps (STEL-2000A+45 only, 10/N Mbps in the STEL-2000A+20). Conversely, for a given data rate Rb, the length N of the PN code employed must be such that the product of N x Rb is less than 11.264 (for BPSK) or 22.528 (for QPSK) Mcps (STEL-2000A+45 only).

The data rate (Rb) and the PN code length (N), however, cannot generally be arbitrarily chosen. United States FCC Part 15.247 regulations require a minimum processing gain of 10 dB for unlicensed operation in the Industrial, Scientific, and Medical (ISM) bands, implying that the value of N must be at least 10. To implement such a short code, a Barker code of length 11 would typically be used in order to obtain desirable auto- and cross-correlation properties. With the STEL-2000A, a PN code length of 11 implies that the maximum data rate supported by the STEL-2000A in compliance with FCC regulations is 2.048 Mbps using differential QPSK (STEL-2000A+45 only). The STEL-2000A further includes transmit and receive code overlay generators to insure that signals spread with such a short PN code length possess the spectral properties required by FCC regulations.

The STEL-2000A receiver circuitry employs an NCO and complex multiplier referenced to RXIFCLK to perform frequency downconversion, where the input I.F. sampling rate and the clock rate of RXIFCLK must be identical. In "complex input" or Quadrature Sampling Mode, external dual analog-to-digital converters (ADCs) sample quadrature I.F. signals so that the STEL-2000A can perform true full single sideband downconversion directly from I.F. to baseband. At PN chip rates less than one-eighth the value of RXIFCLK, downconversion may also be effected using a single ADC in "real input" or Direct I.F. Sampling Mode, as discussed in Appendix I.

The input I.F. frequency is not limited by the capabilities of the STEL-2000A. To avoid destructive aliasing, the NCO should not be programmed above 50% of the I.F. sampling rate (the frequency of RXIFCLK);

moreover, the signal bandwidth, NCO frequency, and I.F. sampling rate are all interrelated, as discussed in Appendix I. Higher I.F. frequencies, however, can be supported by programming the NCO to operate on in-band aliases as generated by the sampling process. For example, a spread signal presented to the STEL-2000A's receiver ADCs at an I.F. frequency of $f_{I.F.}$, where $f_{RXIFCLK} < f_{I.F.} < 2 \times f_{RXIFCLK}$, can generally, as allowed by the signal's bandwidth, be supported by programming the STEL-2000A's NCO to a frequency of ($f_{I.F.} - f_{RXIFCLK}$), as discussed in Appendix I of this product specification. The maximum I.F. frequency is then limited by the track-and-hold capabilities of the ADC(s) selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost as well as the performance can typically be improved by using an I.F. frequency of 30 MHz or lower. Down-conversion to baseband is then accomplished digitally by the STEL-2000A, with a programmable loop filter provided to establish a frequency tracking loop

The STEL-2000A is designed to operate in either burst or continuous mode: in burst mode, built-in symbol counters allow bursts of up to 65,533 symbols to be automatically transmitted or received, while, in continuous mode, the data is simply treated as a burst of infinite length. The STEL-2000A's use of a digital PN Matched Filter for code detection and despreading permits signal and symbol timing acquisition in just one symbol. The fast acquisition properties of this design are exploited by preceding each data burst with a single Acquisition/Preamble symbol, allowing different PN codes (at the same PN chip rate) to independently spread the Acquisition/Preamble and data symbols. In this way, a long PN code with high processing gain can be used for the Acquisition/Preamble symbol to maximize the probability of burst detection, and a shorter PN code can be used thereafter to permit a higher data rate.

To improve performance in the presence of high noise and interference levels, the STEL-2000A receiver's symbol timing recovery circuit incorporates a "flywheel circuit" to maximize the probability of correct symbol timing. This circuit will insert a symbol clock pulse if the correlation peak obtained by the PN Matched Filter fails to exceed the programmed detect threshold at the expected time during a given symbol. During each burst, a missed detect counter tallies each such event to monitor performance and allow a burst to be aborted in the presence of abnormally high interference. A timing gate circuit further minimizes the probability of false correlation peak detection and consequent false symbol clock generation due to noise or interference.

To minimize power consumption, individual sections of the device can be turned off when not in use. For example, the receiver circuitry can be turned off during transmission and, conversely, the transmitter circuitry can be turned off during reception when the STEL-2000A is operating in a half-duplex/time division duplex (TDD) system. If the NCO is not being used as the BPSK/QPSK modulator (i.e., if an external modulator is being used), the NCO can also be turned off during transmission to conserve still more power.

The fast acquisition characteristics of the STEL-2000A make it ideal for use in applications where bursts are transmitted relatively infrequently. In such cases, the device can be controlled so that it is in full "sleep" mode with all receiver, transmitter, and NCO functions turned off over the majority of the burst cycle, thereby significantly reducing the aggregate power consumption. Since the multiply operations of the PN Matched Filter consume a major part of the overall power required during receiver operation, two independent power-saving techniques are also built into the PN Matched Filter to reduce consumption during operation by a significant factor for both short and long PN spreading codes.

The above features make the STEL-2000A an extremely versatile and useful device for spread spectrum data communications. Operating at its highest rates, the STEL-2000A is suitable for use in wireless Local Area Network implementations, while its programmability allows it to be used in a variety of data acquisition, telemetry, and transaction system applications.

Appendix B

PRODUCT BRIEF

AHA4012

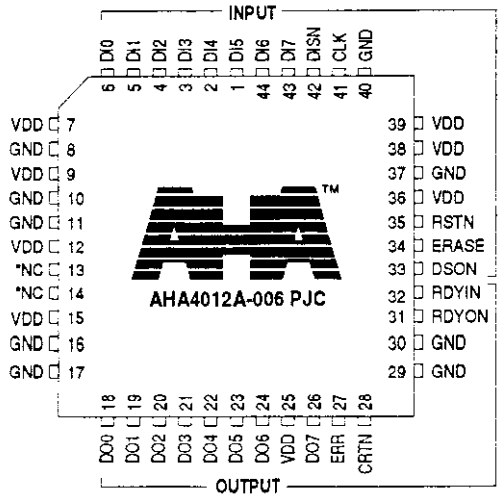
1.5 MBYTES/SEC REED-SOLOMON ERROR CORRECTION DEVICE

The Advanced Hardware Architectures' AHA4012 is the lowest cost member of the AHA PerFEC™ single-chip Reed-Solomon Forward Error Correction (FEC) devices. A single-phase clock synchronizes all chip functions. CMOS technology and custom design techniques help achieve the density needed for a low cost solution. The AHA4012 implements a standard polynomial approved by organizations such as Intelsat.

The device supports several programmable parameters including block size, error threshold, number of check bytes and mode of operation. The device is pin and program compatible with its high performance counterpart, AHA4011. Input and output rate flexibility, low processing latency and various programmable parameters make this an ideal part for many systems requiring Forward Error Correction.

APPLICATIONS

- ISDN/T1.E1/T2.E2/OC1
- Satellite communications/VSAT/INTELSAT
- Global Positioning Systems
- Local/Wide Area Networks



*NC = No connect, reserved for future considerations.

FEATURES

PERFORMANCE:

- Complies to Intelsat IESS-308, Revision 6B; RTCA DO-217 Appendix F, Revision D and proposed ITU-TS SG-18 (formerly CCITT SG-18) Standards
- 6 MBytes/sec burst transfer rate with a 6 MHz clock for all block lengths
- Maximum data transfer rates of 1.5 MBytes/sec continuous for block lengths from 54 bytes through 255 bytes using a 6 MHz clock
- Processing latency time less than 101 µsec in continuous mode for a block length of 100 bytes

FLEXIBILITY:

- Programmable to correct from 1 to 10 error bytes or 20 erasure bytes per block
- Block lengths programmable from 3 to 255 bytes
- Encode, decode or pass-through capability "in-line" with data flow
- Continuous or burst mode operation
- Programmable error threshold to help determine channel performance

SYSTEM INTERFACE:

- Input data pins used for programmable parameters
- Dedicated control pins permit discontinuities in system data flow

OTHERS:

- 44 pin PLCC; 50 mil lead pitch
- Pin and program compatible with the higher performance AHA4011
- Software emulation of the algorithm available

Request the AHA4012 Product Specification for complete details.

Advanced Hardware Architectures

FUNCTIONAL DESCRIPTION

This single-chip CMOS device can be used to encode, decode or pass-through multiple blocks "in-line" with data flow.

The device is first initialized for various programmable parameters including: erasure multiplier, error threshold, number of check bytes, number of message bytes per block, block length and a control byte. Programming is done through the input data bus DI[7:0]. This control byte defines the format of the output data, including, parity information, normal or pass-through operations and conditions for "uncorrectable" block. Following a six-byte initialization, the device may be used to encode, decode or pass-through multiple blocks of data. The device requires reinitialization only when the parameters are changed.

As an encoder, the device clocks input data block followed by "dummy" check bytes designated as "erasures" on the DI bus. ECC core replaces the "dummy" check bytes with corrected check bytes and feeds the block into the Output Buffer for transfer out of the output bus, DO.

As a decoder, the device clocks the user data and check bytes into the Input Buffer. The ECC core performs the necessary corrections and feeds the block to the Output Buffer.

In pass-through mode, the device clocks user data and "dummy" check bytes into the Input Buffer. The ECC core processes the block and transfers the uncorrected input bytes into the Output Buffer. Data is then made available on the output bus, DO.

The device can accept data input and generate corrected data at a continuous rate as high as one byte every 4 clocks. All rates lower than this are also supported. I/O with the buffers can be done in bursts at rates up to 6 MBytes/sec and up to one block at a time. The device can accept a continuous data stream at a maximum rate of 1/4 the clock frequency. Data rates and latencies are discussed further in a later section.

For every 2 check bytes, referred to as R, the decoder can correct either 2 erasures or 1 error. An erasure is an error with a known location. This can be determined with a parity detector or a signal dropout detector, for example. An erasure is indicated by asserting the ERASE signal when the erased byte is clocked into the AHA4012.

The RS code implemented in the AHA4012 uses the primitive polynomial:

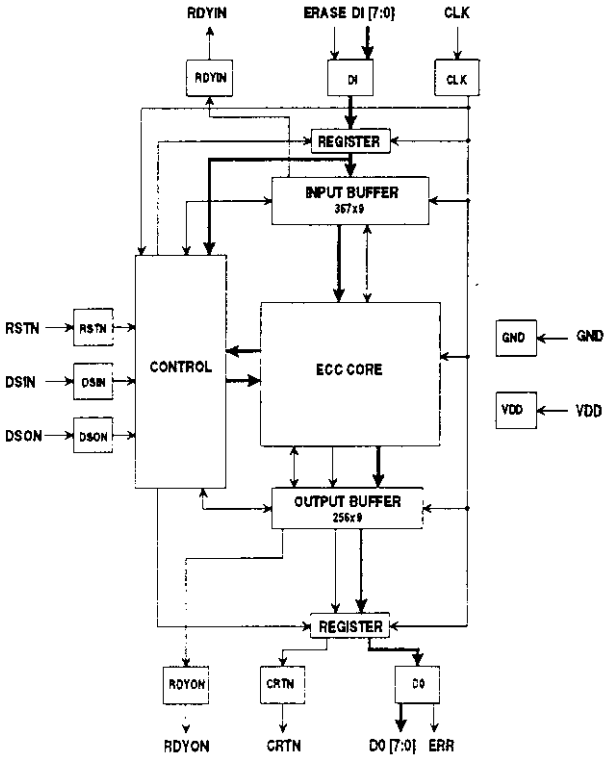
$$P(x) = x^8 + x^7 + x^2 + x + 1$$

to generate GF(256). The generator polynomial for the code is:

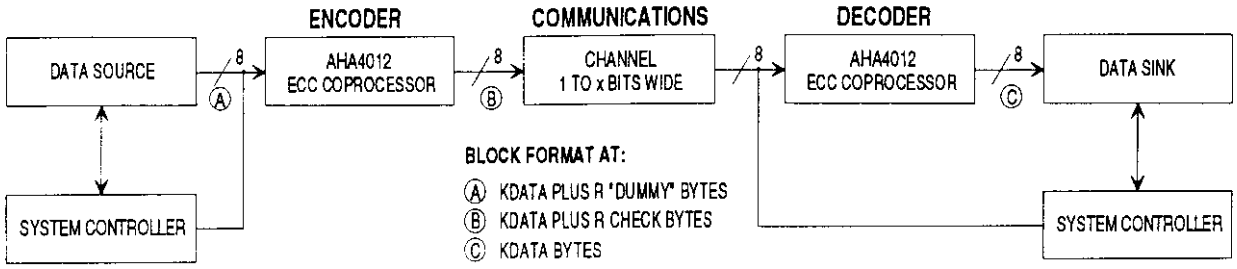
$$G(x) = \prod_{i=120}^{119+R} (x - \alpha^i)$$

These polynomials are specified by the Intelsat IESS-308, Rev 6B; RTCA DO-217 Appendix F, Rev D and proposed ITU-TS SG-18 standards. AHA designs and develops data coding solutions, including FEC, data compression and data controllers and formatters. Other FEC product offerings include AHA4011 and AHA4210.

AHA4012 DEVICE BLOCK DIAGRAM



TYPICAL APPLICATIONS DIAGRAM



SYMBOL (BYTE) ERROR RATE PERFORMANCE CURVES

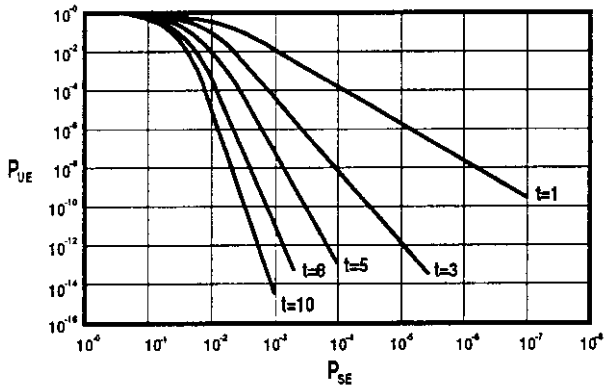
The most common measures of performance for Reed-Solomon code are P_{SE}, P_{UE} and C_{BER}. P_{SE} is the probability of symbol errors and is the ratio of the number of received symbol errors to the total number of received symbols. In the AHA4012 device, a symbol is 8 bits. P_{UE} is the probability of an uncorrectable error and is the ratio of the number of uncorrectable code blocks to the total number of received code blocks. An uncorrectable error occurs when more than t received symbols are in error. C_{BER} is the Corrected Bit Error Rate. The C_{BER} is the reciprocal of expected number of correct bits between errors.

If input noise is random, $C_{BER} = \frac{P_{UE}}{m \times N}$.

If $P_{SE} = 8 \times 10^{-4}$ with $t = 5$, $P_{UE} = 10^{-7}$ and $C_{BER} = \frac{10^{-7}}{8 \times 255} = 4.9 \times 10^{-11}$.

The figure shows probability of Symbol Error and Uncorrectable Error for Block Size (N) of 255.

Error Rate Performance Curves for N=255



DATA RATES AND LATENCIES

Maximum processing latency in burst mode, expressed in number of clocks, is $N \times C_i + R + 60 + N$ for forward order output. For C_i less than or equal to 1, use a value of 2 for C_i. Table 1 presents burst mode performance of the device.

Maximum latency in continuous mode is $(N-1) \times C_i + R + 60 + N \times \frac{C_i}{C_i - 1}$. C_i is the number of input clocks/byte. The minimum clocks/byte required for two different R values and various message lengths are shown in Table 2.

IESS code lengths operated in continuous mode are shown in Table 3.

CORRECTION TERMS

K- Number of user data symbols in one message block.

R- Symbols appended to the user data to detect and correct errors.

N- Sum of message and check symbols. $N = K + R$

t - Maximum number of errors correctable by the device. $t = \frac{\text{Integer}(N-K)}{2}$

Appendix C

LOW COST NOISE FIGURE MEASUREMENT USING THE Y-FACTOR METHOD

The design and manufacture of high performance RF receiver systems requires careful attention to characterizing and reducing undesired broadband energy or "noise." Receiver sensitivity is often degraded by the presence of this noise, and as a result, the receiver may ultimately lose the ability to detect weak signals.

Although receiver sensitivity can be measured in several different ways, "noise figure" is widely used because it can be applied not only to the entire system, but to individual components and sub-systems as well.

Today, however, the noise figure meters used to measure noise figure may have some drawbacks. When it comes to narrowband devices, for example, repeated measurements must be taken to assure noise figure accuracy, adding extra time and cost to the process. In addition, when measuring noise figure in the upper (above 2 GHz) or lower (below 10 MHz) frequency ranges, external down-conversion or up-conversion is required. (Figure 1)

There is, however, an inexpensive alternative for characterizing narrowband devices known as the "Y-Factor Method."

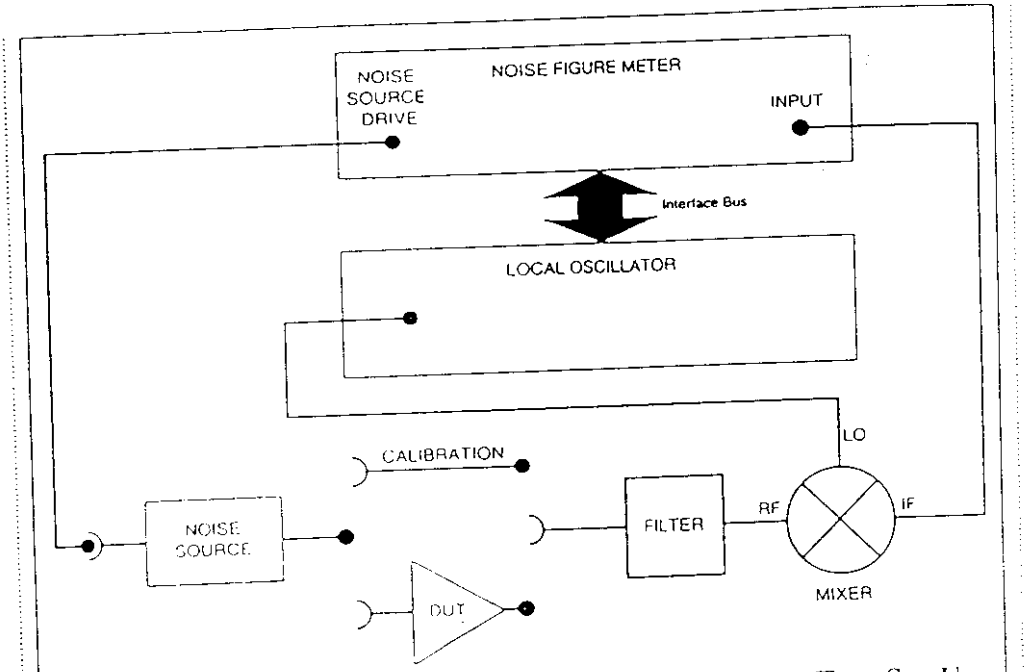


FIGURE 1: TODAY'S STANDARD NOISE FIGURE MEASUREMENT TEST SET-UP

HOW TO MAKE Y-FACTOR MEASUREMENTS

One method used to make Y-Factor measurements simply requires a spectrum analyzer and a calibrated noise source, which is supplied with all Micronetics NF-100 Series Noise Figure Instruments. (Figure 2) With the Y-Factor Method, the ability to measure noise figure at any frequency is limited only by the frequency range of the individual spectrum analyzer.

Y-Factor refers to the ratio of noise power outputs (N_2/N_1) which corresponds to the two source temperatures T_h and T_c. A precision attenuator compensates for the difference in power at the output of the Device Under Test (DUT). The amount of attenuation necessary to keep the output level for the T_h and T_c the same is the Y Factor. From this, noise figure can be calculated according to:

$$F = \frac{\left(\frac{Th}{290} - 1\right) - Y\left(\frac{Tc}{290} - 1\right)}{Y - 1}$$

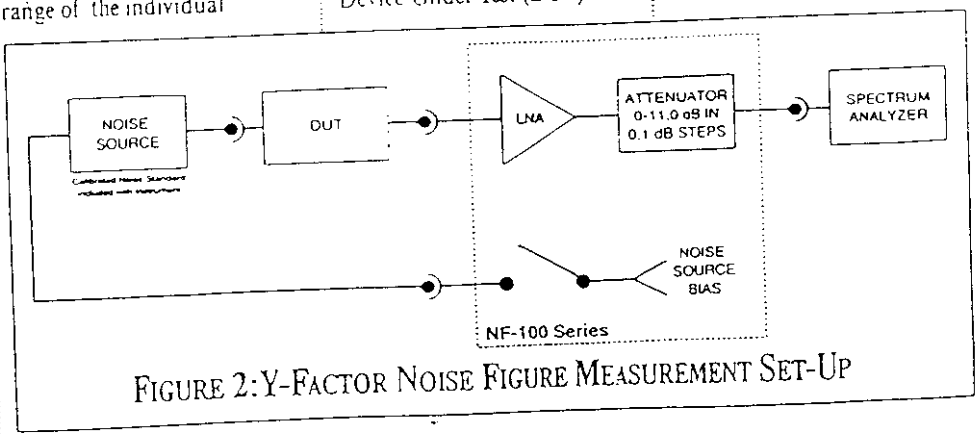
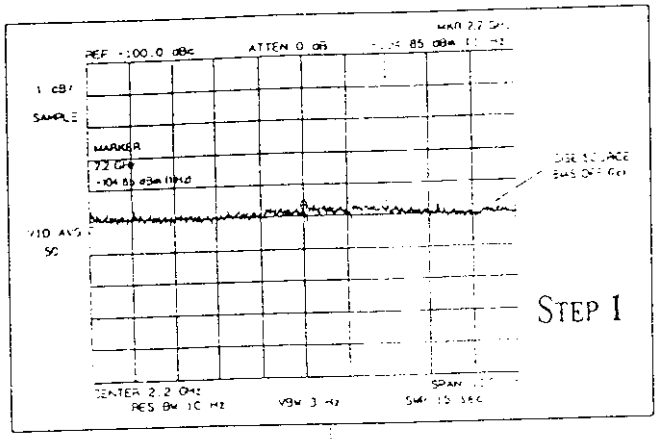


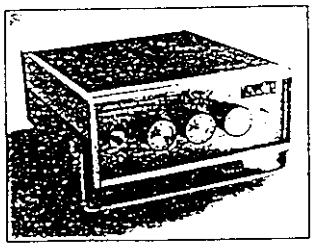
FIGURE 2: Y-FACTOR NOISE FIGURE MEASUREMENT SET-UP



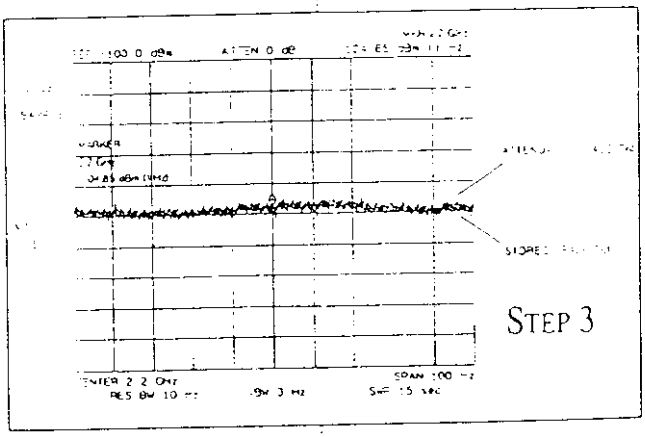
$$NF(dB) = ENR(dB) - 10_{Log}(Y-1)$$

ENR(dB) = the calibrated value as it appears on the noise source

Micronetics NF-100 Series Noise Figure Instrument includes all the necessary components for making Y-Factor measurements in conjunction with a spectrum analyzer.



NF-100 Noise Figure Instrument



GETTING STARTED

Configure the Y-Factor noise figure measurement set-up according to Figure 2.

Step 1. Begin with the cold source (T_c). Use the spectrum analyzer's video averaging to negate variations in signal amplitude. Set the measurement bandwidth on the spectrum analyzer to 1 Hz along with a convenient frequency span. (The measurement bandwidth of 1 Hz is narrower than the DUT as required for accurate noise figure measurement.)

With the noise source bias "Off," set the attenuator to 0 dB and establish a level on the spectrum analyzer. Store the trace; this becomes T_c.

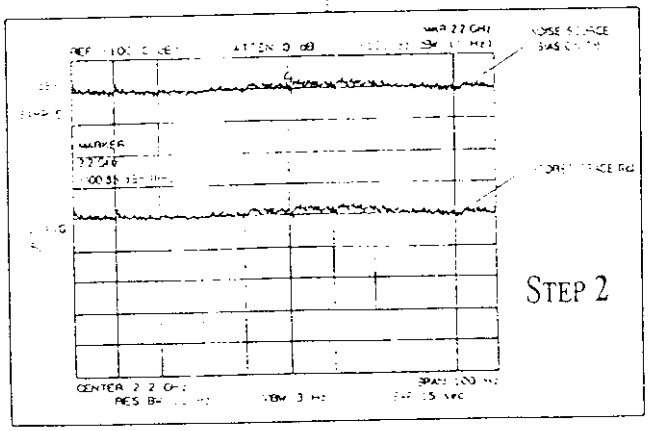
Step 2. Use the hot source (T_h). This is done by turning the noise source bias "On."

Step 3. Adjust the precision attenuator until the trace overlaps the stored trace in the previous measurement. The change in the precision attenuator is equal to the Y-Factor in dB (Y(dB)).

Because power level to the spectrum analyzer is held constant, this helps to eliminate the uncertainties caused by the nonlinearities of the power meter in the spectrum analyzer. The Y-Factor reading must now be converted to a linear ratio according to:

$$Y = INV_{Log}\frac{(Y\ (dB))}{10}$$

Noise figure can now be calculated according to:



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