UT-T2PC CARDBUS Total Block Diagram Description

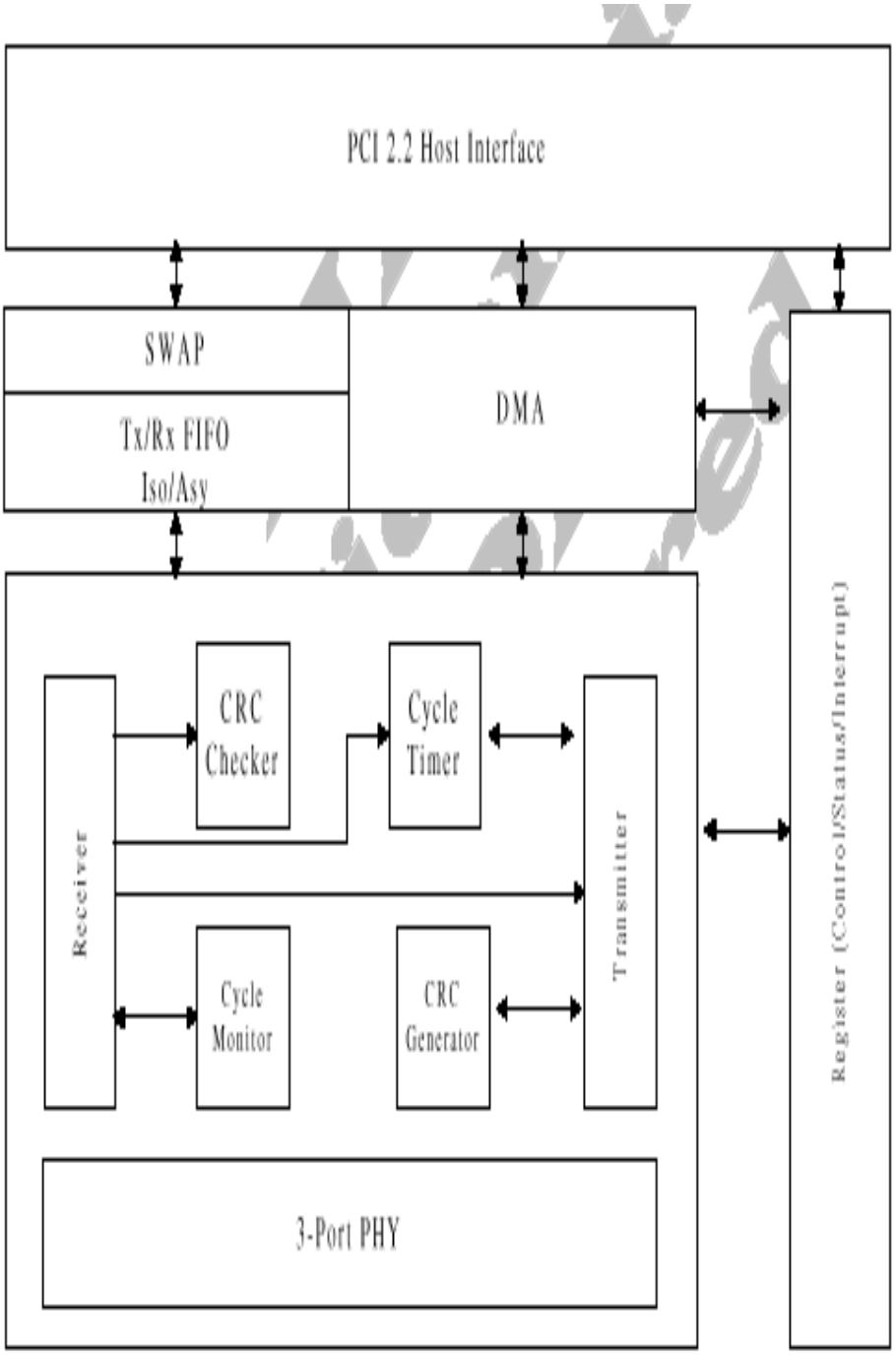


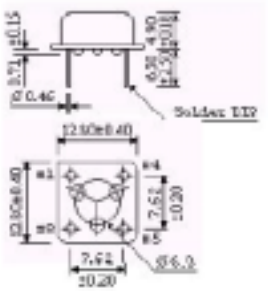
Figure 1. VT6306 Chip Block Diagram

Cycle: 24.576MHz

Oscillate Total Block Diagram Description

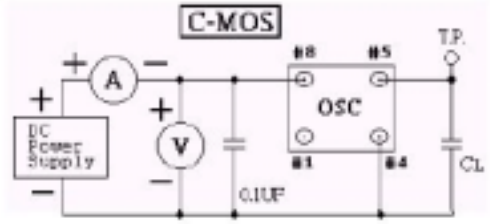
FREQUENCY RANGE:	1-100MHZ
FREQUENCY STABILITY: (INCLUSIVE OF CALIBRATION TOLERANCE AT 25C, OPERATION TEMPERATURE RANGE, INPUT VOLTAGE CHANGE, LOAD CHANGE, AGING SHOCK AND VIBRATION)	A:(+)(-)100PPM B:(+)(-)50PPM C:(+)(-)25PPM
TEMPERATURE RANGE: OPERATING TEMPERATURE STORAGE TEMPERATURE	 -10C TO 70C -55C TO 125C
INPUT VOLTAGE:	4.5-5.5 VDC
INPUT CURRENT:	1-20MHZ 20mA MAX 21-35MHZ 30mA MAX 36-50MHZ 40mA MAX 51-100MHZ 55mA MAX
CMOS OUTPUT: SYMMETRY RISE AND FALL TIME	 60/40% TO 40/60% (AT2.5VDD) 1-50MHZ 10NS MAX 51-100MHZ 5NS MAX
OUTPUT LOAD:	15PF

DIMENSIONS (UNIT mm)



Pin connection	
PIN	CONNECTION
1	N.C or Tri - State
4	CASE GND
5	OUT PUT
8	5.0VDC

TEST CIRCUIT



OUTPUT WAVEFORM