DS 350 COMMAND RADIO VHF HANDHELD TRANSCEIVER

The DS350 transceiver consists of four major sections

1. Main RF board
2. Main Logic board
3. Audio Processing Module
4. Keyboard PCB

MAIN RF BOARD

The main RF board contains one complete synthesized VHF transmitter and two synthesized VHF receivers. One receiver is used as a guard or overhead channel. It is used to receive channeling or data commands. The other receiver is used for voice (working channel). The transmitter can send voice or data on any frequency allowed by its programming.

Transmitter

The transmitter shares the synthesizer IC (U5) with the working channel receiver. This transmitter has its own VCO (MOD1, TX VCO). Power is switched on to the transmitter via transistors Q15, Q16 and Q17. TX 5.5V is the transmitters power supply. The TX VCO can be frequency-modulated by applying an AC signal (modulation) at its MOD pin. Another modulation signal is applied to the reference oscillator (MOD2, TCXO).

MOD2 is a temperature controlled/voltage controlled crystal oscillator. It is the main reference for both synthesizers. It maintains a +/- 2.5-PPM frequency accuracy from –30°C to +60°C. Modulating this reference aids in producing more linear FM modulation at low modulating frequencies.

The FM signal from the TX VCO is buffered and amplified by transistors Q6 and Q8. This signal drives the Transmit Power Amplifier (MOD4, TX PA) via coupling capacitor C52.

Buffer/amplifier Q6 also provides the RF signal feedback to the synthesizer IC (U5). Diode D2 is switched on by the TX 5.5V supply to allow the signal to be coupled to U5. Diode D3 isolates this signal from the receive VCO buffer.

The TX PA module amplifies the signal to eventually drive the antenna. The output of the TX PA is passed through a low pass filter C57, C58 and L9. This signal is then fed to a directional coupler in order to measure the power being “sent” to the antenna. The directional coupler DC1 and DC2 are actually PC board traces (a coupling strip). Power going to the antenna is coupled to the strip DC2 and rectified by diode D4 and filtered by C60. As the forward power increases, the voltage drive to Q10 increases. As Q10 conducts harder due to the increased drive, Q9 will have less available base voltage. Since Q9 is an emitter follower, the reduced base voltage causes the emitter to drop in voltage as well. This emitter is the control voltage (Vgg) that controls the transmit PA module. As Vgg drops, the power output drops. This forms a feedback loop to stabilize the forward power to the antenna. Adjustment R56 controls the transmitter in the HI (5W) power mode. Q12 is on, shorting R57 in the HI power mode. In the low power mode, Q12 is off, putting R57 into the circuit; this adjusts the transmitter power in the LO (1 or 2W) power mode.

A second control, PA EN (PA Enable) controls Q18. Q18 is a dual transistor used to allow Q9 to have a collector supply. If the PA EN pin (P3-13) does not switch HI, Q9 cannot supply Vgg (control voltage) to the TX PA. If the transmit PLL is out-of-lock, transmit power is switched off by this control path.

In the transmit mode, the TX 5.5V supply turns on diode D5 via R60, R39, L10, L11 and D6. D5 allows the forward transmit power to be sent to the low-pass filters of L12, C64, C63, C65, L13, L14, C67, and

C66. This filters out the upper harmonics that are produced by the transmit power amplifier. The forward current that switches on D5 also switches on D6. This prevents damaging transmit power from reaching the power splitter and RF amplifier in the receiver section. In the receive mode, D5 and D6 are off, allowing received antenna current to flow to the receiver section. D5 prevents the current from traveling backwards into the transmitter power sections.

Working channel receiver

Voltage regulator U8 provides 5.5V to Q15. This receiver has it's power switched on by Q15 (RX 5.5V). RX 5.5V supplies power to the receive VCO (MOD3). It also supplies power to the Guard Channel Receiver. The VCO signal is buffered and amplified by Q7. Diode D3 is switched on by the RX 5.5V supply. This VCO signal is fed through the same filters as the transmit VCO signal. The synthesizer IC (U5) uses this signal as a feedback signal.

U5 is a fractional N synthesizer that divides the reference signal produced by MOD2. The result is an available frequency increment of 2500Hz. This reference is compared with the feedback signal from the VCO modules (MOD1 in transmit, MOD3 in receive) by the phase detector in U5. If the VCO signal is lower than it should be, U5 provides pulses to raise it. If the VCO signal is higher than it should be, U5 provides pulses to lower it. A low-pass filter made from C90, R80, C89, R79, and C88 filter these pulses into a DC voltage used by the VCO (transmit and receive) to control its frequency. This DC voltage (tuning voltage) is also used by the front end module (MOD8) to center its frequency response, thereby tracking the desired receive frequency.

The receive VCO signal (after buffering/amplification by Q7) is fed to the first mixer (MOD5). MOD5 is a passive, double balanced mixer module. The other input to the mixer is the RF signal coming from MOD8.

The signal from the antenna passes through the transmitters low-pass filters and is blocked by diode D5. D6 is also off in the receive mode allowing the received signal to pass through a high-pass filter of L23, C70, C69, L15, C71, L25, L24, and C73. This signal is then fed to an RF amplifier (Q13) that amplifies and divides the signal available from the antenna. The RF signal at the antenna must be split evenly between two receivers. Q13 uses a power splitter transformer (PS1) to differentially drive the two front-end modules (MOD8 and MOD9).

MOD8 is a track - tuned filter and RF amplifier. The output of MOD8 drives the RF input of the first mixer (MOD5).

The desired IF output of MOD5 is 21.4MHz. This first IF signal from the mixer is applied to transistor Q3. This stage effectively matches the low impedance output of the mixer to the much higher input impedance of the first IF crystal filter (XF3). The output of XF3 is buffered and amplified by Q4 and passed through another 21.4 filter, XF4. R26 provides a good match (DC loading is blocked by C21) to the IF chip, U2. U2 contains the second local oscillator (LO), the second mixer, the second IF amplifier and limiter amplifiers and a quadrature discriminator. It (U2) also provides a current output proportional to the input signal strength (RSSI, or Received Signal Strength Indicator). R27 and C22 convert this current to a filtered DC voltage used by the main microprocessor. Amplifier U10 inverts the RSSI signal and provides some gain to provide better resolution.

The incoming first IF signal at 21.4MHz is mixed with the 20.945 MHz (Y2) signal of the second LO. The difference signal (second IF) is then at 455kHz. This 455kHz signal is then fed to one of two second IF filters, CF2 or CF3. Transmission gates U3 and U4 switch the inputs and outputs of the filters. These transmission gates are controlled by Q5. The main processor switches Q5 depending on the desired channel bandwidth required (wideband or narrowband, 25 or 12.5 kHz). U3 and U4 are always in opposite switch states.

The second IF filter output is amplified and limited inside U2 to strip AM products. L4 provides the correct phase shift for the detector. Recovered audio is present at pin 9 of U2. R30 and C27 remove any residual 455KHz signal that will ride on the audio.

Guard channel receiver

This receiver has it's power switched on by Q15 (RX 5.5V). RX 5.5V supplies power to the receive VCO (MOD6). The VCO signal is buffered and amplified by Q11. This buffered signal is sent to the first mixer MOD7, and through a low-pass filter L29 and C26, to the synthesizer IC U6.

U6 is a conventional synthesizer using the signal from MOD2 as a reference. This reference is compared with the feedback signal from the VCO modules (MOD6) by the phase detector in U6. If the VCO signal is lower than it should be, U6 provides pulses to raise it. If the VCO signal is higher than it should be, U6 provides pulses to lower it. A low-pass filter made from R75, R76, C84, C83, R72, and C97 filter these pulses into a DC voltage used by the VCO to control its frequency. This DC voltage (tuning voltage) is also used by the front end module (MOD9) to center its frequency response, thereby tracking the desired receive frequency.

The receive VCO signal (after buffering/amplification by Q11) is fed to the first mixer (MOD7). MOD7 is a passive, double balanced mixer module. The other input to the mixer is the RF signal coming from MOD9.

The signal from the antenna passes through the transmitters low-pass filters and is blocked by diode D5. D6 is also off in the receive mode allowing the received signal to pass through a high-pass filter of L23, C70, C69, L15, C71, L25, L24, and C73. This signal is then fed to an RF amplifier (Q13) that amplifies and divides the signal available from the antenna. The RF signal at the antenna must be split evenly between two receivers. Q13 uses a power splitter transformer (PS1) to differentially drive the two front-end modules (MOD8 and MOD9).

MOD9 is a track - tuned filter and RF amplifier. The output of MOD9 drives the RF input of the first mixer (MOD7).

The desired IF output of MOD7 is 21.7MHz. This first IF signal from the mixer is applied to transistor Q1. This stage effectively matches the low impedance output of the mixer to the much higher input impedance of the first IF crystal filter (XF1). The output of XF1 is buffered and amplified by Q2 and passed through another 21.7 filter, XF2. R10 provides a good match (DC loading is blocked by C6) to the IF chip, U1. U1 contains the second local oscillator (LO), the second mixer, the second IF amplifier and limiter amplifiers and a quadrature discriminator. It (U1) also provides a current output proportional to the input signal strength (RSSI, or Received Signal Strength Indicator). R11 and C7 convert this current to a filtered DC voltage used by the main microprocessor.

The incoming first IF signal at 21.7MHz is mixed with the 22.155 MHz (Y1) signal of the second LO. The difference signal (second IF) is then at 455KHz. This 455KHz signal is then fed to a ceramic filter CF1. The guard channel is assumed to be always a narrow band signal.

The second IF filter output is amplified and limited inside U1 to strip AM products. L2 provides the correct phase shift for the detector. Recovered audio is present at pin 9 of U1. R12 and C14 remove any residual 455KHz signal that will ride on the audio

MAIN LOGIC BOARD

The main processor (U12) resides on the logic board. This logic board also serves as the carrier for the audio module. The main processor has its program memory residing in a Flash EEPROM, U3. This program memory is programmable in system with special software running on a PC. A Static RAM (SRAM, U4) is used for data memory that is used either for the display or for channel configuration data.

This SRAM is backed up by a Lithium battery (B1) to prevent loss of data when the main power is shut down.

A programmable logic array is used as a latch. This latch holds the lower part of the address sent to the Flash memory and the SRAM. It also latches several command lines used by the synthesizer chips, audio module, etc.

An optically coupled serial data interface using optocoupler U6 is used to receive data from a PC. Q3 and R57 send data to a PC.

A small serial EEPROM (U9) is used for detail data that must be kept in the event of a total loss of power, including the lithium cell. U8 is a Real Time Clock that is used to maintain a correct Time-of-Day. U8 has its own clock, (32KHz) for timekeeping.

Power to the logic system is controlled by a small microcontroller U17. This controller is essentially powered up constantly by regulator U10. The reset controller U7 monitors the battery condition to force a reset of this power controller. U17 is essentially "asleep" as long as the main ON/OFF switch is OFF. If the power switch is turned ON, U17 is interrupted and it turns power to the logic section on via regulator U2 and Q7. The 17MHz clock for this part is then gated on and sent to the main processor by transmission gate U1A. When the main processor "wakes up" U17 stays on. If the Power Save mode is entered, the main processor tells the power control processor (U17) it is ready to be powered down. The main processor cannot be powered down unless it is ready to be shut down. This prevents corruption of crucial SRAM data. When U17 is instructed, it drops power to the entire logic board, except for the power control processor itself. Every 100 msec U17 will wake the logic section in a special mode. The main processor will only check the radio sections and then signal U17 that it can return to a power-down state.

In this power save mode, voltage to the RF section (except for the reference oscillator) is shut down. The power is back on for approximately 50 msec to check the radio status. Power to the LCD display remains on, maintaining data on the screen.

If the PTT switch is depressed, it will interrupt U17 in the sleep mode and immediately wake the main processor.

Regulator U16 and transistor Q6 supply a regulated voltage to the on-board GPS receiver module.

Resistor R5 and R6 divide the battery voltage down so the main processor can detect low battery states.

Also on the main logic board is both audio power amplifiers (U13 audio PA). There is a separate audio PA for both the internal speaker and the external speaker/mic option. Receiver audio is conditioned by the audio module and sent to transmission gate U14. One of the gates of U14 is on at any time. If an external speaker/mic is plugged in, the line marked INT/EXT is grounded, causing U14B to be switched off, U14A to be switched on. Receive audio is routed to the external audio PA (U13B). Audio is routed by U14B to U13A if the INT/EXT line is high (no external speaker/mic is connected). Q5 and Q4 switch power to the audio PA. If no signal is present, the audio PA is powered down to save energy and quiet the speaker(s).

The microphone amplifier for the external speaker/mic is on the main logic board. U19 provides signal from the external mic to transmission gate U11A. Transmission gate U11B receives mic audio from the amplifier on the keyboard PCB. Only one mic amp is used at a time, the audio is routed into the audio module via U11 (A or B).

AUDIO PROCESSING MODULE

Transmit Audio path

The conditioning of the receive and transmit audio is done primarily by U2 and U3. U3 has a crystal (X2) for its oscillator. The oscillator output of U3 feeds U2. The Vcc supply for all part on the audio module is Avcc, 5V. This power is on anytime the RF section is powered up.

The internal microphone is amplified by an amplifier (U5) on the keyboard PCB. This amplifier adds some gain as well as high-pass filtering (pre-emphasis). This amplified mic audio is sent to the logic board and transmission gate U11. The INT/EXT control line controls this gate. The external mic is amplified and filtered by U19. The audio from either mic is then sent to the audio module.

This audio is summed with the DTMF (MX829, U3-16) signal and the DSC modem data at pin 13 of U3. The level of the DSC data is adjusted by R16; the level of the DTMF tones can be adjusted by R15.

The signal going into pin 13 is amplified and low-pass filtered again by an internal amplifier in U3. This filtered signal is then passed through a high-pass filter. This sets the allowable modulation spectrum. The signal is then passed through a limiter (still contained inside U3) and a low-pass filter to set the total level of signal.

The output of this attenuator is pin 15 of U3. The modulation from the 4FSK (high-speed) modem is summed with the Sub-Audible tones at this pin. The level of the 4FSK signal is adjusted by R17; the level of the sub-audible tones is set by R14. This composite signal (now contains all possible modulating signals) is buffered and summed by the amplifier at pin 17 of U3. The result of the summing is present at pin 18 of U3.

This summed output is connected internally to an attenuator that feeds the MOD 2 output (pin 23 of U3). The summed output is also connected to an inverting unity gain buffer (U5). This inverts the signal and sends it to pin 19 of U3. This signal then feeds the attenuator that outputs to MOD 1. This allows for two-point modulation to be used that is 180 degrees out-of phase for the reference oscillator modulation.

The MOD 1 and MOD 2 amplifiers can be attenuated 6dB for narrowband transmissions.

Receive Audio path

The receive audio from the IF (J3-6) is sent directly to U6 (4FSK modem) and to the working DSC modem (U7). Both parts have internal amplification and band limiting. The output of the 4FSK modem is sent to the main data bus. It outputs parallel data. The DSC modem output is serial data.

The same receive audio is applied to U2, pin 14. This connects to an internal amplifier that adds gain and some low-pass filtering. The output of this amp is sent to an internal Sub-Audible tone detector. The amplified signal is also sent to a bandpass filter that removes the sub-audible tones and limits the high frequency content of the recovered audio. This signal is then sent to an attenuator. In the wide-band receive mode this attenuator is set to 6dB. This filtered and attenuated (if necessary) signal is sent through the scrambler (if it is installed) and on to the volume control potentiometer on the top of the radio and to the DTMF decoder IC (U1).

The audio signal from the wiper of the volume control is sent to pin 20 of U3. This connects to an attenuator internal to the chip. Turning this attenuator off when the processor sends a key beep prevents receive audio from being heard mixed in with the beep.

This signal is then sent to the audio power amp (and transmission gates) on the logic board.

The recovered audio from the guard channel is sent only to (U4) to decode the DSC signaling data. The recovered audio is not sent to the internal speaker.

KEYBOARD PCB

The keyboard PCB contains the switch pads for the elastomer keyboard. It also contains the mic amp for the internal microphone. The interface to the display is handled here. The LCD module needs negative 10 volts to operate. U1 is an inverting charge pump that converts +5V to –5V. The – 5V is then sent to U2. U2 doubles the –5V to –10V.

The network of RT1, R11, R12, and D11 control the overall display contrast. As the ambient temperature changes, the Vlc voltage (pin3 of J2A) must change to compensate for the temperature change.

U3 inverts and stretches the Enable pulse to the display. U4 inverts the second chip select pin on the display module to ensure that only one half of the display is being written to at a time.

Q3 switches the backlight on the LCD module on. Q1 turns on the backlights for the elastomer keyboard. D1 through D5 are green LED's mounted on the keyboard PCB.

Filters FL1 through FL25 prevent noise from the logic board from being conducted up the flex cable to the LCD module.