NSA2010 System Description
(refer to the block diagram)

1.1 Receiver (RX) section

1.1.1 Input (receiving frequency)

fri=869.040 to 893.970 MHz, 30KHz step

1.1.2 Description

The RX signal caught by Helical antenna is fed to RX RF amplifier and mixer (Q101,Q121) through the duplexer (F100) with band-pass filtering.

→ See characteristics of the duplexer (DFYGR836CR881NHA).

Then the RX signal amplified by Q101 and applied to RX mixer1, Q121 (RX MIX1) through the SAW band-pass filter (F102) which reduces out of band noises and spurious.

→ See characteristics of the SAW band-pass filter.

The signal of input is mixed with the local frequency (fo1) which is generated by the VCO (X911) that works as a frequency synthesizer combined with phase locked loop IC, U900, at the first mixer Q121.
The output of the first mixer generates first IF frequency (fi1) , 86.460MHz and this signal is delivered to the first IF filter (F102).

The fi1 and fo1 is calculated as below;
The second IF frequency fi2=60KHz
The second local frequency fo2= 14.4MHz(TCXO frequency) x6 =86.400MHz
Therefore, fi1= fi2 + fo2 =86.460 MHz
Therefore, fo2=fri + fi1 =955.500 to 980.430MHz, 30KHz step

The F102 is a SAW filter with 86.460MHz of center frequency that has very good shape factor.
This filter works to eliminate alternate frequency (fi1+/- 60KHz) and image frequency of second mixer (fi1+120KHz=86.58MHz) that rejection ratio should satisfy the specification.
→ See characteristics of the SAW IF filter.

The fi1 signal is amplified by Q131 in order to obtain enough gain of RX section.

The IC, U101, is incorporating the following function;
Second Mixer with image frequency cancellation circuit,
Band-pass filter with 60KHz of center frequency
Second IF amplifier
FM detector
RSSI (Receiving Signal Strength Indicator) output)
→ See block diagram and characteristics of TA31181FN.

The second local frequency (fo2=86.460MHz) is obtained to be multiplied by six(6) of TCXO frequency (f TCXO=14.4000MHz).
The f TCXO is fed to tuned amplifier inside of U900 and Q171. The about 86 MHz tuning circuit, L171, L172, C174 and C175, picks up the 86.400MHz which is a six times harmonics of f TCXO.

The second mixer inside of U101 generates a second IF signal which frequency is 60KHz
The fo2 is split into 2 path inside of U101, one for in-phase signal and other for quadrature signal. These signals are applied to two second mixers.
The output of second mixers is synthesized with 90 degrees phase shifting for quadrature mixer side.
This function works to make cancellation of the image frequency, about 30dB rejection ratio.
About 75 dB total image rejection ratio for fi2 can be obtained to combine with F102, even though such lower IF frequency.

The sharp narrow (+/-15KHz) BPF having 60KHz-center frequency inside U101 works to eliminate adjacent channel.
The center frequency of 60KHz BPF is synchronizing to its clock frequency, 14.400MHz that is fed from TCXO. So very stable filter characteristics can be obtained due to very stable frequency of TCXO.

After 60KHz filtering, the signal is amplified and limiting its amplitude by limiter.
Then quadrature detector that is incorporated into U101 demodulates the FM signal. The center frequency is also synchronizing to 14.4 MHz like 60KHz filter.

RSSI (DC level) is obtained to gather second IF signal.

1.2 Transmitting (TX) section

1.2.1 TX frequency

ftx= 824.040 to 848.940MHz, 30KHz step

1.2.2 Activation control for the transmitter

When TX starts to activate, TX VCO and TX section of the U101 simultaneously.
The TX VCO is switched by Q701 that is controlled by CPU with active high level, and TX section synthesizer of U101 can be controlled by data from CPU through its serial data transmission line, SYE, SYD and SYC.
After a few milliseconds waiting, the TX switch, Q606 and Q607 work to turn on. Then all TX sections as U201 (buffer amplifier), Q603 (TX driver), Q604 (TX final power amplifier), U241 (APC circuit) Q607 and Q606 (power switch) become to activate.
Note that TX switch circuit, Q606 and Q607 are not switched on if TX synthesizer circuit including VCO has already activating. The synthesizer must be priority in order to activate all TX circuits. The emitter of Q607 detects whether synthesizer is activating, i.e., Q607 must be low level for activation.

Usually it is switched on; then, enough current capacity is applied to final stage of TX power amplifier VCC (6.0V).

1.2.3 TX VCO and Modulator

The basic TX VCO circuit is built of X931.

It is controlled by applied DC voltage that is the output of the synthesizer, U900, through low pass filter, C939, C935, R932, R933 and C933.

The controlled voltage is within 0.8 to 2.2V to cover the TX frequency range.

The CPU is monitoring synthesizer lock-upped DC voltage through the TVL line.
If this voltage is out of 0.8 to 1.0 volt at minimum frequency, CH0991, the DC voltage to TX V.C.O applied from CPU through TVA line is adjusted until becoming specified range since this loop works as negative feedback circuitry.
After fixing DC voltage at CH0991, the synthesizer frequency moves to upper frequency, CH0799 and monitored this frequency by CPU through TLV line.
If this DC voltage is lower than 2.2volt, this VCO is accepted, otherwise, higher than 2.2V, this is failure VCO and rejected.
At the same time, lock condition is monitored by CPU and unconditionally is rejected if unlocked condition occurs.

TX V.C.O is also used for the modulator. The modulation signal comes from the base band processor through MOD line. R401 and R934 to be obtained optimized modulation level divide this signal. → Refer to paragraph of Modulation

1.2.4 TX power stage

The fig.1.2.4.1 shows block diagram of TX power stage for NSA2010.

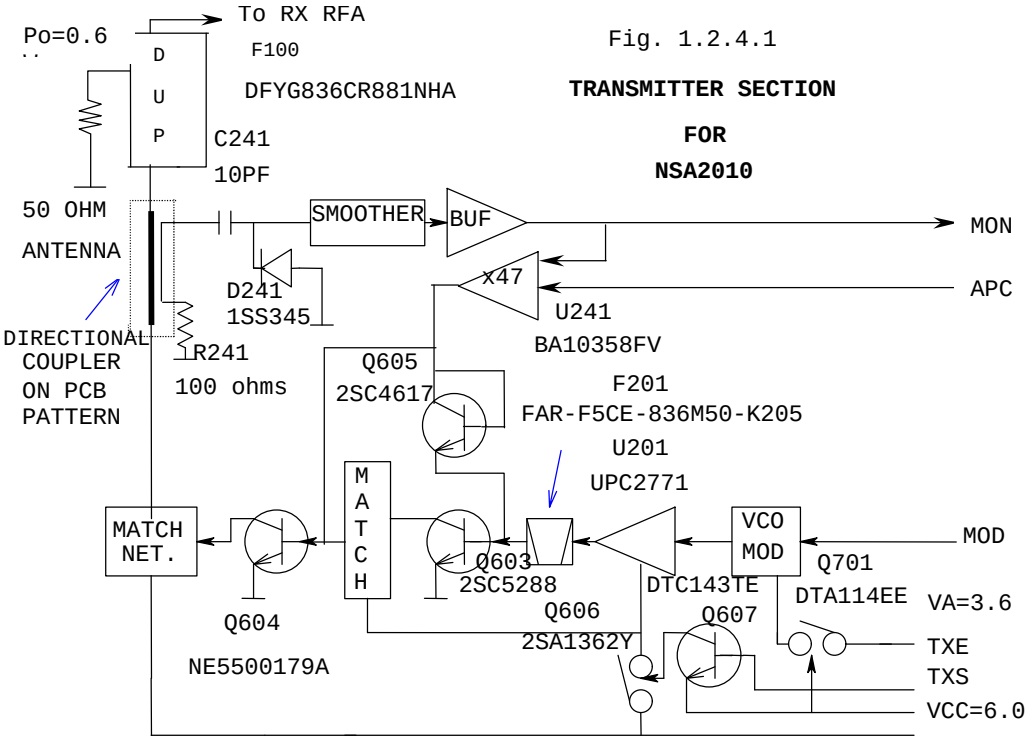


Fig. 1.2.4.1

TRANSMITTER SECTION

FOR

NSA2010

The modulated FM signal generated by TX VCO is amplified by U201 and obtained about 10mW (10dBm) output power on U201.
And about 5mW (7 dBm) that drives driver transistor, Q603, is obtained at the output F201 which has about -3 dB gain.

Both TX power amplifier and driver consists of discrete circuits. The driver transistor, Q603, which have class-AB biasing can obtain about 100mW RF power output that is used for driver for final stage of power amplifier.
The Q605 is used as bias compensation circuit of Q603.

The final transistor, Q604, which is biased class-AB, is an N channel silicon MosFET.
The current drain of Q604 is 350mA at the 0.6W power output.
The power gain is about 11 dB and delivering about 1.2W power input for the Duplexer (F100) through directional coupler made by PCB pattern.
→ See data sheets of NE5500179, 2SC5288 and UPC2771T.

Protection Against False Transmission

When the loop of synthesizer becomes unlocked, the TX VCO, X931 oscillates out of band frequency or spurious frequencies.
The unlock detection port of U900, pin #5 falls into Low level in unlock condition although this port is keeping High level in locked (normal) condition.
The port of CPU U504, pin #93 is monitoring the level of unlock port of U900, pin #5.
If pin #93 detects High level, the system works as normal condition.
If Pin #93 recognized low level, CPU U504 suddenly works to set High level of TXE line (pin #97 of U504) and Low level of TXS line (pin #98 of U504).
Then, Q701, Q606 and Q607 turn off.
This condition means that the all transmitting circuits are shut down by force. (Refer to paragraph 1.2.2 and fig.1.2.4.1)

1.2.5 Automatic Power Control (APC) circuit

The operation of APC is described as following:

a. The directional coupler composed by PCB pattern by F202 RF coupler with the
Detects traveling wave of TX output power.
b. The D241, low forward voltage Schottky-barrier diode, rectify the RF signal and getting DC signal after smoothing circuit.
c. This detected DC level is compared with reference voltage that is supplied from CPU through APC line, at comparator, U241.
The reference voltage of APC is obtained in advance at the alignment process and memorized into EEPROM. The CPU gets this data and converting to DC using on chip R-2R type DA (digital to analog) converter for APC reference.
There are 8 levels of power level that is specified by IS-19B (+8 to 28dBm).
d. The difference DC voltage between detected DC and APC reference is amplified by U241 and controlling the bias voltage of Q605 (driver).
If detected voltage is greater than reference voltage, the bias voltage of Q605 works to be reduced that means to reduce output power since this circuit is looped as negative feedback
e. The loop operation is completed if the difference of detected and reference voltage is almost zero.
→ See data sheet of 1SS345.

1.3 TCXO (Temperature Compensated Crystal Oscillator)

The X451 is the crystal oscillation circuit for TCXO.
In general, crystal oscillation element with AT-cut has a third order curve frequency variation versus temperature.
In order to achieve stable oscillated frequency in wider temperature range (-30 to

+60 C degree), the selected crystal element in limited temperature characteristics and compensatory circuit should be required for TCXO circuit.

The fig.1.3.1 shows the frequency variation versus temperature for this circuit. And the initial frequency can be adjusted by AFC voltage that comes from the DA converter of the CPU. → fig.1.3.1
The IS-19B specifies the frequency tolerance must be below 2.5ppm (parts per million) in temperature range of –30 to +60 C degree and long term time passing. This TCXO frequency is used for the reference frequency of synthesizer circuit, clock for U101, fundamental frequency of RX second local frequency, time base for base-band processor (U501) and system clock of CPU as 4.8MHz which is obtained divided-by 3 of TCXO frequency by the counter inside of U501. → See fig. 1.3.2

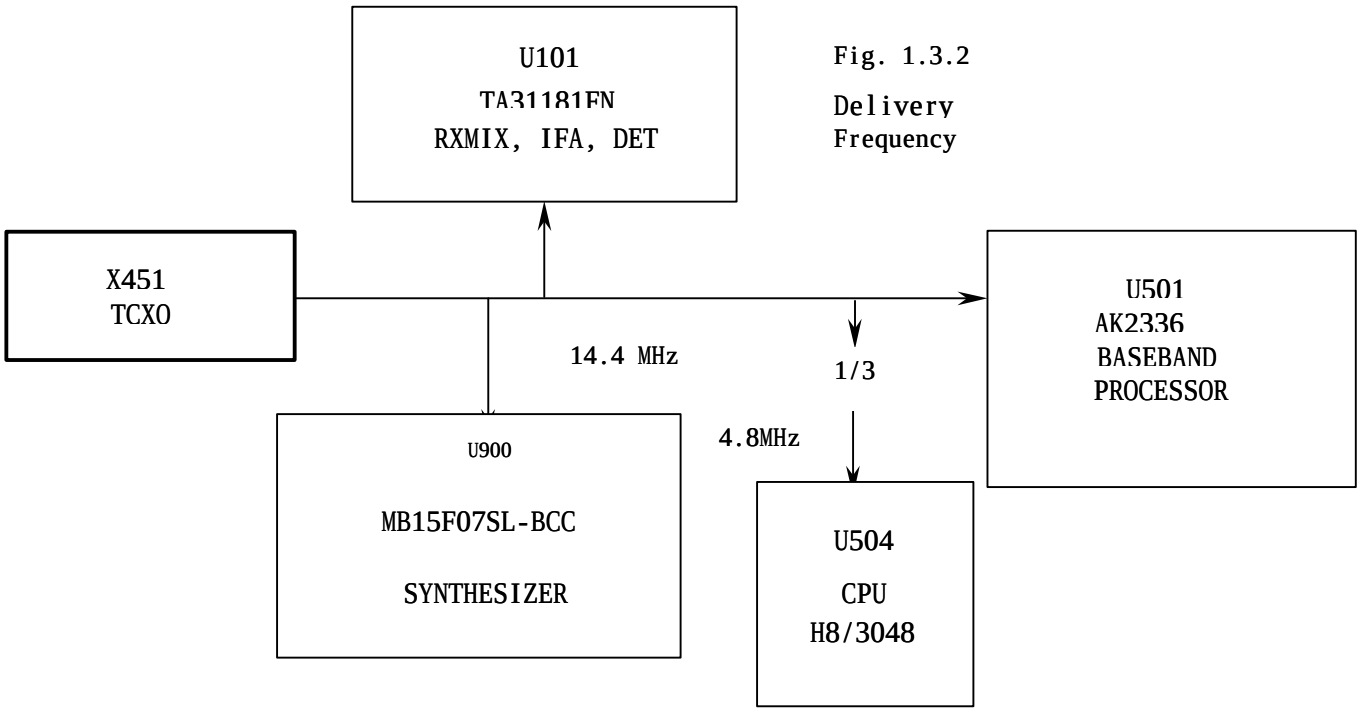


Fig. 1.3.2

Delivery Frequency

1.4 Synthesizer section

The fig.1.4.1 shows the block diagram of the synthesizer IC, MB15F07SL-BCC This IC has a dual 1.1GHz programmable counter, a programmable reference counter, a dual phase comparator and a dual constant current drive charge pumps.
All control data is transferred from CPU through three line synchronous serial bus.

The program data can be calculated as following:

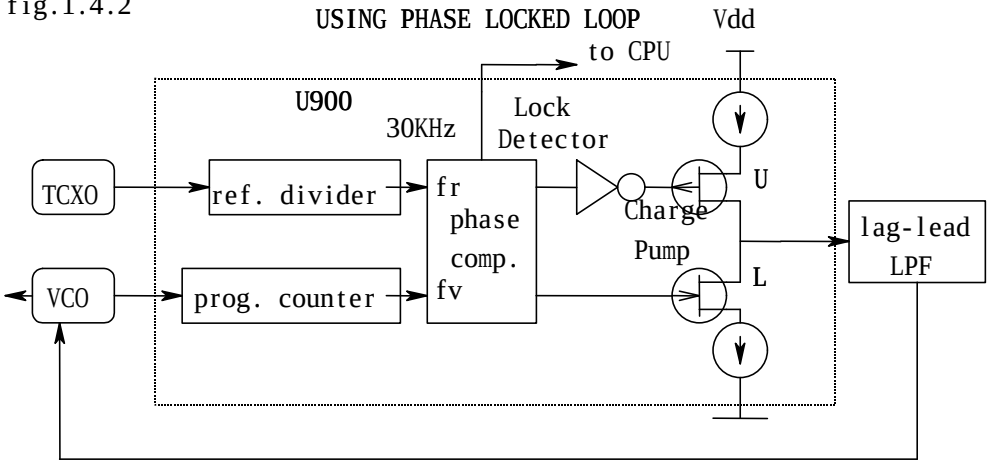
a. the divided-by N of reference frequency ; Nr = 14.4/0.03 =480=1E0h
b. the divided-by N or TX frequency ; Nt= (824.040 - 848.970)/0.03=27468 - 28299
=6B4Ch - 6E8Bh
c. the divided-by N of RX local frequency; NL=(955.500 - 980.430)/0.03= 31850 - 32681=7C6Ah- 7FA9h where *h* means hexadecimal data and frequency step per channel is 30KHz.

The output of VCO is fed to programmable counter and divided by Nt or NL. This

divided signal is applied to phase comparator and compared with reference frequency, 30KHz.

From fig.1.4.2 the upper charge pump (U) turns on and lower charge pump turns off if
divided-by Nt or NL (fv) is smaller than Fr(30KHz)..

fig.1.4.2 BLOCK DIAGRAM OF BASIC SYNTHESIZER USING PHASE LOCKED LOOP



As the output of charge pump gives pulse wave, the second order lag-lead low pass filter is used to generate smooth waveform for VCO control.
If both phase and frequency of *fr* and *fv* are coincident, the output of charge pump becomes very high impedance and the DC level of VCO control voltage is holding.
Due to very low leakage current of the capacitor in the lag-lead filter and very high impedance of charge pump output, the frequency stable output of the VCO can be obtained for long time.

In idle mode, the RX synthesizer is activating and TX synthesizer section is inactivating.
The RX synthesizer is scanning the control channel.
In conversation mode, both synthesizers are activating simultaneously.

1.5 Base-band and Modulation

TheAK2336 is a base-band processor for AMPS that includes RX and TX bandpass filter, voice signal processing both RX and TX, compandor, wideband decoder and encoder, majority voting, SAT decoder and encoder and peripheral circuits.
(See data sheet for details)