DESCRIPTION OF CIRCUIT FUNCTION

5. DESCRIPTION OF CIRCUIT

5.1 SUMMARY

This radio call pager is POCSAG CODE mode radio call receiver which is operated in frequency range of 929.000~932.000KHz as UHF range the signal modulated to BINARY FSK-NRZ is received as DOUBLE HETERODYNE mode and the received number or character are displayed on 12 positions LCD, therefore it is radio call receiver of NUMERIC DISPLAY TYPE.

5.2 DESCRIPTION OF CIRCUIT

5.2.1 RECEIVING PART (RF PART)

1) ANTENNA
It is designed suitable to human body's influence and field features
.as small loop antenna.

2) RF AMPLIFIER AND BATCH PASS FILTER (BPF)
Received RF signal from antenna is approved as TR(Q1) Base and TR(Q1)&TR(Q2) are connected to CASCADE in the amplifier and it is designed so that FEED BACK of partial signal can be suppressed maximumly. At this time noise index is less than 2, therefore low voltage amplification is available at very low noise producing condition. BPF circuit is composed F1(SAW FILTER), L&C and surrounding terminals RF batch is passed.

3) 1st LOCAL OSCILLATOR (LOCAL)
1st local oscillator is composed of TR(Q5), X-TAL(X1) and surround parts and following formular is applied for oscillator FL of (X1).

$$FL = \frac{FC-21.4}{2} \text{ (MHz)}$$

FC=CARRIER FREQUENCY(MHz)

Basic oscillator frequency is determined by 3rd OVERTONE TYPE X-TAL(X1) and it is tuned as 2 times frequency by (L4) Sync circuit and its micro control is available at (C41) for the frequency.

4) FILTER BETWEEN 1st CONVERTING CIRCUIT AND 1st INTERMEDIATE FREQUENCY
1st conversion circuit and frequency filter are passed through antenna, RF amplifier and BPF and mixing the signal from 1st local oscillator and inputted receiving signal and then converts to 1st intermediate frequency of 21.4MHz. 1st intermediate frequency filter selects only 21.4MHz signal in various frequency factors which was produced during the mixing in the 1st mixer and then it is approved 1st intermediate frequency amplifier and other zamming signals except approved signal are excluded. This filter is 2 POLE MCF FILTER and sit has 15KHz band.

5) 2nd PART OSCILLATOR
2nd part oscillator is composed of capacitor(C30),(31) & X-TAL(X2) and it generates 20.945MHz of 2nd part oscillator frequency.

6) DEMODULATIOR PART (UI)

The signal removing unnecessary wave by F2 and 2nd part oscillator frequency(20.945MHz) given by X-TAL(X2) are mixed by 2nd converting circuit in inside of IC and then 455KHz of intermediate frequency is made in 1st intermediate frequency. 2nd intermediate frequency is suppressed by F3 intermediate filter and only 455KHz of intermediate frequency is passed and it is approved inside of IC. Amplified 455KHz of intermediate frequency and output restored data through QUADATURE wave detector or DISCI. Restored data output is approved to LOWPASS FILTER and filtered data out put is passed through IC inside COMPARATOR again and it is converted to old wave type and it is approved LOGIC DECODER IC DATA input group. FM wave detector IC(U6) has voltage regulator and it is controlled ON/OFF position by receiver ENABLE signal sent from battery voltage which was approved externally, therefore battery span of life can be extended due to reduction of electric power consumption of receiving each part.

5.2.2 CONTROL PART (LOGIC)

1) DECODER IC PART(IC102)

Using electric power source of decoder IC is 3V ±0.5V and it is connected to MPU(IC100) and received data from RF and stored data in EEPROM(IC103) are compared. Restored data in receiving part is filtered by filter group inside decoder IC, and then it is decoded. If the decoded data is same as CAPCODE inside EEPROM IC, then this data is outputted to MPU. And also battery saving action data is outputted by RF ON/OFF control to extend span of life of battery.

2) MPU PART (IC100)

All functions of MERIT PAGER are performed by (IC100) MPU and the IC is operated at 3V power source and it is reset by reset signal produced by (IC 101:BH6111), and external clock of (430KHz~460KHz) from RC oscillator is used as main system and 32KHz from 32.768KHz oscillator circuit is operated as SUB clock.
MPU analyzes decoding data from IC decoder and display the message on LCD and controls warning sound, lamp and buzzer etc.

MERIT

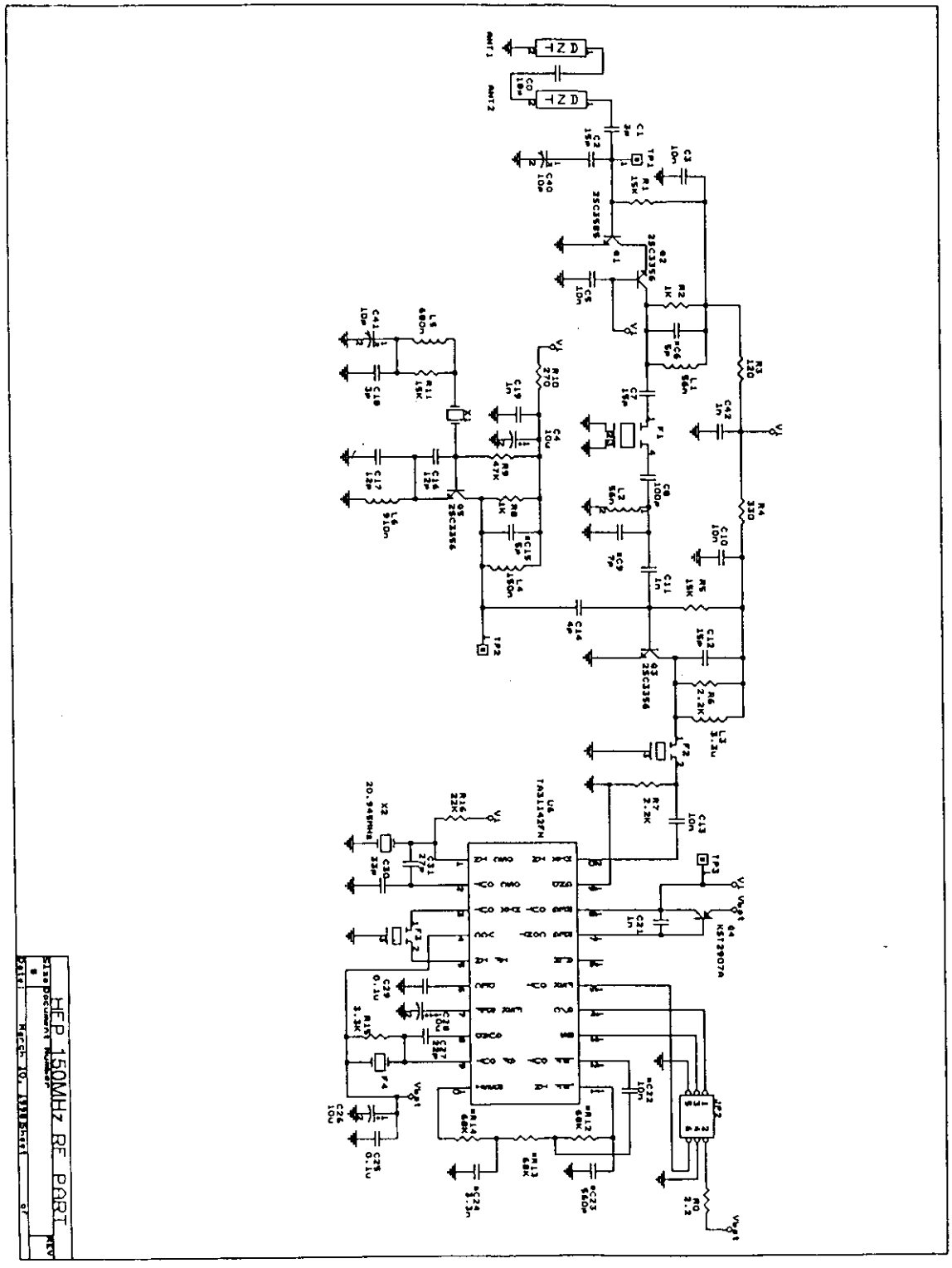
3) DC-DC CONVERTER PART (IC 101)
Poser is supplied from 1.5V/DC of external battery and 3V power is supplied to 3V/DC of stable voltage is required circuit. (3V converting part is in IC101)

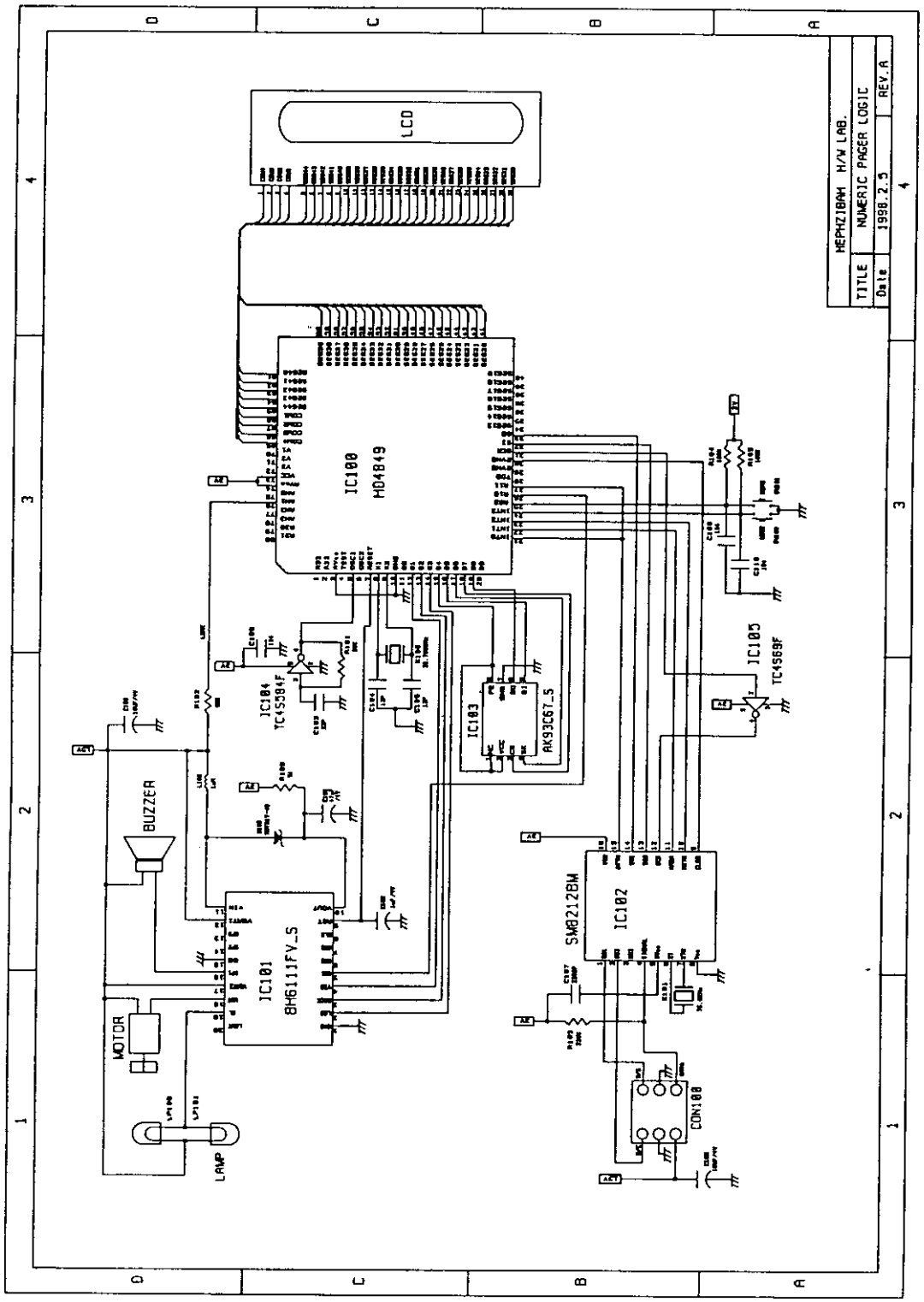
4) EEPROM PART (IC 103)
EEPROM is composed of 1K BIT's SERIAL IN/OUT and direct writing to MPU is available at minimum 2.4V.
CAP CPDE, PAGER's OPTION DATA & CAPCODE for DISPLAY and BACK-UP message etc are stored.

5) LCD PART
LCD is drived by MPU(IC100) and 1/4 of 3V/DC operation voltage DUTY, 7 SEGMENT 12 DIGIT of 1/3 BIAS.

6) DRIVER PART
Driver part is divided into motor, lamp and buzzer part and it is operated by data control as driver IC in the MPU.

7. CIRCUIT DRAWING




LCD
IC100
HD4849
IC101
BH6111FV_S
IC102
SW82128M
IC103
AK93C67_S
IC104
TC4S584F
IC105
TC4S69F
CON100
BUZZER
MOTOR
LAMP
MEPHISTO H/W LAB.
TITLE
NUMERIC PAGER LOGIC
Date
1998.2.5
REV.A