MT6630QA Data Sheet

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Document Revision History

Revision	Date	Author	Description
1.00	2013/11/05	Loris Li	Initial version
1.01	2013/11/13	Loris Li	1. Update list of table and list of figure 2. Update figure.13
1.02	2013/11/22	Dyck Lai	Add QFN PIN & Package information
1.04	2014/02/05	Dyck Lai	Fix Fig.9 mismatch : VBAT : 2.97V~4.5V
1.06	2014/03/28	Dyck Lai	Update ***Table 31,32,33,34,38,40,42,43,44,45,46,47,48,49***
1.07	2014/04/03	Dyck Lai	1. Add ***Figure 9. MT6630QA QFN POD (c)*** 2. Update ***6.5 Current Consumption : Table 49,50,52***
1.08	2014/04/22	Dyck Lai	1. Revise Figure 1. 2. Update Figure 2.6 3. Revise AVDD33/AVSS33 as AVDD35/AVSS35 4. Remove Chapter 4.5.3
1.09	2014/07/30	Dyck Lai	1. Update ***Figure 1.*** 2. Sec 2.3 : WLCSP-113
1.10	2014/08/08	Dyck Lai	1. Add impedance info to ***Table 1*** & ***Table 2***
1.11	2014/09/15	Dyck Lai	1. Revise 6.1.1 note
1.12	2015/03/24	Dyck Lai	1. Add power-on sequence waveform as ***Figure 10.*** 2. Fix package size typo in chapter 1.2
1.13	2015/12/21	Chun-Yi Wu	1. Fix QFN pin number error in chapter 2.1.2
1.14	2017/02/25	Chun-Yi Wu	1. Fix I2S_DATA_IN Typo in chapter 2.1.1 2. Refine from MT6630QA 1.14 version 3. Remove WLCSP related information 4. Change BT power to 8dBm

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1 System Overview

1.1 General Description

MediaTek MT6630QA is the worldwide first 5-in-1 wireless connectivity combo chipset supporting 802.11a/b/g/n/ac 1T1R WLAN function at 20/40/80MHz bandwidth, Bluetooth v4.1+HS, ANT/ANT+, multi-GNSS (Five systems: GPS, Glonass, Beidou, Galileo and QZSS) and FM Transceiver. By integrating the five advanced radio technologies, MT6630QA SoC delivers the system designers from the complexity and efforts. To prevent the crosstalk among different radios, MT6630QA implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. To reduce the external components, MT6630QA integrates most RF blocks such as PA, LNA, T/R switch etc. It also supports single antenna sharing among 5GHz WLAN, 2.4 GHz Bluetooth/ANT+ and WLAN, and 1.575 GHz GPS. For mobile devices, including mobile phones and media tablets, MT6630QA can simultaneously transmit and receive voice, data, and audio/video without interferences. To reduce the current consumption and offer high throughput on WLAN, MT6630QA equips 802.11ac function for over 200Mbps data rate. Either Bluetooth or ANT-enabled devices, MT6630QA can communicate with those Wireless PAN products to fulfill user expectations as much as possible. The multi-GNSS capability of MT6630QA also improves the TTFF (Time To First-Fix) and less dead zones which single satellite signal might be too weak. QFN type supports the normal PCB with less cost.

1.2 Features

- Embedded single core 32-bit RISC CPU for better system level management between sub-systems
- Supports single 2.4GHz antenna for Bluetooth, ANT+ and WLAN
- Supports single tri-band antenna for WLAN (2.4GHz and 5GHz), Bluetooth, ANT+ and GNSS
- Self calibration to reduce test time in manufacturing line
- Supports single TCXO for all radios
- Integrated switching regulator enables direct connection to battery
- Best-in-class current consumption performance
- Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account of protocol exchange sequence, frequency, etc.)
- Intelligent BT/WLAN 2.4GHz and LTE coexistence mechanism, both proprietary and BT SIG defined specification
- Data Interfaces: SDIO3.0, UART
- Packages: QFN (7x7 mm2)

WLAN

- Dual-band (2.4/5GHz) single stream 802.11 a/b/g/n/ac MAC/BB/RF SoC, 20/40/80MHz bandwidth, MCS0~9 (256-QAM)
- Supports worldwide available 5GHz channels, including new bands in the US and China (5925MHz)

- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control and DFS radar pulse detection
- 802.11i enhanced security
- 802.11j WLAN 4.9 to 5GHz operation in Japan
- 802.11k radio resource measurement
- 802.11r fast handoff for AP roaming
- 802.11v Timing Measurement
- 802.11w protected management frames
- Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (Hardware)
- QoS: WFA WMM, WMM PS
- Supports 802.11n optional features: LDPC, STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
- Supports 802.11ac LDPC Tx/Rx, STBC Rx, 4T1R beamformee, MU-MIMO Rx, WoWLAN
- Supports MediaTek proprietary low power Green AP mode for portable hotspot operation
- Auto rate control for optimizing the signal range and performance
- Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
- Supports WFA Passpoint (HotSpot 2.0)
- Supports EAP-TLS / EAP-TTLS / EAP-PEAP / EAP-SIM / EAP-AKA / EAP-AKA'
- Interface: SDIO 3.0 (4-bit & 1-bit, DDR50 and SDR104 modes)
- Integrated 2.4GHz PA with max 23dBm output power and 5GHz PA max 18.5dBm
  - Rx sensitivity at 11n HT20 MCS7 mode and -62dBm 5GHz Rx sensitivity at 11ac VHT80 MCS9 mode
- Supports external 5GHz PA path and external 2.4/5GHz LNA paths
- Supports 32 multicast address filters and TCP/UDP/IP checksum offload
- Per packet Tx power control

Bluetooth

- Bluetooth specification v2.1+EDR, 3.0+HS, v4.1+HS compliant
- Integrated PA with 8dBm (class 1) transmit power and switch
- Rx sensitivity: GFSK -94dBm, DQPSK -95dBm, 8-DPSK -89dBm, BLE -96dBm
- HCI over high speed (4Mbps) UART(H4), and SDIO 3.0
- Best-in-class BT/Wi-Fi coexistence performance
- Up to 4 piconets simultaneously with background inquiry/page scan
- Supports BT legacy, BLE and ANT+ scatternet
- Packet loss concealment (PLC) function for better voice quality
- Low-power scan function to reduce the power consumption in scan modes
- Supports Wideband speech (16KHz sampling rate)
  - SBC encode include mono and stereo
  - SBC decode only support mono
  - mSBC support in controller
- Supports secure connection with AES128 and ECC256
- Supports LTE coexistence enhanced features: Clock nudge and generalized interlace scan
- Supports FM over BT A2DP

ANT/ANT+

- The wireless protocol standard for sport and fitness monitors
- Supports different profiles for various applications: sport & fitness, health & Wellness, recreational activity, transportation, and information management etc.

GNSS

- Supports GPS/Glonass/Beidou/Galileo/QZSS tri-band reception concurrently
- Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
- Best-in-class sensitivity performance
  - -165 dBm tracking sensitivity
  - -163 dBm hot start sensitivity
  - -148 dBm cold start sensitivity
  - -151 dBm warm start sensitivity
- AGPS sensitivity can reach 8dB design margin over 3GPP
- Full A-GPS capability (E911/SUPL/EPO/HotStill), EPO and HotStill are MediaTek proprietary designs
- Active interference cancellation for up to 12 in-band tones
- Low-power operational modes for mobile phone and tablet
- Supports TCXO
- 5Hz update rate

FM

- Supports both FM receiving and transmitting capabilities
- 65-108MHz with 50kHz step
- Supports RDS/RBDS Tx and Rx
- Digital stereo modulator/demodulator
- Digital audio interface (I2S) and analog audio output supported
- Fast seek time 30ms/channel
- Stereo noise reduction
- Output power control of FM Tx is from 90dBuV to 120dBuV
- Audio sensitivity 2dBμVemf ((S+N)/N=26dB), RDS sensitivity 18dBuVemf
- Audio SINAD 60dB
- Anti-jamming supported
- Built-in capacitor bank and internal resonation calibration system for short antenna
- Supports UART and SDIO 3.0 interface
- Supports FM over Bluetooth to reduce system current consumption

1.3 Applications

- Smartphone applications
- Media Tablet applications
- Mobile Internet Device (MID) applications
- Portable Navigation Device (PND) applications

- Portable Media Player (PMP) applications
- Portable gaming devices
- PC/NB and Ultrabook applications

1.4 Block Diagram

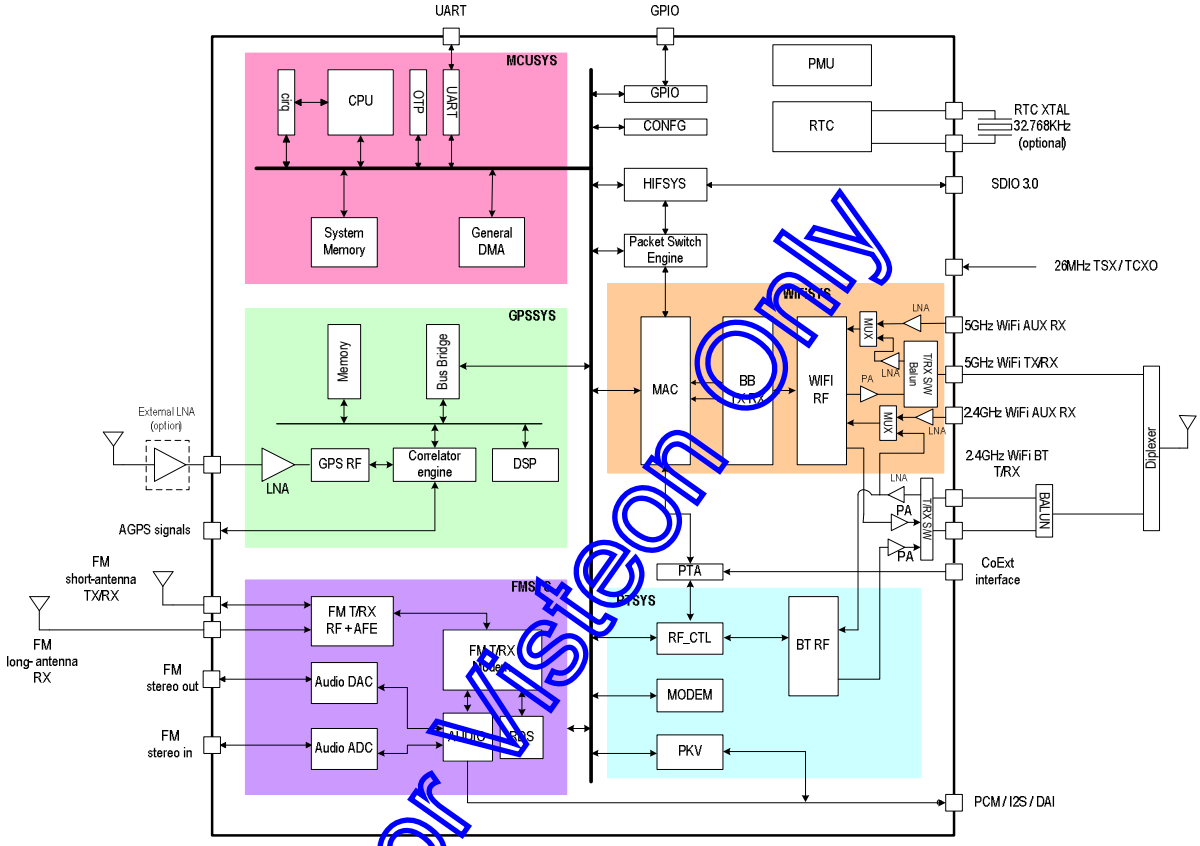

Figure 1. MT6630QA block diagram

2 Product Description

2.1 Pin Description

2.1.1 MT6630QA QFN

There are total 56 pins in QFN package.

Symbol	QFN Pin	Power domain	Description	PU/PD	Impedance	I/O
Power ground pin						
DVDD	5		1.2V core power	NA	NA	VDD
DVDD	40		1.2V core power	NA	NA	VDD
DVDDIO	35		I/O power	NA	NA	VDD
DVDDIO_SDIO	29		SDIO I/O power	NA	NA	VDD
PMU						
PMUEN	13		PMU enable	NA	50	I
VREF	14		Reference bandgap voltage	NA	NA	O
AVDD45_MISC	15		VBAT for internal circuit	NA	NA	VDD
AVDD25_V2P5NA	16		Internal 2.5V power	NA	NA	VDD
LX1	18		Switching node	NA	50	I/O
LX2	21		Switching node	NA	50	I/O
AVDD45_SMPS	17		Battery voltage	NA	NA	VDD
AVSS45_SMPS	19		Switching regulator ground	NA	NA	VSS
VOUT_VCORE	22		1.2V core power output	NA	NA	O
VOUT_VRF	20		1.55V RF power output	NA	NA	O
AVDD28_ALDO	12		2.8V ALDO output	NA	NA	O
AUXIN	10		ADC input	NA	50	I
AVSS28_ADC	11		ADC ground	NA	NA	VSS
RTC						
RTCCLK	7	VCCRTC	RTC 32kHz clock input	NA	50	Analog/I
RTCCLK_O	8	VCCRTC	RTC 32kHz clock output	NA	50	Analog/O
AVDD28_32K	9		RTC power	NA	NA	VDD
Analog						

GPS_RF_INP	56		GPS RF input	NA	50	RF/I
AVSS_FM_LANT_N	54		Ground	NA	50	VSS
FM_LANT_P	53		Long antenna FM RF port	NA	50	RF I/O
FM_LOUT	51		FM audio output	NA	50	Analog/ O
		DVDDIO	GPIO2: GPIO2 in/out	SW	50	I/O
FM_ROUT	52		FM audio output	NA	50	Analog/ O
		DVDDIO	GPIO3: GPIO3 in/out	SW	50	I/O
AVDD33_FM	55		FM power	NA	NA	VDD
WB_RFION_G	44		WiFi 2G/BT RF port	NA	50	RF I/O
WB_RFIOP_G	45		WiFi 2G/BT RF port	NA	50	RF I/O
AVDD15_WBT_AFE	42		WiFi 2G/BT power	NA	NA	VDD
AVDD15_WBT_TRX	43			NA	NA	VDD
AVDD33_WBT_TX	46		WiFi 5G power	NA	NA	VDD
AVDD33_AC_MOD	47			NA	NA	VDD
AVDD33_AC_PA	48			NA	NA	VDD
AC_RFIO_A	49		WiFi 5G RF port	NA	50	RF I/O
AVDD15_RF	3		RF power	NA	NA	VDD
XO	2		XTAL input	NA	10K//5pF	Analog/I
AVDD28_XO	1		XTAL power	NA	NA	VDD
			Digital			
SYSRST_B	41	DVDDIO	External system reset active low	PU	75K	I
OSC_EN	4	DVDDIO	OSC_EN: OSC enable in clock daisy chain	NA/S W	Hi-Z	O
			GPIO0: GPIO0 in/out			I/O
SDIO_CLK	25	DVDDIO_SDIO	SDIO_CLK: SDIO interface	NA/S W	Hi-Z	I
			GPIO3: GPIO3 in/out			I/O
SDIO_CMD	27	DVDDIO_SDIO	SD_CMD: SDIO interface	NA/S W	Hi-Z	I/O
			GPIO4: GPIO4 in/out			I/O
SDIO_DAT3	28	DVDDIO_SDIO	SDIO_DAT3: SDIO interface	NA/S W	Hi-Z	I/O

			GPIO5: GPIO5 in/out			I/O
SDIO_DAT2	26	DVDDIO_SDIO	SDIO_DAT2: SDIO interface	NA/SW	Hi-Z	I/O
			GPIO6: GPIO6 in/out			I/O
SDIO_DAT1	24	DVDDIO_SDIO	SDIO_DAT1: SDIO interface	NA/SW	Hi-Z	I/O
			GPIO7: GPIO7 in/out			I/O
SDIO_DAT0	23	DVDDIO_SDIO	SDIO_DAT0: SDIO interface	NA/SW	Hi-Z	I/O
			GPIO8: GPIO8 in/out			I/O
UART_RX	38	DVDDIO	UART_RXD: UART RX data	PU/SW	75K	I
			GPIO9: GPIO9 in/out			I/O
UART_TX	37	DVDDIO	UART_TXD: UART TX data	PU/SW	75K	O
			Strap: Common interface selection			I
			GPIO10: GPIO10 in/out			I/O
UART_CTS	36	DVDDIO	UART_CTS: UART flow control	PU/SW	75K	I
			GPIO12: GPIO12 in/out			I/O
PCM_CLK	32	DVDDIO	PCM_CLK: PCM interface clock	PD/SW	75K	I/O
			I2S_CLK: FM I2S interface clock			I/O
			DAI_CLK: digital audio interface clock			I
			GPIO13: GPIO13 in/out			I/O
PCM_SYNC	33	DVDDIO	PCM_SYNC: PCM interface sync	PD/SW	75K	I/O
			I2S_WS: FM I2S interface WS			I/O
			DAI_SYNC: digital audio interface sync			I
			GPIO14: GPIO14 in/out			I/O
PCM_OUT	30	DVDDIO	PCM_OUT: PCM interface	PD/SW	75K	O

			output data			
			I2S_DATA_OUT : I2S interface output data			O
			DAI_TX: digital audio interface TX data			O
			GPIO15: GPIO15 in/out			I/O
PCM_IN	31	DVDDIO	PCM_IN: PCM interface input data	PD/SW	75K	I
			I2S_DATA_IN: I2S interface input data			I
			DAI_RX: digital audio interface RX data			I
			GPIO16: GPIO16 in/out			I/O
AGPS_SYNC	6	DVDDIO	SYNC: AGPS SYNC	PD/SW	75K	I
			GPIO17: GPIO17 in/out			I/O
I2S_DATA_OUT	34	DVDDIO	I2S_DATA_OUT: FM I2S data output	NA/SW	Hi-Z	O
			I2S_DATA: FM I2S data			I/O
			PCM2OUT: PCM2 synchronous data output			O
			GPIO20: GPIO20 in/out			I/O
			Strap: test mode selection			I
BGF_INT_B	39	DVDDIO	ALL_INT_B: All interrupt to host	NA/SW	Hi-Z	O
			BGF_INT_B: BT, GPS & FM host interrupt			O
			GPIO2: GPIO2 in/out			I/O
GPIO0	50	DVDDIO	WIFI_INT_B: WiFi interrupt to host	NA/SW	Hi-Z	O
			ALL_INT_B: All interrupt to host			O
			GPIO1: GPIO1 in/out			I/O

Table 1. MT6630QA QFN Pin descriptions

2.1.2 Strapping table

UART_TX	Description
0	SDIO
1	UART

Table 2. Common interface selection

2.2 Package Information

2.2.1 MT6630QA QFN Packaging

DDDD: DATE CODE
&&&&: sub-contractor code
XXXXX: LOT NO.
“.”: Pin #1 dot

Figure 2. MT6630QA QFN top marking

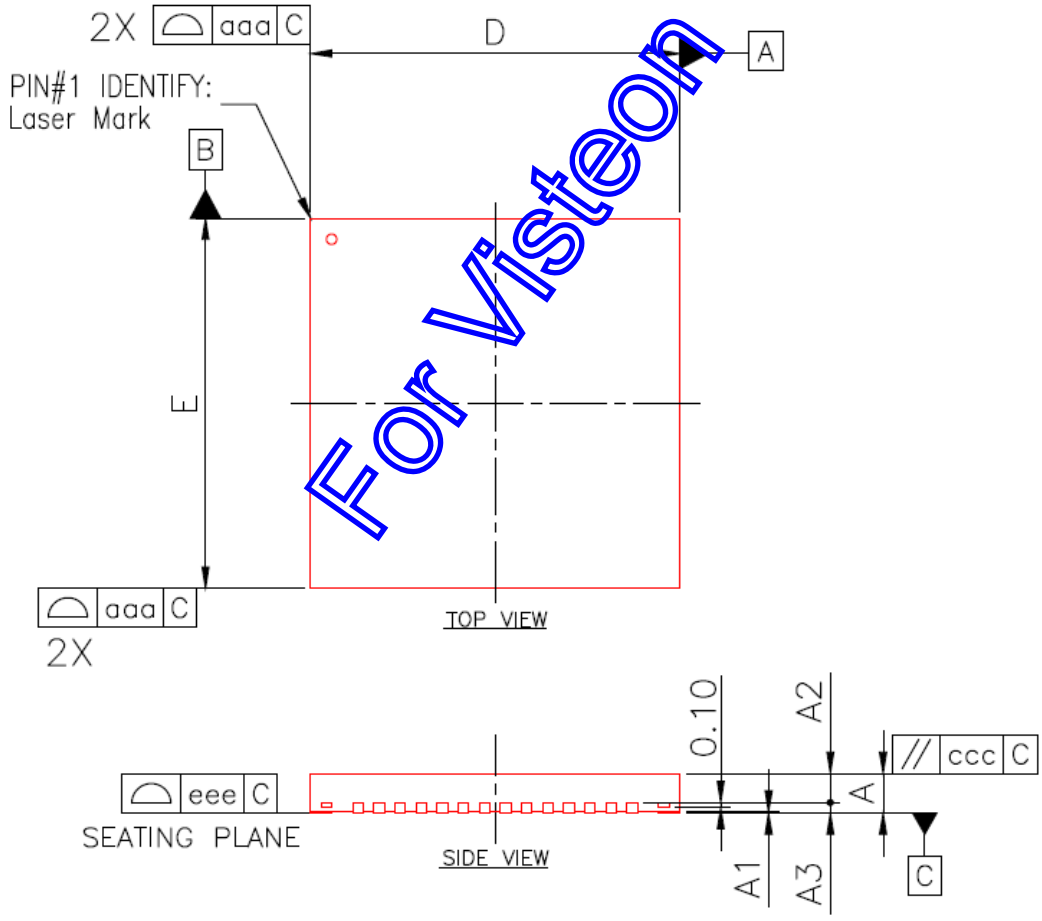

Figure 3. MT6630QA QFN POD (a)

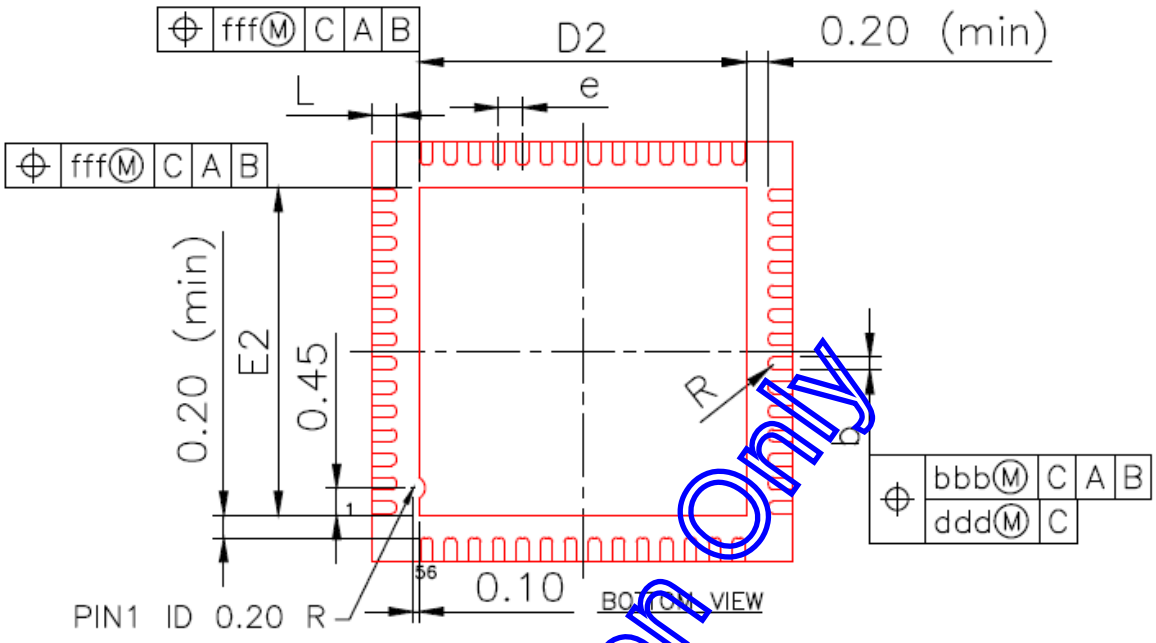

Figure 4. MT6630QA QFN POD (b)

Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	6.90	7.00	7.10
	Y	E	6.90	7.00	7.10
E-PAD size	X	D2	5.35	5.45	5.55
	Y	E2	5.35	5.45	5.55
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	0.125
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Parallelism		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

Figure 5. MT6630QA QFN POD (c)

Pin localtion:

PAD NAME	Bonding	PAD NAME	Bonding	PAD NAME	Bonding	PAD NAME	Bonding
AVDD15_XO	1	AVDD45_MISC	15	DVDDIO_SDIO	29	AVDD15_WBT_TRX	43
PAD_XO	2	AVDD25_V2P5NA	16	PAD_PCM_OUT	30	PAD_WB_RFION_G	44
AVDD15_RF	3	AVDD45_SMPS	17	PAD_PCM_IN	31	PAD_WB_RFIOP_G	45
PAD_OSC_EN	4	PAD_LX1	18	PAD_PCM_CLK	32	AVDD33_WBT_TX	46
DVDD	5	AVSS45_SMPS	19	PAD_PCM_SYNC	33	AVDD33_AC_MOD	47
PAD_AGPS_SYNC	6	PAD_VOUT_VRF	20	PAD_I2S_DATA_OUT	34	AVDD33_AC_PA	48
PAD_RTCCLK	7	PAD_LX2	21	DVDDIO	35	PAD_AC_RFIO_A	49
PAD_RTCCLK_O	8	PAD_VOUT_VCORE	22	PAD_UART_CTS	36	PAD_GPIO0	50
AVDD28_32K	9	PAD_SDIO_DAT0	23	PAD_UART_TX	37	PAD_FM_LOUT	51
PAD_AUXIN	10	PAD_SDIO_DAT1	24	PAD_UART_RX	38	PAD_FM_ROUT	52
AVSS28_AUXADC	11	PAD_SDIO_CLK	25	PAD_BGF_INT_B	39	PAD_FM_LANT_P	53
AVDD28_ALDO	12	PAD_SDIO_DAT2	26	DVDD	40	AVSS_FM_LANT_N	54
PAD_PMUEN	13	PAD_SDIO_CMD	27	PAD_SYSRST_B	41	AVDD33_FM	55
PAD_VREF	14	PAD_SDIO_DAT3	28	AVDD15_WBT_AFE	42	PAD_GPS_RF_INP	56

2.3 Ordering guide

Model	Temperature Range	Package	Shipping Medium
MT6630QN	-40°C to +85°C	QFN-56	Tape

2.4 Storage Condition

1. Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   a. Mounted within 168 hours at factory condition of 30°C/60% RH, or
   b. Stored at 20% RH.
3. Devices require baking before mounting, if
   a. Humidity Indicator Card is > 20% when read at 23°C ± 5°C, or
   b. Item 2 is not met.
4. If baking is required, device may be baked for
   a. 192 hours at 40°C+ 5°C/ - 0°C and < 5% RH for low temperature device containers, or
   b. 24 hours at 125°C+ 5°C/ - 0°C for high temperature device containers.

3 Electrical Characteristics

3.1 PMU Description

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), Single-Input-Dual-Output (SIDO) buck converter and reference band-gap circuit.

The PMU integrates two LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

The input voltage of the buck converter ranges from 2.97V to 4.5V. One of its outputs is 1.55V to feeds into the input power of the RF circuit and the other outputs are 1.2V for all digital circuits.

There is one PA LDO for WLAN with output voltage of 3.5V. There is also one dedicated LDO which provides 2.8V output voltage for RF blocks, and TCXO.

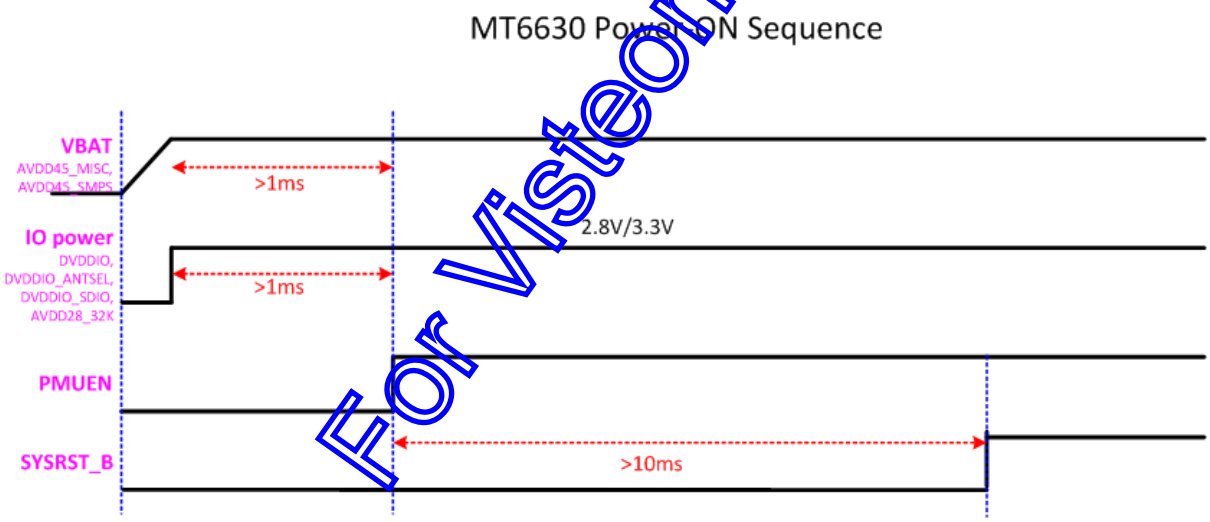

Figure 6. MT6630QA Power-ON sequence

3.1.1 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below 2.15V threshold. It ensures that MT6630QA is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

3.1.2 WF_PA_LDO

WF_PA_LDO converts the battery input to a 3.5V supply for WiFi RF PA circuits. It is optimized for high-performance including high transient response and adequate quiescent current.

3.1.3 ALDO

ALDO converts voltage from battery input to 2.8V output. This LDO supply TCXO power, internal AUXADC and PLL.

3.1.4 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 280mA (max.) with 1.55V output voltage for VRF and 420mA (max) with 1.2V output voltage for VCORE simultaneously. It supplies power for the RF circuitry and digital circuitry. The buck converter is optimized for high-efficiency, low-EMI, and low quiescent current.

3.1.5 PMU Power Connection

Power connections are suggested as shown in Fig.6. The voltage source for RF and digital core is from the DC-DC converter. The voltage source of PA and TCXO/XTAL LDOs is from VBAT directly. The 1.8V or 2.8V IO voltages are from the host side.

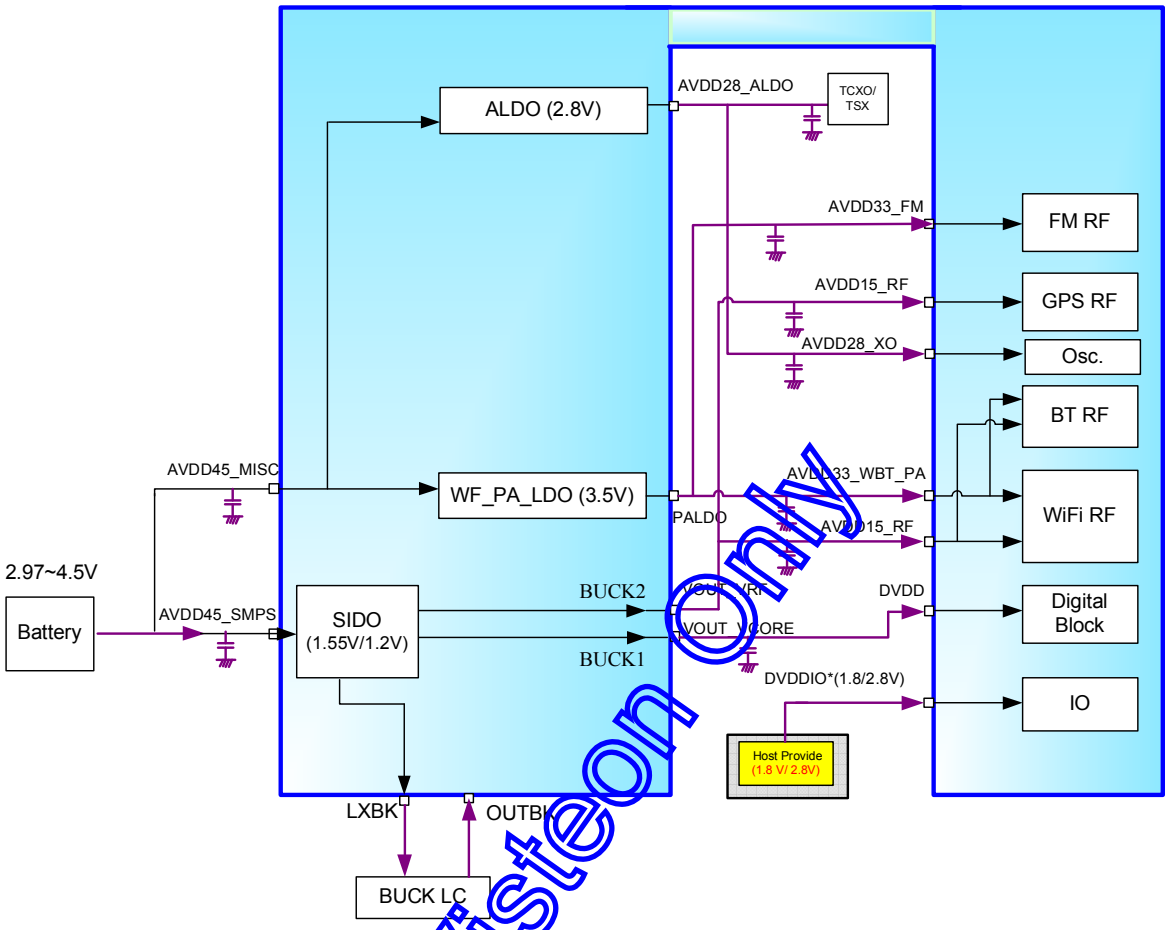

Figure 7. Normal mode power connection

3.2 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
DVDDIO	1.8V/2.8V digital IO power supply	-0.3 to 3.6	V
DVDDIO_SDIO	1.8V or 2.8V SDIO digital IO power supply	-0.3 to 3.6	V
DVDD	Digital 1.2V power supply	-0.3 to 1.32	V
AVDD28_32K	RTC power supply	-0.3 to 3.6	V
AVDD28_XO	Internal X'tal Oscillator circuit power supply	-0.3 to 3.08	V
AVDD33_*	WPA power supply FM circuit power supply	-0.3 to 3.6	V
AVDD15_*	RF power supply	-0.3 to 1.8	V
AVDD45_SMPS	BUCK power supply	-0.3 to 4.5	V
AVDD45_MISC	Power-on circuit supply	-0.3 to 4.5	V
T_{stg}	Storage temperature	-60 to +150	°C
T_a	Operating temperature	-40 to +85	°C

Table 3. Absolute maximum ratings

3.3 Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDDIO	2.8V digital power supply	2.0	2.8	3.3	V
DVDDIO_SDIO	1.8V digital power supply	1.6	1.8	2.0	V
DVDD	Digital core power supply	1.08	1.2	1.32	V
AVDD28_32K	RTC power supply	2.52	2.8	3.08	V
		1.62	1.8	1.98	V
AVDD28_XO	Internal X'tal Oscillator circuit power supply	2.52	2.8	3.08	
AVDD33_*	WPA power supply FM circuit power supply	3.25	3.5	3.6	V
AVDD15_*	RF power supply	1.475	1.55	1.65	V
AVDD45_SMPS	BUCK power supply	2.97	3.8	4.5	V
AVDD45_MISC	Power-on circuit supply	2.5	3.8	4.5	V
T_j	Commercial junction operating temperature	0	25	115	°C
	Industry junction operating temperature	-40	25	125	°C
T_a	Operation temperature	-40	25	85	°C
T_{stg}	Storage temperature	-60	25	150	°C

Table 4. Recommended operating range

3.4 PMU Electrical Characteristics

3.4.1 PMU Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
PMU_EN = 0: Shut down current					
2.5V < VBAT < 4.5V	VBAT = 3.8V		20	25	μA
4.5V < VBAT	VBAT = 4.5V		25	35	μA
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold			2.25		V
Under voltage falling threshold			2.15		V
PMU_EN Voltage Level					
High voltage		1.4			V
Low voltage				1	V
Thermal Shutdown					
Threshold			150		°C
Hysteresis			40		°C
LDO Enable Response Time			250		μs

Parameter	Conditions	Min.	Typ.	Max.	Unit
SMPS Voltage for VRF					
Input voltage		2.97	3.8	4.5	V
Output voltage (VRF)		1.475	1.55	1.65	V
Output current (Imax)				280	mA
Quiescent current			80		uA
Line regulation	@no load			1	%
Load regulation	1mA~full load			0.05	mV/mA
PWM mode switching frequency			1.5		MHz
PWM mode ripple voltage	Static load		20		mV
Burst mode ripple voltage	Static load		40		mV
PFM/PWM mode switching condition	VBAT = 3.8V		15		mA
Efficiency (PWM)			84		%
Efficiency (PFM)			73		%
SMPS Voltage for Vcore					
Input voltage		2.97	3.8	4.5	V
Output voltage (Vcore)		0.8	1.2	1.3	V
Output current (Imax)				420	mA
Quiescent current			80		uA
Line regulation	@no load			1	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
Load regulation	1mA~full load			0.05	mV/mA
PWM mode switching frequency			1.5		MHz
PWM mode ripple voltage	Static load		20		mV
Burst mode ripple voltage	Static load		40		mV
PFM/PWM mode switching condition	VBAT = 3.8V		15		mA
Efficiency (PWM)			82		%
Efficiency (PFM)			72		%
WLAN PA Voltage					
Input voltage		2.97	3.8	4.5	V
Output voltage (VWIFI_PALDO)		3.25	3.5	3.6	V
Output current (Imax)				450	mA
Quiescent current			100		uA
Line regulation				35	mV
Load regulation	1mA ~ Imax (full-load)			35	mV
Output noise voltage	f = 10Hz to 80kHz			500	uVrms
Drop-out voltage	0.5*Imax		250		mV
	1*Imax		350		mV
Start-up time				240	us
External output capacitor			4.2 (2.2+1+1)		uF
ALDO Voltage					
Input voltage		2.97	3.8	4.5	V
Output voltage (ALDO)		2.66	2.8	2.94	V
Output current (Imax)				30	mA
Quiescent current			42		uA
Line regulation				1	%
Load regulation	1mA ~ Imax (full-load)			1	%
Output noise voltage	f = 10Hz to 80kHz		60		uVrms
Drop-out voltage	0.5*Imax		250		mV
	1*Imax		350		mV
Start-up time				240	us
External output capacitor			1		uF

Table 5. PMU characteristics

3.4.2 PMU Summary List

Item	LDO/Switcher	Voltage	Current	Description
1	SMPS(VRF)	1.55V	280mA	Buck output

Item	LDO/Switcher	Voltage	Current	Description
2	SMPS(Vcore)	1.2V	420mA	Buck output
3	WFLDO	3.5V	450mA	WLAN PA LDO
4	ALDO	2.8V	30mA	ALDO

Table 6. PMU summary list

Note: All the characteristic values are guaranteed at room temperature (25°C).

3.5 XOSC32

3.5.1 Block Description

The low-power 32-kHz crystal oscillator, XOSC32, is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors, as shown in the figure below.

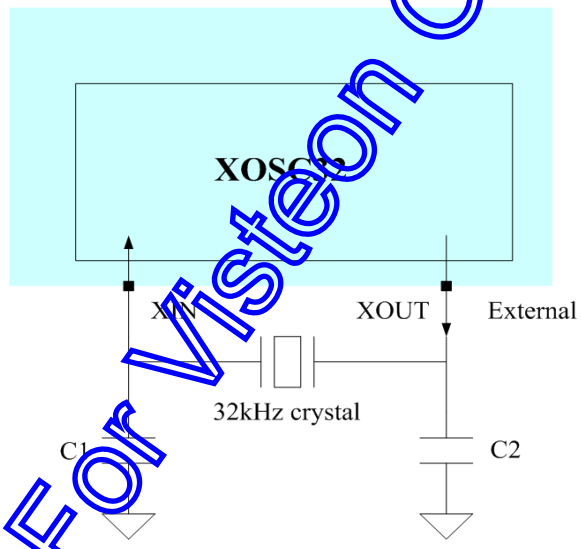

Figure 8. Block diagram of XOSC32

3.5.2 Functional Specifications of XOSC32

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCRTC	Analog power supply	1.62		3.08	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle		50		%
	Current consumption		5		µA

Table 7. Functional specifications of XOSC32

3.5.3 Recommendations for Crystal Parameters for XOSC32

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance			1.6	pF
CL[1]	Load capacitance	6		12.5	pF

Table 8. Recommended parameters of the 32 kHz crystal

3.6 IO PAD DC Electrical Characteristics

3.6.1 For 3.3 Volts Operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		1.08	1.2	1.32	V
VDDIO	Supply voltage of IO power		2.97	3.3	3.63	V
V_{IL}	Input logic low voltage	LVTTL	-0.3	-	0.8	V
V_{IH}	Input logic high voltage	LVTTL	2.0	-	VDDIO+0.3	V
V_{OL}	Output logic low voltage	VDDIO = min I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	Output logic high voltage	VDDIO = min I_{OH} = -2 mA	2.4	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	75	190	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 3.3 V	40	75	190	KΩ

Table 9. Pin descriptions

3.6.2 For 2.8 Volts Operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		1.08	1.2	1.32	V
VDDIO	Supply voltage of IO power		2.52	2.8	3.08	V

[1] CL is the parallel combination of C1 and C2 in the block diagram.

V_{IL}	Input logic low voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input logic high voltage	LVTTL	0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output logic low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output logic high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

Table 10. Pin descriptions

3.6.3 For 1.8 Volts Operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		1.08	1.2	1.32	V
VDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
V_{IL}	Input logic low voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input logic high voltage	LVTTL	0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output logic low voltage	VDDIO = min I_{OL} = -1.5 mA	-	-	0.15*VDDIO	V
V_{OH}	Output logic high voltage	VDDIO = min I_{OH} = -1.5 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	KΩ

Table 11. Pin descriptions

4 Functional Description

4.1 Clock Generation

There are two clock domains inside MT6630Q. One is the RF XTAL clock, and the other is the F32K (32.768 KHz) clock. The former supports the RF and the major MODEM functions, while the latter maintains the system operation in sleep mode.

There are two scenarios for F32K:

1. RTC exists: The RTC clock can be an external 32.768 KHz clock from the host, or it can use its own RTC XTAL.
2. Internal-32K: The required 32K clock is divided from XTAL through digital frequency divider.

MT6630QA can auto detect RTC existence during power-on sequence. If there's no RTC clock detect, then internal-32K is used.

The RF XTAL is shared by all the RF and modem sub-systems. MT6630QA has two options for this system clock source: One is for one-pin crystal input, and the other is for external clock source. The choice of which option used is brought down from host driver.

MT6630QA supports most widely used clock frequencies on mobile devices, including 19.2, 20, 24, 26, 38.4, 40 and 52MHz. In the case of RTC exists, the input frequencies can be automatically detected by the internal frequency meter. If internal 32K scenario is applied, host driver must bring down the frequency info to MT6630Q.

4.2 Chip Power Management

4.2.1 Power Saving Mode

There are 4 power modes that MT6630QA operates: Active mode, Standby mode, Idle mode and Sleep mode. The following are the brief introduction to each mode.

- **Power off:** Power supply is not enabled or PMU_EN is low.
- **Standby mode:** When MT6630QA is powered on, it first enters the Standby mode. In this mode, the system operates under the XTAL clock, while AHB bus is alive but PLL is still off.
- **Active mode:** It is defined as the state that RF circuit is enabled to transmit or receive data, and the entire system is under normal operation. PLL is active, and the AHB bus is alive.
- **Idle mode:** When the firmware finishes its task and starts to wait for the next hardware trigger, it forces the hardware to enter this mode. In this mode, part of the logic circuits, like MCU, will enter the low power mode. The RF circuits might still be operating in the Idle mode.

- **Sleep mode:** The baseband controller determines when to enter the Sleep mode to turn off most circuits of MT6630Q. All the RF, PLL circuits and XTAL are turned off. In the Sleep mode, the system can be awakened after the sleep time is expired or by an external wake-up signal from the host controller.

	Power off	Standby	Active	Idle	Sleep
RTC 32K	OFF	ON	ON	ON	ON
MCU PLL	OFF	OFF	ON	OFF	OFF
MCU clock	OFF	XTAL	MCU PLL	OFF	OFF
AHB Bus	OFF	ON	ON	ON	OFF
RF XTAL	OFF	ON	ON	ON	OFF

Table 12. Power state descriptions of power management

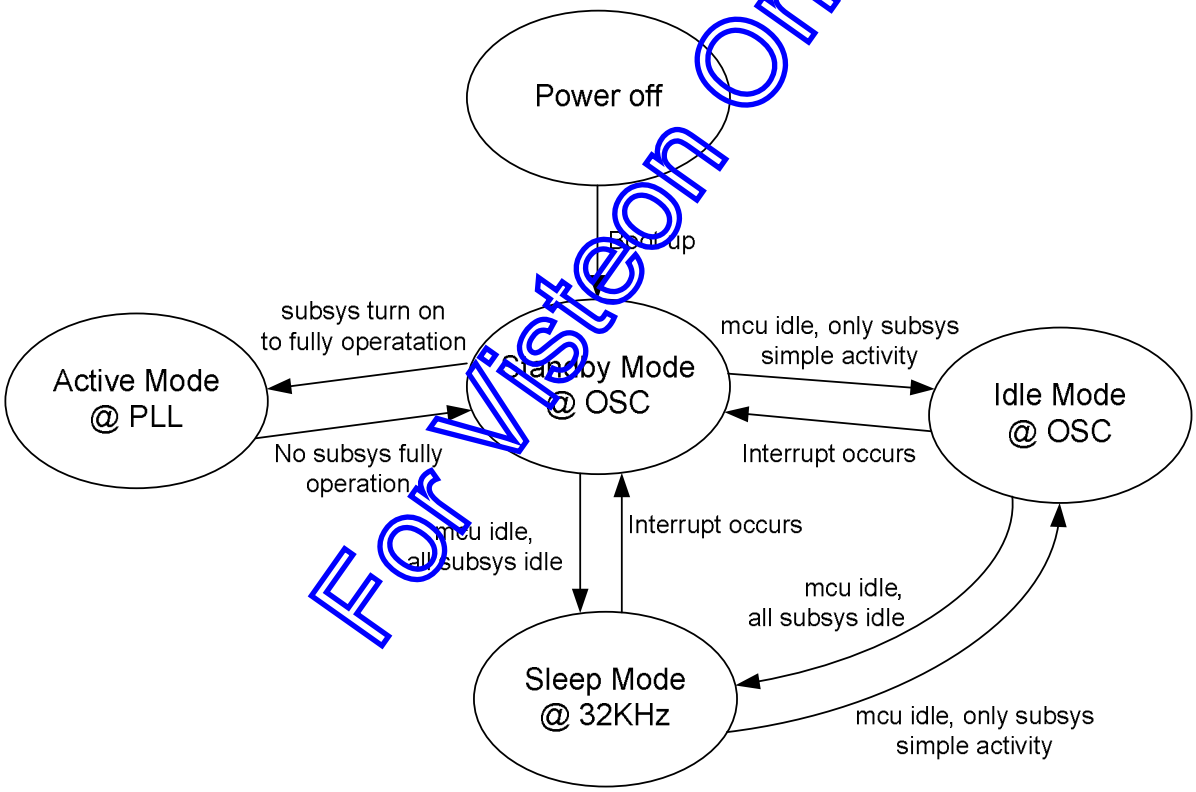

Figure 9. System power state machine

4.3 WLAN Subsystem

The MT6630QA WLAN is designed to support IEEE 802.11™ a/b/g/n/ac single stream with the state-of-the-art design techniques and process technology to achieve low-power consumption and high-throughput performance to address the requirement of mobile devices. The MT6630QA WLAN low-

power function adopts the innovative design techniques and optimized architecture which best utilizes the advanced process technology to reduce active and idle power and achieve extreme-low power consumption in the sleep state to extend the battery life. The MT6630QA WLAN TX A-MPDU function adopts the state-of-the-art design technique to maximize the throughput performance while achieving the best buffer utilization at low cost. Further, the MT6630QA WLAN also implements the highly sophisticated coexistence scheme to allow extremely collaborative WLAN and BT coexistence. As a result, the enhanced overall quality can be achieved for simultaneous voice, video and data transmission on a mobile device.

4.3.1 MAC Features

- 802.11 a/b/g/n/ac single-stream
- 802.11 d/e/h/i/j/k/r/w/v compatible
- 802.11n throughput: 45M/90Mbps at 20M/40MHz BW
- 802.11ac throughput: over 200Mbps at 80MHz BW (max data rate is 433.3Mbps)
- Hardware state machine controller for extreme low-power consumption
- WLAN/BT coexistence mechanisms:
  - WLAN supports time domain division (TDD) mode by scheduling WLAN/BT blocks for optimal distance with acceptable throughput
    - For periodic BT traffic, like SCO, WLAN supports the following enhancement.
      - WLAN schedules all traffic in BT idle period.
      - WLAN supports channel protection to prevent rate-down when BT is busy.
        - Channel protection by NAV reservation
        - Fast power saving
  - WLAN supports time domain division (TDD) mode by PTA (Packet Traffic Arbiter) with BT.
- 802.11n optional features
  - A-MPDU TX
    - Up to 8 simultaneous links
    - Up to 16 MPDUs A-MPDU
    - TX window size up to 24 (maximum)
    - MMSS full support (0~16 us)
    - Instantly releases the acknowledged MPDUs data buffer to achieve perfect data buffer utilization
    - Instant aggregation for not acknowledged retry MPDUs and outstanding MPDUs within SIFS to achieve A-MPDU burst for best throughput performance
    - BAR for life time out to help RX side re-ordering buffer early release
    - Auto rate control for range/performance optimization

    - TX power control by transmission rate
  - TXOP protection and truncation
  - Reverse direction
  - Link adaptation (MCS feedback)
  - PCO
  - RIFS TX/RX
  - PSMP
- 802.11ac optional features
  - TXOPPS RXDynamic BW
  - MU-MIMO RX
  - 80MHz bandwidth
  - Supports MCS9
  - Supports 2.4GHz VHT40 MCS9 operation
  - STBC RX
  - LDPC TX/RX
  - 802.11ac beamformee
- AP/STA/ad-hoc mode
- Repeater
- Concurrent network support
  - Compatible with Microsoft Windows 8.x
  - Compatible with Google Android 4.2.1 Jelly Bean and the after
- Windows 8.x features support
  - 1-sec Wi-Fi fast connection
  - D0 packet coalescing
  - WoWLAN/Wake packet detection
- Network list offloading (NLO) Up to 20 peers for Direct Link or ad-hoc mode
- 802.1H packet format translation
- TCP/UDP/IP checksum offload
- Up to 32 multicast addresses
- Rate adaption mechanism
- Hardware WAPI
- CCX5
- TX/RX on-the-fly encryption/ decryption
  - WEP, TKIP, AES-CCMP, WPI-SMS4, GCMP
  - Up to 16 pair-wise keyed peers for hotspot

- WFA Wi-Fi certification
  - WPA
  - WPA2
  - WMM
  - WMM PS
  - WPS 1.0 and 2.0
  - VoWiFi-Personal
  - VoWiFi-Enterprise
  - WiFi P2P
    - Group Owner Basic
    - Group Owner 11n
    - Group Client Basic
    - Coexistence of P2P and BT-over-WLAN
  - PMF
- Low power consumption
  - Sleep mode for power saving (with 32KHz clock calibration for timing sync)
  - Waked up host by specific packets (pattern filter)
  - ARP offload/NS offload/Group key rekey offload
    Network list offload
  - Low power beacon RX
- BT-over-WLAN
  - Supports QoS(WMM)
  - Supplicant of PSK engine
  - Coexistence of concurrent

4.3.2 PHY Features

- Supports 802.11b,11g,11n,11j, and11ac
- Supports 20,40 and 80MHz Channel Bandwidth
- Supports Legacy, Green-Field, Mixed-Mode, and Very-High Throughput packet format TX and RX
- Supports G-band VHT TX and RX
- Supports modulation-coding scheme up-to MCS9
- Supports Short GI
- Supports STBC RX
- Supports LDPC TX and RX
- Supports 4TX compressed BFee RX
- Supports 4TX MU-MIMO-RX
- Provides Clear Channel Assessment on primary and secondary channels

- Provides Payload Detection on primary and secondary channels
- Supports 5G Radar detection
- Supports Low-power RX schemes
- Supports Green-AP
- Supports Packet-on-packet protection
- Supports calibration and digital compensation to handle non-ideal CMOS RF effect
- Robust RX sensitivity for wider coverage range
- Supports External LNA
- Supports RX antenna diversity scheme
- High Resistance of Co-channel Bluetooth interference
- High Resistance of Co-channel narrow band interference
- High Resistance of WIFI Adjacent channel Interference
- High Resistance of WIFI Co-channel interference

4.4 Bluetooth Subsystem

4.4.1 Bluetooth Baseband Subsystem

The Bluetooth baseband subsystem of MT6630QA contains a baseband processor which supports timing control, bit stream processing, encryption, frequency hopping and modulation/demodulation. The baseband processor fulfills v2.1+EDR, BT3.0+HS, v4.0 BLE, v4.1+HS and ANT/ANT+ specifications. It also contains the voice codec, PTA/PTI, shared PCM interface controller, WLAN coexistence interface controller and a sleep mode controller. It also supports FM over BT and SCO over I2S function. MT6630QA Bluetooth enhances BT and BLE encryption with AES-128.

One hardware accelerator is added to implement packet loss concealment function. The packet loss concealment (PLC) function is used to improve the voice quality in a noisy environment. A low-power scan function, deep sleep mode function and pll idle mode function are implemented in MT6630QA to reduce the power consumption in the scan mode.

4.4.2 Bluetooth RF Subsystem

In the TX path of MT6630Q, the data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 8dBm power for class 1 operation.

MT6630QA uses a low IF receiver architecture. An image-rejecting mixer down-converts the RF signal to the IF with the LO from the synthesizer, which supports different clock frequencies as the reference clock described in section 4.1. The mixer output is then converted to digital signal, down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.

MT6630QA features a self calibration scheme to compensate the process and temperature variation to maintain high performance. The calibration is performed automatically right after the system boot-up.

4.5 GPS Subsystem

4.5.1 GPS Subsystem Digital Part

The digital part of GPS subsystem provides competitive correlator circuits with high-performance and low-power consumption. The implemented measurement engine supports GPS/GLONASS/Galileo/Beidou/QZSS satellite system and performs C/A code acquisition and tracking, Doppler and carrier phase measurement, pseudo-range measurement and data bit decoding. Additionally, RTC block is used to maintain time information while most circuits of this subsystem are switched off.

A novel technique for interference cancellation which can detect, track and remove up to 12 in-band interferences is also implemented.

For A-GPS application, a user-defined 1 pulse-per-second (1PPS) output and external SYNC input are provided.

4.5.2 GPS Subsystem RF Part

The GPS RF uses only one single receiver path and a single synthesizer to support simultaneous tri-band reception, which usually necessitates the use of three dedicated receivers driven by three separate synthesizers, which adds complexity, die area, cost and most importantly current consumption. The block diagram of the receiver is shown in following section. The SoC consists of a reconfigurable low-IF receiver, a fractional-N frequency synthesizer, and a digital baseband processor. Since different satellite signals are uncorrelated and are buried well below the noise floor, they can be amplified and down-converted by the same RF/analog chain as an image of one another, and then separated in digital domain by the corresponding correlator and signal processor. As a result, the radio architecture allows for configurations of GPS/Galileo-only, GPS/Galileo-Glonass,GPS-Beidou modes or GPS/GLONASS/BEIDOU triple-bands, which are set by the LO and baseband filter configurations. In the case of GPS/Galileo-only reception, the LO (fLO_GPS) is set to 1571.328MHz resulting in an IF frequency of 4.092MHz, with the baseband filter configured as complex BPF. On the other hand, for simultaneous GPS/Galileo and Glonass dual reception, the LO (fLO_GG) is set to 1588.608MHz. As a result, the GPS/Galileo signal becomes the image of the Glonass satellite signal with an IF frequency of 13.1MHz, and the baseband filter in this case is configured as real LPF. The Glonass signal is separated from the GPS/Galileo image signal in digital baseband. Similarly, with the LO (fLO_GB) is set to 1568.256MHz, the resulting IF frequency is about 7.1MHz for GPS/Galileo and Beidou dual reception, as shown in Figure 4.5.2.1.1. For triple band receive, the LO is set to 1581.504MHz, the resulting IF frequency are -20.406MHz, -6.084MHz and 20.214MHz for Beidou, GPS and GLONASS, respectively. Only one synthesizer is needed to support this architecture. All

RF/analog blocks operate under a 1.55V supply voltage (Please double check the descriptions as MT6630 support tri-band reception)

4.6 FM Subsystem

4.6.1 General Description

FM radio subsystem integrates complete receiver supporting 65-108 MHz bands with 50 KHz tuning step. MT6630QA performs fast channel seek/scan algorithm to validate 206 carrier frequencies in 10 seconds, with maximum valid channel and minimum fake (silence) channel performance. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM receiver utilizes state-of-the-art digital demodulation/modulation technique to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize the RX system performance in all ranges of signal quality by referring to the Channel Quality Index (CQI). When receiving poor signals, MT6630QA not only enhances the ACI rejection capability but also soft-mutes annoying noise to provide good perception quality.

The FM radio subsystem supports long antenna, which is usually in the earphone on the mobile device, and short antenna which is usually a FPC short antenna.

MT6630QA QFN package FM only supports RX feature, which has only long antenna port, the typical application scenario:

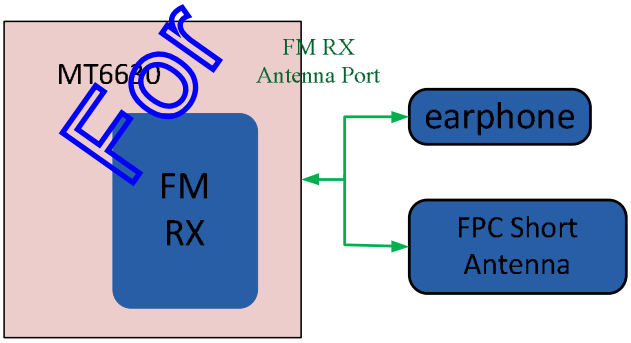

Figure 10. Long/short antenna RX application scenario (QFN package)

The control interface of the FM radio subsystem can be either SDIO or UART shared with other subsystems. That is, no additional control pin is needed for FM. MT6630QA supports audio input via either analog line-in/line-out interface or the I2S digital audio interface. The following figure illustrates the typical circuit of FM radio subsystem on the mobile.

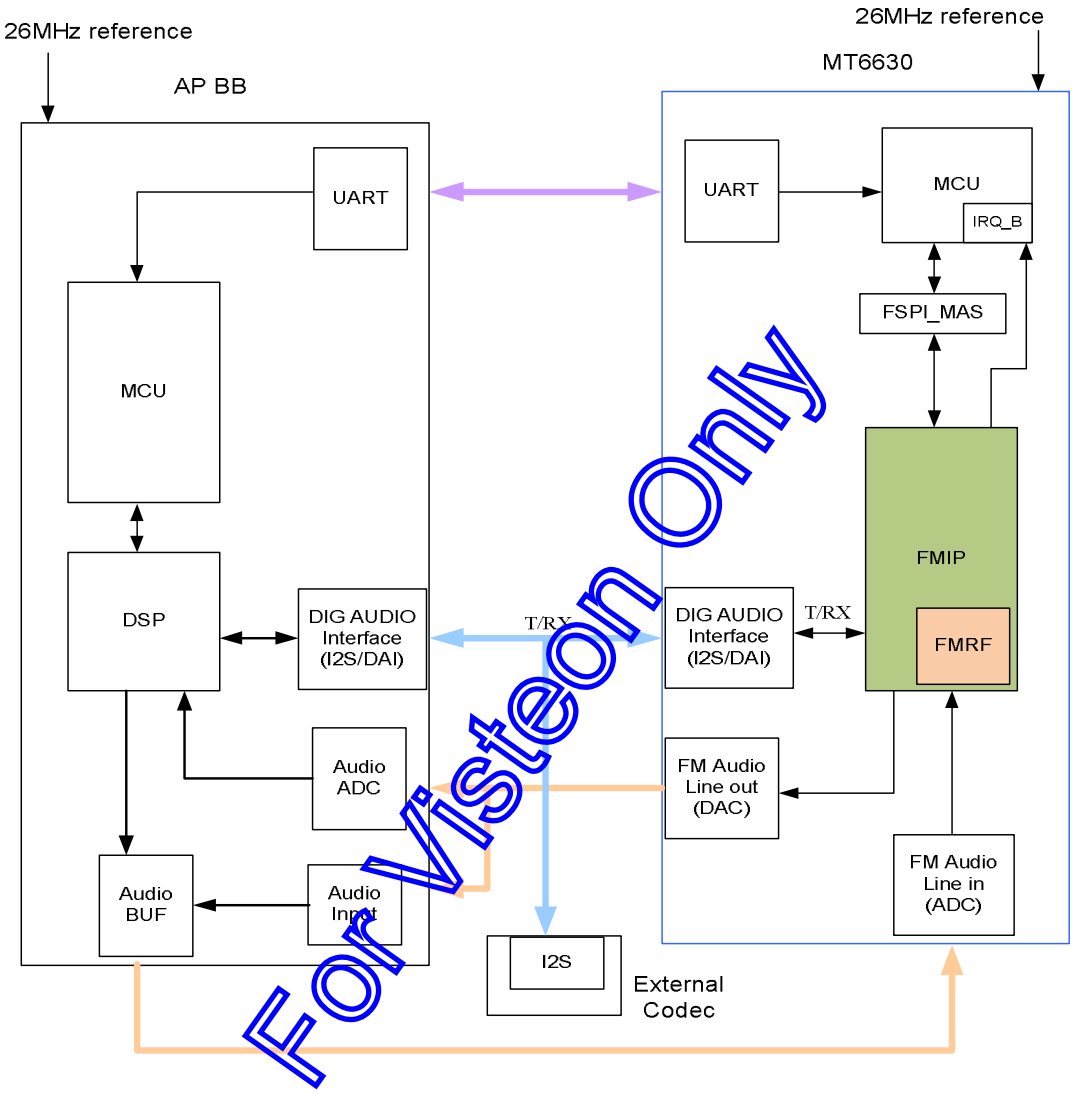

Figure 11. FMSYS typical application connection

4.6.2 FM RX Features

- 65-108 MHz worldwide FM bands with 50-kHz tuning step
- Supports RDS/RBDS radio data system
- Digital stereo demodulator
- Adaptive FM demodulator for both high- and low-quality scenarios
- Low sensitivity level with superior interference rejection
- Programmable de-emphasis (bypass/50μS/75μS)

- Stereophonic multiplex signal (MPX) signal detection and demodulation
- Superior stereo noise reduction and soft mute volume control
- Audio dynamic range control
- Mono/stereo blending
- Audio SINAD≥60dB
- Audio sensitivity3dBμVemf (SINAD=26dB)
- Supports Anti-jamming algorithm
- Supports both long and short antennas with auto calibration
- Supports I2S output master/slave 32/44.1/48KHz 16bit L&R

4.7 BT/WLAN/Multi Radio Co-existence Interface

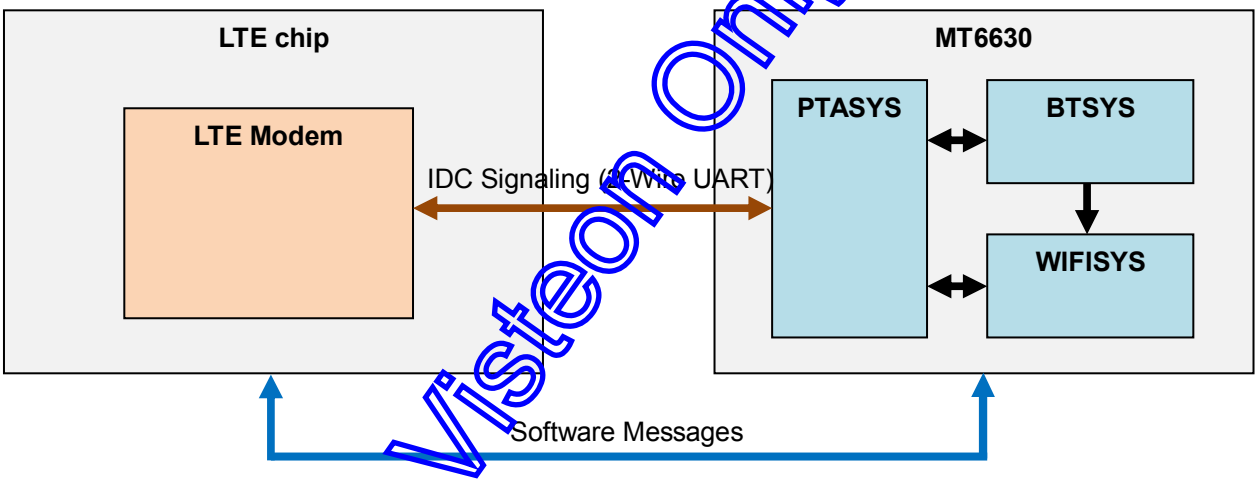

Figure 12. BT/WLAN coexistence design architecture

a. BT internal interface
b. WLAN internal interface
c. Antenna control interface
d. LTE IDC signaling interface

Detailed descriptions are listed in the following sections.

4.7.1 Internal Interface for Co-existed and Co-located 2.4GHz WLAN and BT

MT6630QA supports an information exchange scheme for co-existed and co-located 2.4GHz WLAN and BT. The information exchange is mainly defined for:

a. Scheduled coexistence mode (SCM)
b. Baseband enhancement in both Bluetooth and WLAN

SCM is aimed at low-cost BT/WLAN coexistence design. When SCM is used, BT and WLAN share the antenna exclusively.

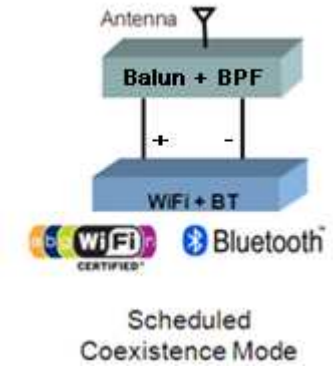

Figure 13. Illustration of single antenna scheduled coexistence and unscheduled coexistence architecture

The scheduled coexistence mode is supported by adjusting Bluetooth and WLAN activities for the optimal signal coverage with acceptable throughput. The BT voice/audio traffic is always in high priority. The WLAN packets will be scheduled in Bluetooth idle period. When Bluetooth is busy, WLAN will protect its channel and prevent rate-down by NAV reservation or fast power saving.

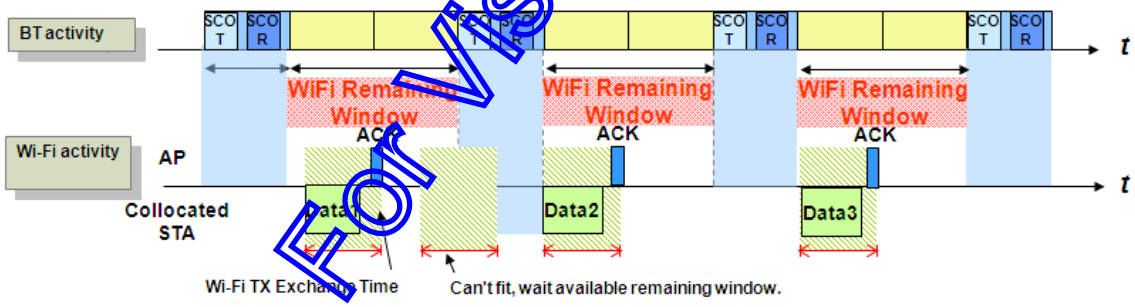

Figure 14. When scheduled coexistence mode is used, BT and WLAN can share the antenna exclusively

4.7.2 Antenna Control Interface

MT6630QA provides a configurable antenna control interface to support BT/WLAN single antenna architectures, external WLAN LNA, and external WLAN(5G) PA options. All of them can be configured through the host WMT driver interface.

4.7.3 LTE IDC Signaling Interface

Two UART pins are used to communicate between MT6630QA and LTE modem chip. MT6630QA implements a proprietary protocol to transmit traffic information. With this protocol, LTE and WiFi/BT can efficiently share 2.4G bandwidth and avoid collision in TDD manner.
BTSIG protocol is also supported in addition to MTK proprietary mode.

5 Interface Description

5.1 Host Interface (HIF)

MT6630QA supports two common host interfaces, SDIO3.0 and UART. The two common host interfaces are decided by the strap function. SDIO supports four sub-systems (WLAN, BT, ANT+, FM and GPS) as the host interface while UART only supports BT, ANT+, FM and GPS.

Host Interface	BT/ANT+	FM	GPS	WLAN	Functionality
Common Interface 1	SDIO	SDIO	SDIO	SDIO	By strap
Common Interface 2	UART	UART	UART	SDIO	By strap

Table 13. Host interface

5.1.1 HIF Sharing SDIO

SDIO provides ultra high-speed data I/O with low power consumption for mobile devices. During normal initialization and interrogation by the SDIO host, the SDIO client identifies itself as an SDIO card. The host software obtains the card information in a tuple (linked list) format and determines if the I/O functions of the card are acceptable to activate. MT6630QA HIF module provides one SDIO3.0 card interface connected to the host and can support multiple speed modes, which include default speed, high speed, SDR12, SDR25, SDR50, SDR104 and DDR50.

Even if MT6630QA is already designed with multiple HIF capabilities for different functions, it still reserves the capability for HIF sharing among different functions. However, under this user scenario, the performance/latency limitation may be the issue for normal operation due to HIF access sharing. To prevent such uncertainty, it is recommended that independent HIF should be selected for different functions.

The SDIO interface can be used as a common interface between BT/ANT+/FM/GPS (function2) and WLAN (funtion1). The bus driver will read the SDIO CIS and load different client drivers based on the function number, and these two function drivers will work independently.

For the SDIO bus driver provided by OS, it simply maintains a single First-In-First-Out queue for processing the SDIO bus requested from different client drivers. For the client driver operated on the OS, its function is registered to OS and will be invoked by OS in its thread priority.

With the assumption that the host interface is the performance limitation for the functions attached to the HIF, several bus access management approaches can be taken toward differentiating the high and low priority traffic. However, the performance limitation may also exist under different user scenarios.

5.1.2 Signal Pins

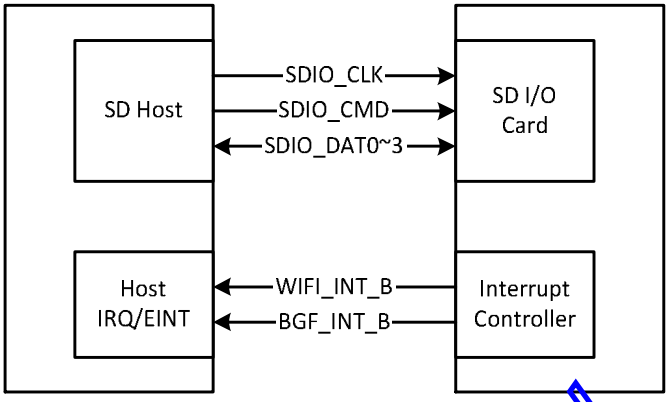

Figure 15. Signal connections to two 4-bit SDIO cards and host interrupt

5.1.3 SDIO Timing Waveform(3.3v)

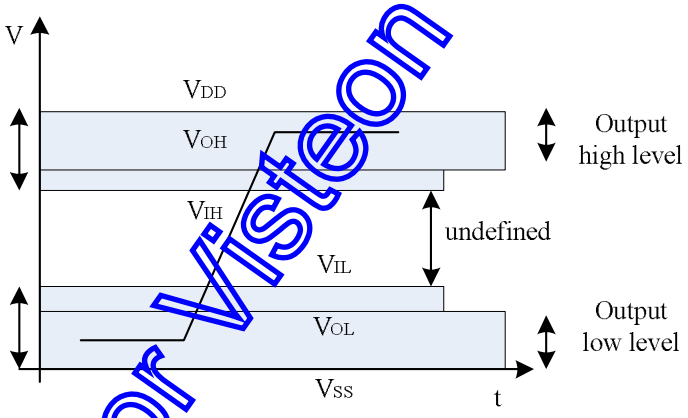

Figure 16. Bus signal levels

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD min
Output Low Voltage	VOL		0.125*VDD	V	IOL = 2mA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25*VDD	V	

Table 14. Bus signal voltage

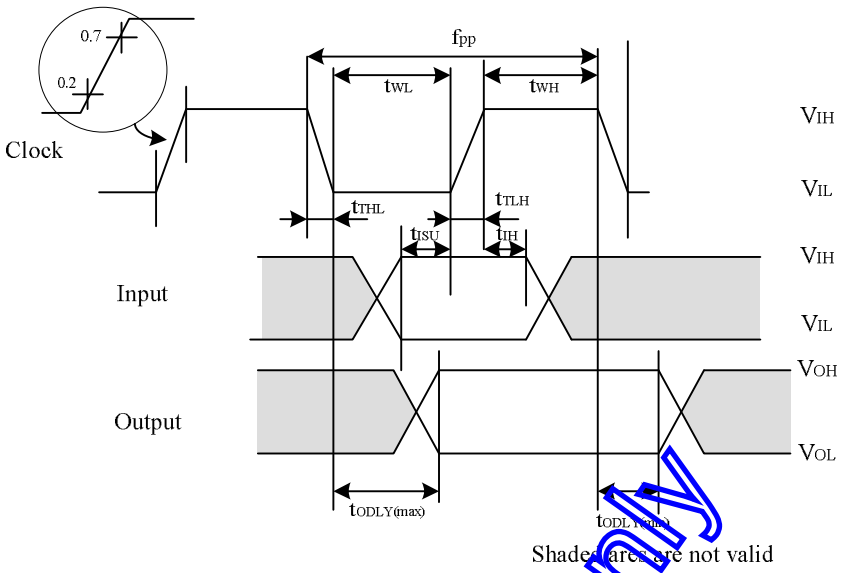

Figure 17. Bus timing diagram (default)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock frequency identification mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{OLDY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output delay time during identification mode	t_{OLDY}	0	50	ns	C_L ≤ 40 pF (1 card)

Table 15. Bus timing parameter values (default)

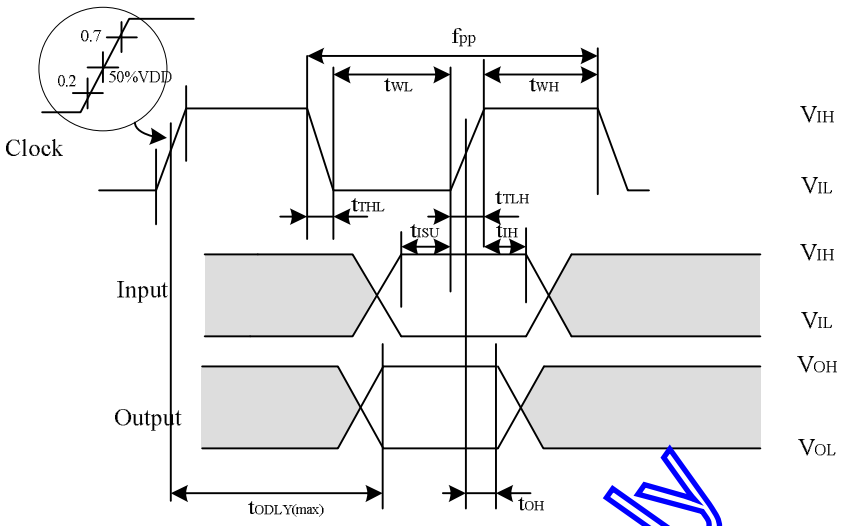

Figure 18. High-speed timing diagram

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{OLDY}		14	ns	C_L ≤ 40 pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L ≥ 40 pF (1 card)
Total system capacitance for each line (1)	C_L		40	pF	1 card

(1) In order to satisfy the serve timing, the host shall drive only one card

Table 16. High-speed timing parameter values

5.1.4 SDIO Timing Waveform(1.8v)

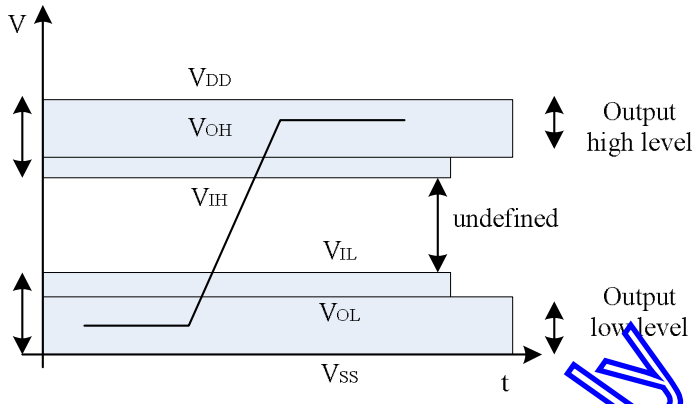

Figure 19. Bus signal levels

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output High Voltage	VOH	1.40		V	IOH= - 2mA
Output Low Voltage	VOL		0.45	V	IOL = 2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	Vss-0.30	0.58V	V	

Table 17. Bus signal voltage

SDR12 、SDR25、 SDR50 and SDR104 mode :

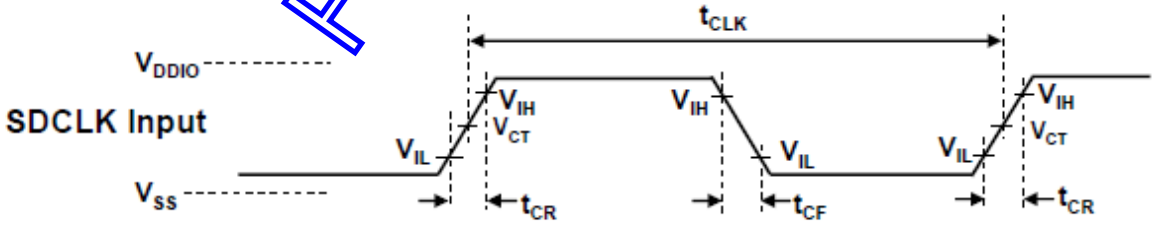

Figure 20. SDR12 、SDR25、 SDR50 and SDR104 mode clock signal timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Table 18. SDR12 、SDR25 、 SDR50 and SDR104 mode clock signal timing parameter values

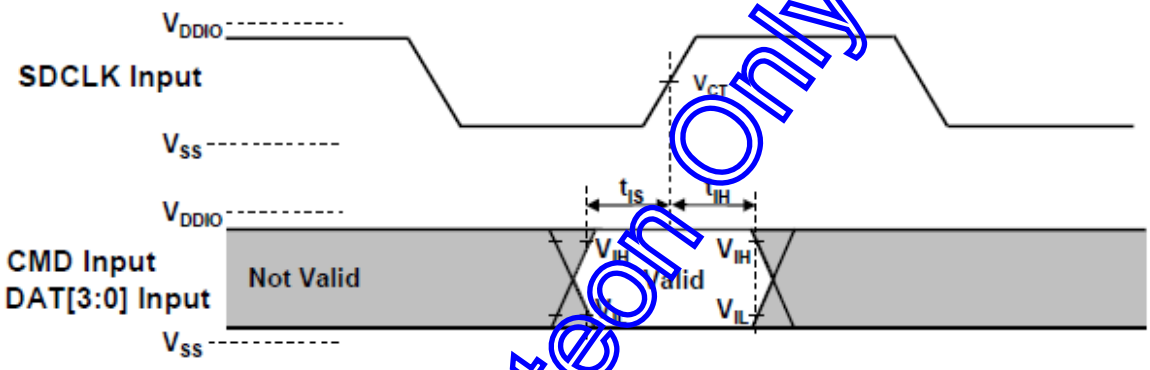

Figure 21. SDR50 and SDR104 input signal timing

Symbol	Min.	Max.	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80		ns	C_{CARD} =5pF, V_{CT}= 0.975V
Symbol	**Min.**	**Max.**	**Unit**	**SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} =5pF, V_{CT}= 0.975V

Table 19. SDR50 and SDR104 input timing parameter values

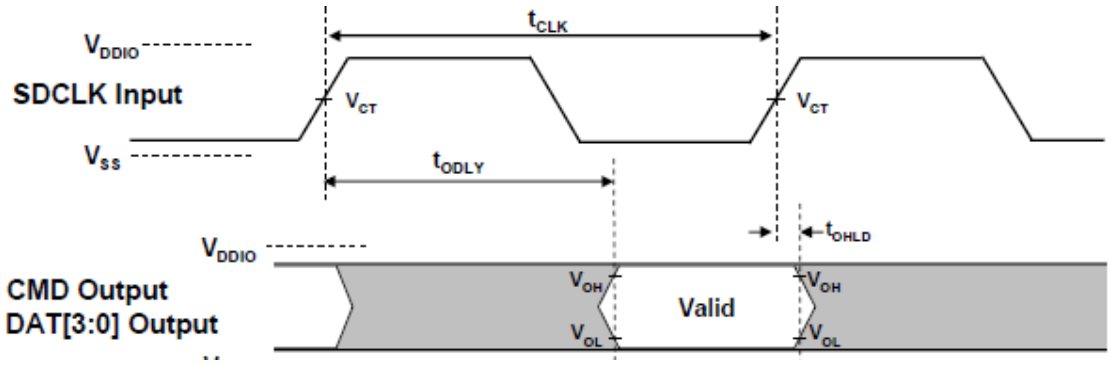

Figure 22. SDR12、SDR25 and SDR50 output timing

Symbol	Min.	Max.	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50,
t_{ODLY}		14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Table 20. SDR12、SDR25 and SDR50 output timing parameter values

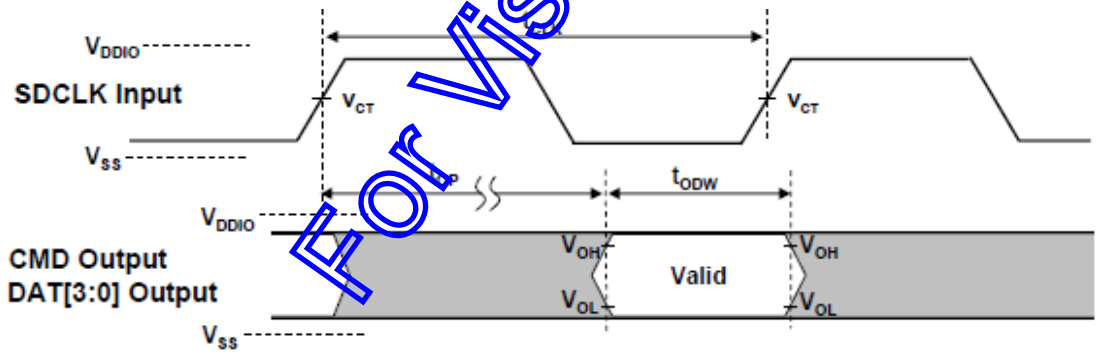

Figure 23. SDR104 output timing

Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW}=2.88ns at 208MHz

Table 21. SDR104 output timing parameter values

DDR50 Mode:

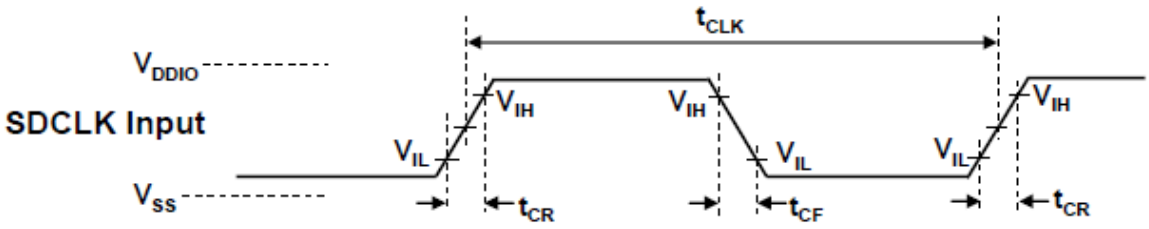

Figure 24. SDR50 clock timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Table 22. SDR50 clock timing parameter values

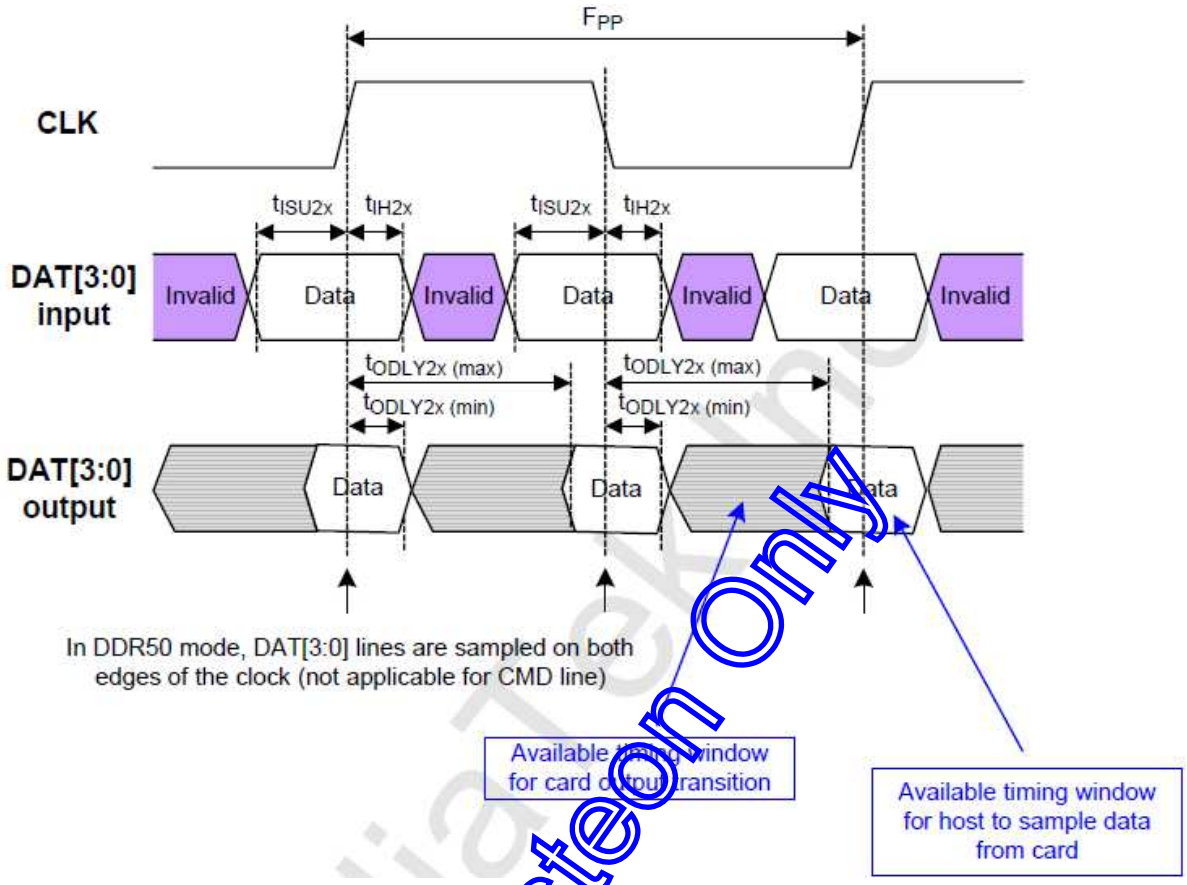

Figure 25. SDR50 input and output timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30$ pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geq 15$pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{CARD} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output hold time	t_{ODLY2x}	1.5	-	ns	$C_L \geq 15$pF (1 card)

Table 23. SDR50 input and output timing parameter values

5.2 Common UART1 Interface

The UART interface provides full duplex serial communication channel between the baseband chipset and its external devices. It supports the word length from five to eight bits, an optional parity bit and one or two stop bits. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmitting and receiving FIFOs. The UART also includes modem control lines and two DMA handshake lines which are used to indicate when the FIFOs are ready to transfer data to the connectable device.
Other baud rates that are not shown in the baud rate table below may also be supported through UART register configuration. However, system designers must take care in making sure that the total baud rate frequency mismatch between the 2 sides, along with the electrical signal timings, can still meet the 2% error margin required in order to sustain the rate of operation.

BAUD(bps)	19.2MHz	20MHz	24MHz	26MHz	38.4MHz	40MHz	52MHz
110	√	√	√	√	√	√	√
300	√	√	√	√	√	√	√
1,200	√	√	√	√	√	√	√
2,400	√	√	√	√	√	√	√
4,800	√	√	√	√	√	√	√
9,600	√	√	√	√	√	√	√
19,200	√	√	√	√	√	√	√
38,400	√	√	√	√	√	√	√
57,600	√	√	√	√	√	√	√
115,200	√	√	√	√	√	√	√
230,400	√	√	√	√	√	√	√
921,600	√	√	√	√	√	√	√
3,250,000	×	×	×	√	√	√	√

Table 24. Supported baud rates for different crystal clocks

Note: If the desired baud rate is not list in the table above, please consult MediaTek support for help.

The UART provides more powerful flow control:

- **Hardware flow control:** Use two dedicated signals, Clear To Send (CTS) and Request To Send (RTS), to indicate if it is ready to acquire or send data. When CTS is high, UART can start to transmit data. As long as CTS is not activated, UART is not allowed to send data. RTS goes high means UART FIFO in the received path is sufficient to receive data. UART is not allowed to receive data when RTS is low.
- **Software flow control:** Use special character Xon/Xoff for software flow control. Xon/Xoff is software programmable. When Xoff is received, UART transmission will be halted. Once Xon is received, the transmission will resume.

5.3 EFUSE Function

There are some EFUSE macros inside MT6630Q. The EFUSE macro is a one-time-programming (OTP) non-volatile memory used to store sensitive and important data. The EFUSE controller delivers EFUSE status and re-initializes the EFUSE macro. The user can program the EFUSE via the EFUSE controller with proper configuration and sequences.

5.4 PCM Interface

MT6630QA incorporates the Pulse Coded Modulation (PCM) interface and I2S for Bluetooth voice data transferring between MT6630QA and the host system continuously without MCU intervention for maximum power saving.

MT6630QA PCM interface supports most commonly used formats by user configuration, as listed below.

Interface configuration parameters	Supported values
Line interface format	Linear
Data length	Linear: 13/14/15/16 bits
Voice sampling rate	8kHz samples/16kHz samples
PCM clock/sync source	PCM master mode: Clock and sync are internally generated. PCM slave mode: Clock and sync are from external. PCM hybrid master mode: Clock is internally generated, and sync is from the external. PCM hybrid slave mode: Clock is from the external, and sync is internally generated.
PCM sync rate	8kHz/16Khz
PCM clock rate	8Khz: PCM master mode/PCM hybrid master mode: 128kHz/256kHz/512kHz/1,024kHz/2,048kHz (Linear) PCM slave mode/PCM hybrid slave mode: 128kHz ~ 2.4MHz (Linear) 16Khz: PCM master mode/PCM hybrid master mode: 256kHz/512kHz/1,024kHz/2,048kHz (Linear) PCM slave mode/PCM hybrid slave mode:256kHz ~ 2.4MHz (Linear)
PCM sync format	Short sync or long sync
Data ordering	MSB or LSB first (see configuration matrix for limitation)
Zero padding	Yes (see configuration matrix for limitation)
Sign extension	Yes (see configuration matrix for limitation)
2's complement	Yes (see configuration matrix for limitation)
1's complement	Yes (see configuration matrix for limitation)
Sign-magnitude	Yes (see configuration matrix for limitation)
Unsigned	Yes (see configuration matrix for limitation)

Table 25. PCM interface configurations

Interface configuration parameters	Supported values
Line interface format	Linear
Data length	Linear: 13/14/15/16 bits
Voice sampling rate	8kHz samples
I2S clock/sync source	I2S master mode: Clock and sync are internally generated. I2S slave mode: Clock and sync are from external. I2S hybrid master mode: Clock is internally generated, and sync is from the external. I2S hybrid slave mode: Clock is from the external, and sync is internally generated.
I2S WS rate	8kHz/16Khz/32Khz/48Khz
I2S clock rate	256Khz/512Khz/1024Khz/1536Khz
Data ordering	MSB or LSB first (see configuration matrix for limitation)
Zero padding	Yes (see configuration matrix for limitation)
Sign extension	Yes (see configuration matrix for limitation)
2's complement	Yes (see configuration matrix for limitation)
1's complement	Yes (see configuration matrix for limitation)
Sign-magnitude	Yes (see configuration matrix for limitation)
Unsigned	Yes (see configuration matrix for limitation)

Table 26. I2S interface configurations

The supported configuration matrix is summarized as below.

Note that the sign extension and zero padding are only relevant when the linear input bits are less than 16 bits (only for PCM).

Configurations	Sign extension	Zero padding	MSB first	LSB first	PCM long sync	PCM short sync
1		V	V		V	
2	V		V		V	
3		V	V			V
4	V		V			V
5		V		V	V	
6		V		V		V

Table 27. PCM configuration matrix summary

5.4.1 Recommended Settings

For the best quality, the recommended settings are:

16b linear CVSD + MSB first + short sync + 256 kHz PCM clock

5.4.2 Detailed Interface Description

5.4.2.1 PCM Master/Slave Mode

When MT6630QA is a PCM slave, both PCM sync and PCM clock signals will be generated by the external PCM master. When being a PCM master, both PCM sync and PCM clock will be generated by MT6630Q.

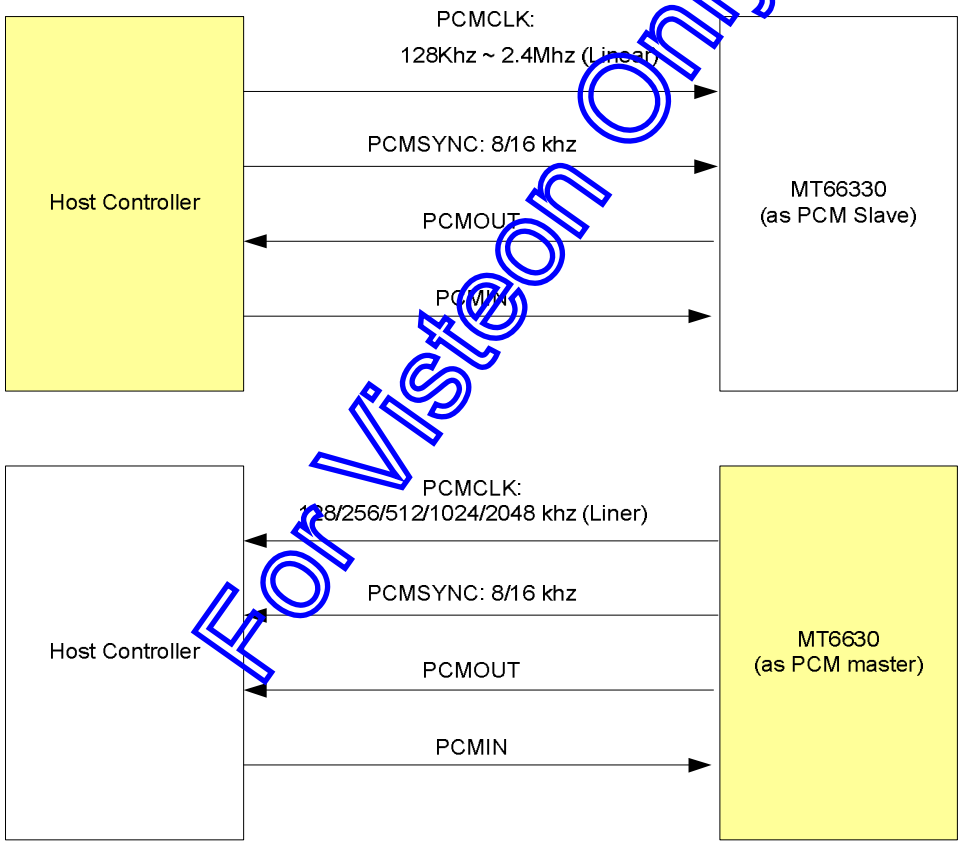

Figure 26. PCM master/slave modes

5.4.2.2 PCM Hybrid Master/Slave Mode

When MT6630QA is a PCM hybrid slave, PCM clock signal will be generated by the external PCM hybrid master, and the PCM sync signal is internally generated by MT6630Q. When being a PCM master, the PCM clock signal will be generated internally by MT6630Q, and the PCM sync signal will be generated by the external PCM hybrid slave.

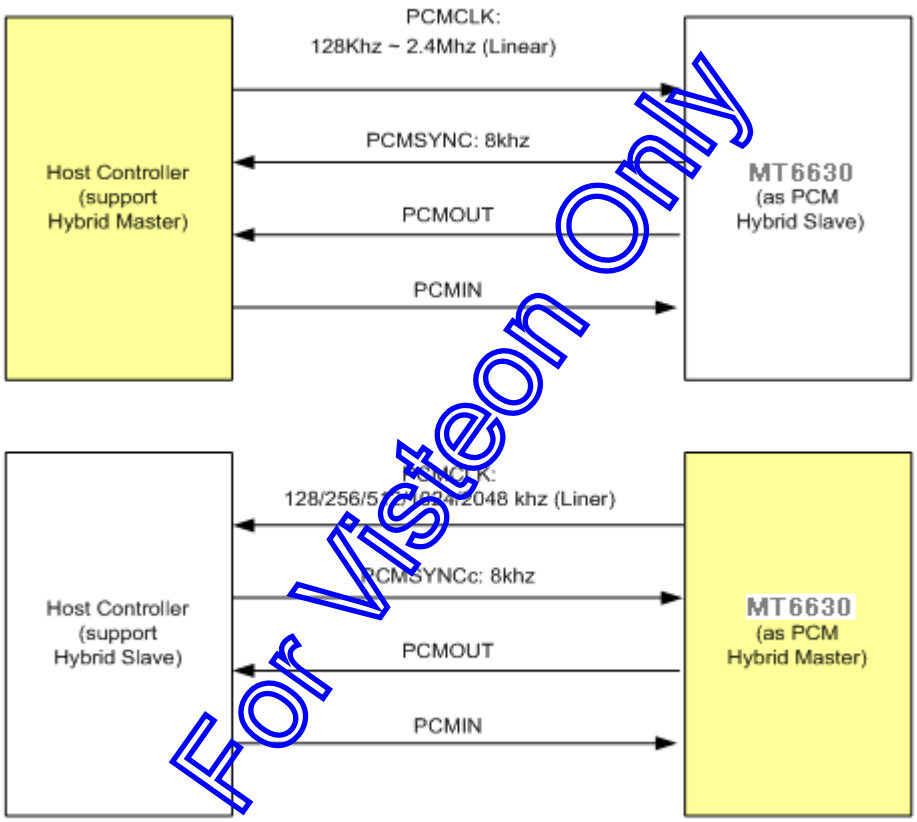

Figure 27. PCM hybrid master/slave hybrid modes

5.4.2.3 Sign Extension

The sign extension is only meaningful when the linear PCM length is shorter than 16 bits, and it only applies to MSB first data formats.

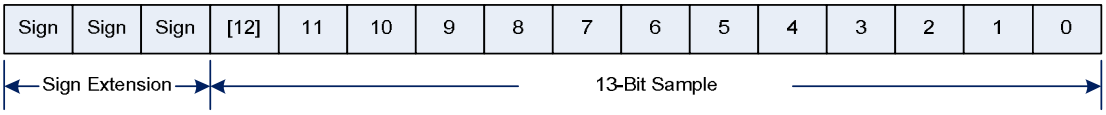

Figure 28. PCM format: sign extension

5.4.2.4 Zero Padding

Zero padding is only meaningful when the linear PCM length is shorter than 16 bits, and it only applies to the first data formats of LSB.

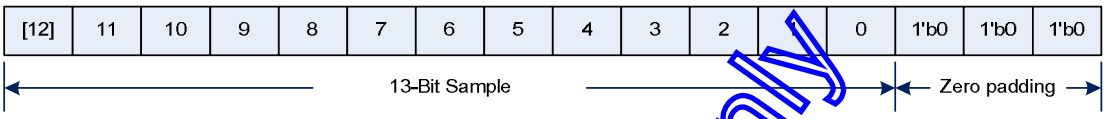

Figure 29. PCM format: zero padding

5.4.2.5 I2S Master/Slave Mode

When MT6630QA acts as a I2S slave, both I2S WS and I2S clock signals will be generated by the external I2S master. When it acts as a I2S master, both I2S WS and I2S clock will be generated by MT6630Q.

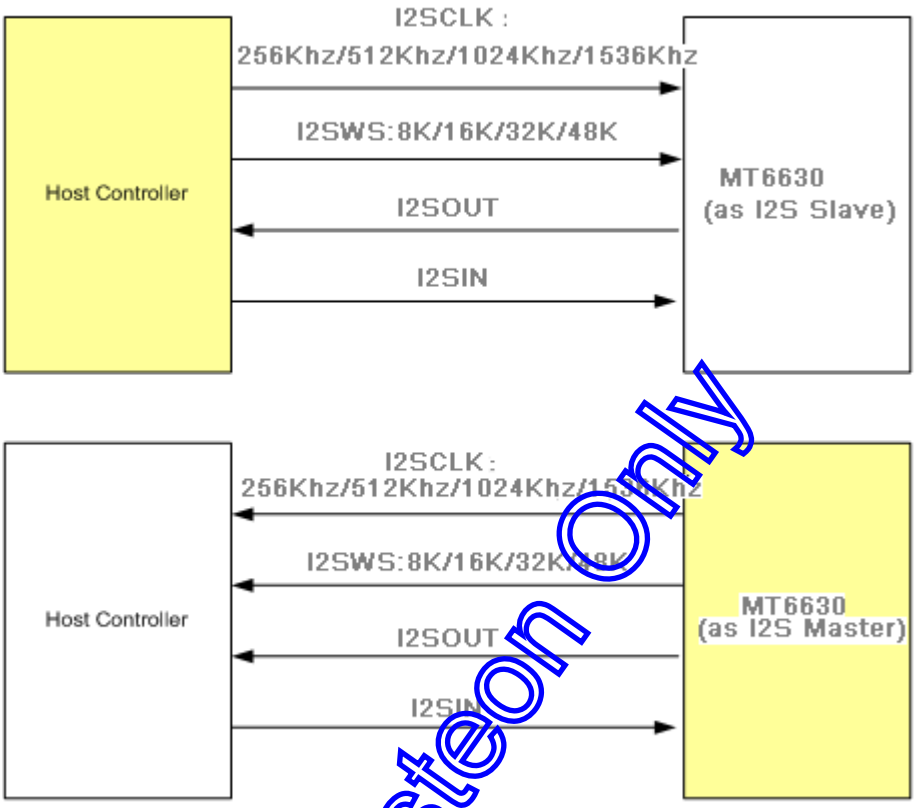

Figure 30. I2S master/slave modes

5.4.3 VOICE Timing Examples

The figure below gives a common interface timing configuration example.
Example: 16b linear PCM, 256kHz PCM clock, 8k sync

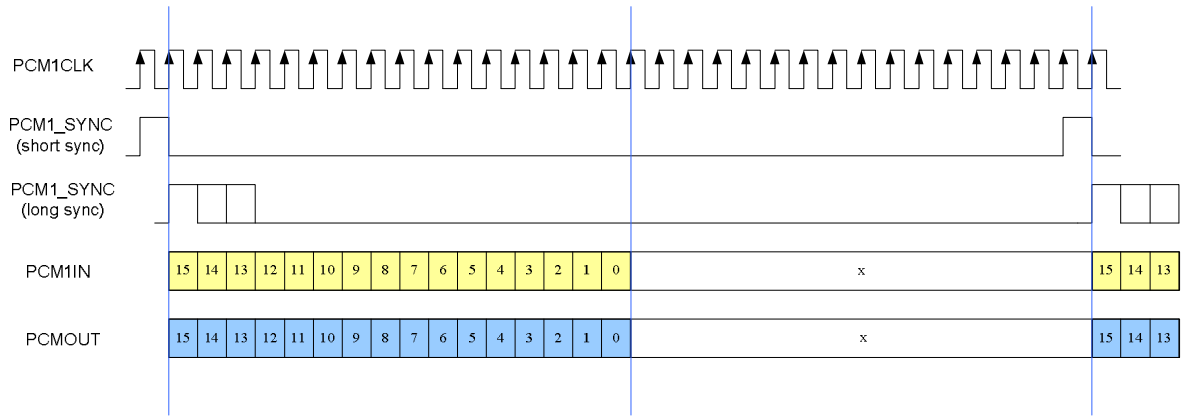

Figure 31. PCM format: 16b example

Example: 16b linear PCM, 256kHz PCM clock, 8k sync 32bit

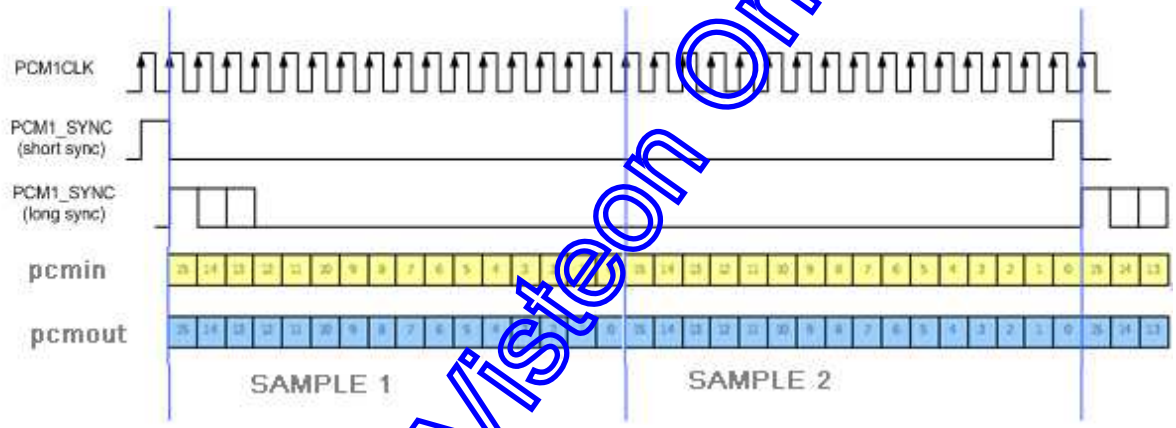

Figure 32. PCM format: 32b example

Example: 48K I2S with bitwidth = 16,clock rate=1536khz

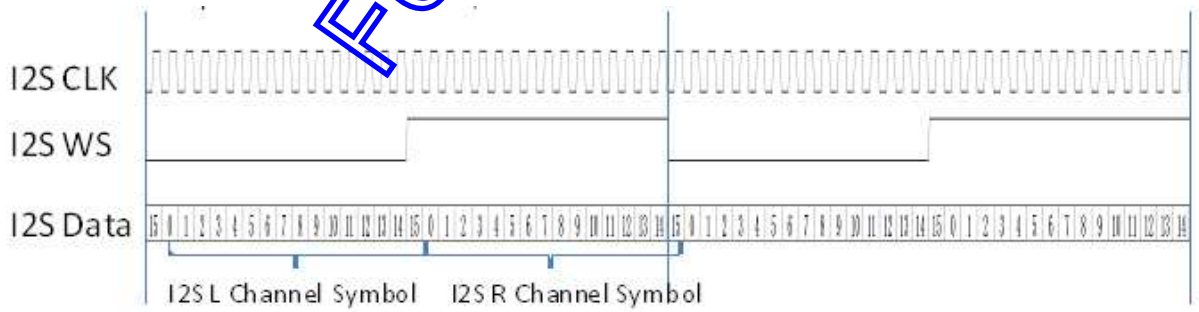

Figure 33 I2S formate: 48Khz

5.5 FM Digital Audio Interface Description

5.5.1 I2S Interface

For digital audio input and output, the industry standard I2S interface is supported by MT6630Q, and the I2S controller can be in either master mode (MT6630QA supplies clock and ws) or slave mode (host supplies clock and ws).

The supported formats are listed in the table below:

I2S Format Supported	
Role	Slave mode (Host provides clock and ws) Master mode (MT6630QA provides clock and ws)
Sample rate	32kHz/44.1kHz/48kHz
Data bit width	16 bits per channel
Alignment	MSB first
Clock rate	Nominal 1.024MHz for 32kHz sample rate Nominal 1.536MHz for 48kHz sample rate Under the slave mode, a higher clock rate above the nominal rate can be used, and the extra clock cycles will simply be discarded internally by the controller.

Table 28. FM I2S format supported

MT6630QA support two I2S standards: One is EIAJ mode which WS and DATA is aligned, and the other is I2S mode which WS is advanced DATA one bit. The provided I2S protocol is MSB first, and Left channel first also.

The signal timing diagram is depicted below. Note that EDI_DAT represents either the output data pin or input data pin.

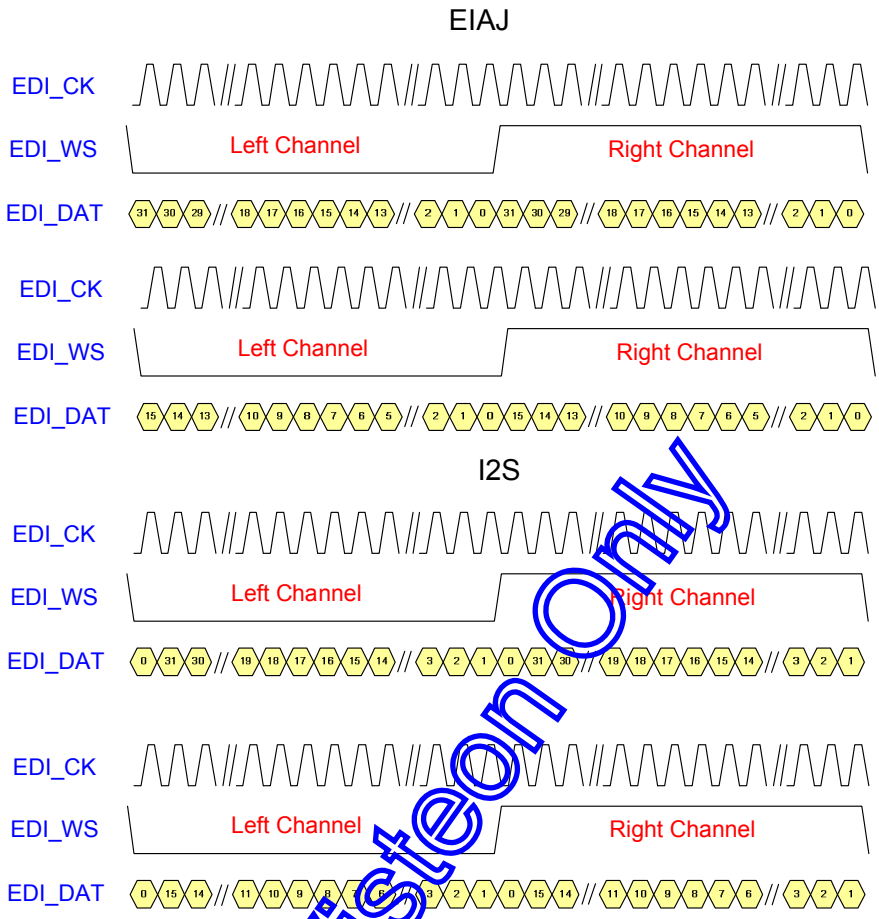

Figure 34. I2S timing waveform

5.6 BT/FM Shared PCM Interface

MT6630QA supports MediaTek's proprietary interface, FM stereo audio and Bluetooth voice on the same interface.

Figure 35. Merge interface block diagram

In this mode, the bus data rate should be the sample rate of the FM audio. A sync pulse is used to indicate the beginning of the frame, and only slave mode is supported.

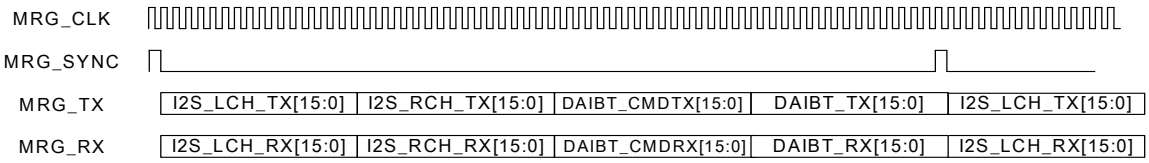

Figure 36. Merge interface timing diagram

5.7 AGPS Interface

5.7.1 ECLK

ECLK is a clock input pin which introduces external clock signals to MT6630QA and obtains the relationship between the external clock and GPS local clock. With precise external clock input, the clock drift of the GPS local clock can be correctly estimated. Therefore, the Doppler search range is narrowed down accordingly. This technology is beneficial for speeding up the satellite acquisition process. Especially in the case of cold start, due to limited priori information on the satellite's location and local clock uncertainty, a receiver will execute a search in full frequency range. Consequently, a longer acquisition time will be expected. However, the ECLK technology reduces the frequency uncertainty so that the search process will be completed shortly. Efficient acquisition and less power consumption are attained by the ECLK technology.

5.7.2 SYNC

SYNC is a time stamp signal input pin which introduces external timing to the GPS receiver of MT6630QA to obtain the relationship between the external timing and GPS receiver local timing. With precise external timing input and the established relationship, the GPS Time Of Week (TOW) can be correctly estimated in the GPS receiver. This technology is beneficial for Time To First Fix (TTFF), especially in weak signal environments. In the case of hot start, with priori information on the GPS receiver's location and satellite ephemeris data, the GPS receiver uses the correct GPS TOW to accurately predict the signal code chip/phase. Therefore, the code search range can be narrowed down accordingly. Hence, fast TTFF can be achieved by the SYNC technology.

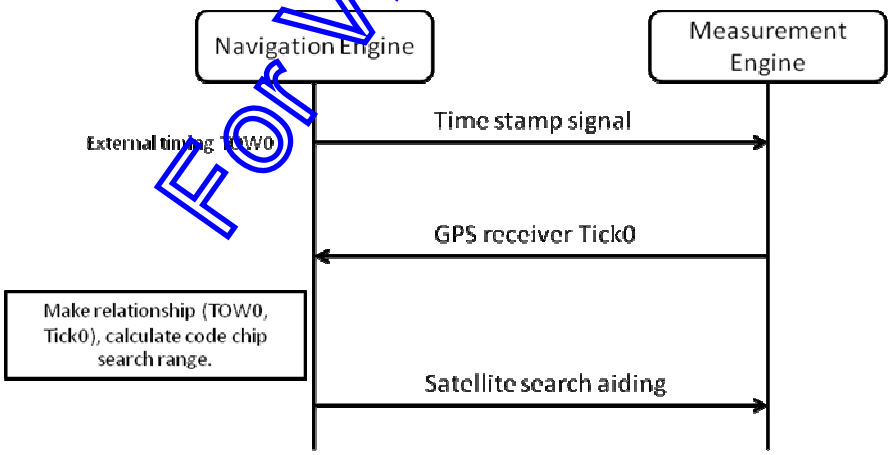

Figure 37. Time sync mechanism

5.8 Clock Daisy Chain

The clock daisy chain supports the co-clock feature of MT6630QA with the host side or other peripheral ICs. The clock enable signal is sent to the next IC through the OSC_EN output pin. The final control signal is fed into the host side chip which controls the on/off of reference clock. It may be TCXO or XTAL.

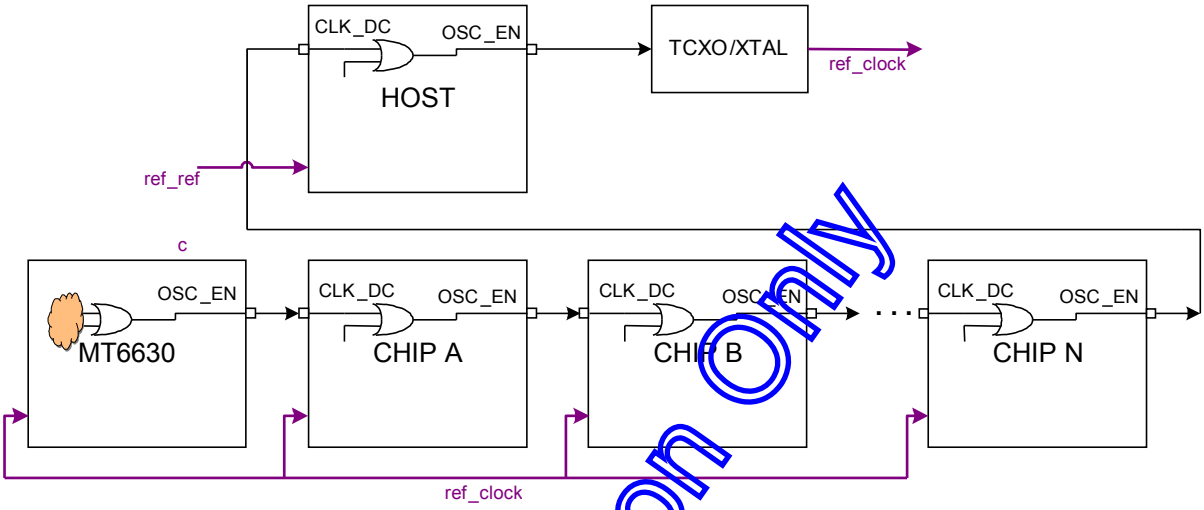

Figure 38. Clock daisy chain depiction

6 Radio characteristics

6.1 WLAN Radio Characteristics

The WLAN radio characteristics are described in this section. Unless otherwise specified, all specifications are measured at the chip output ports which are depicted in the following figure.

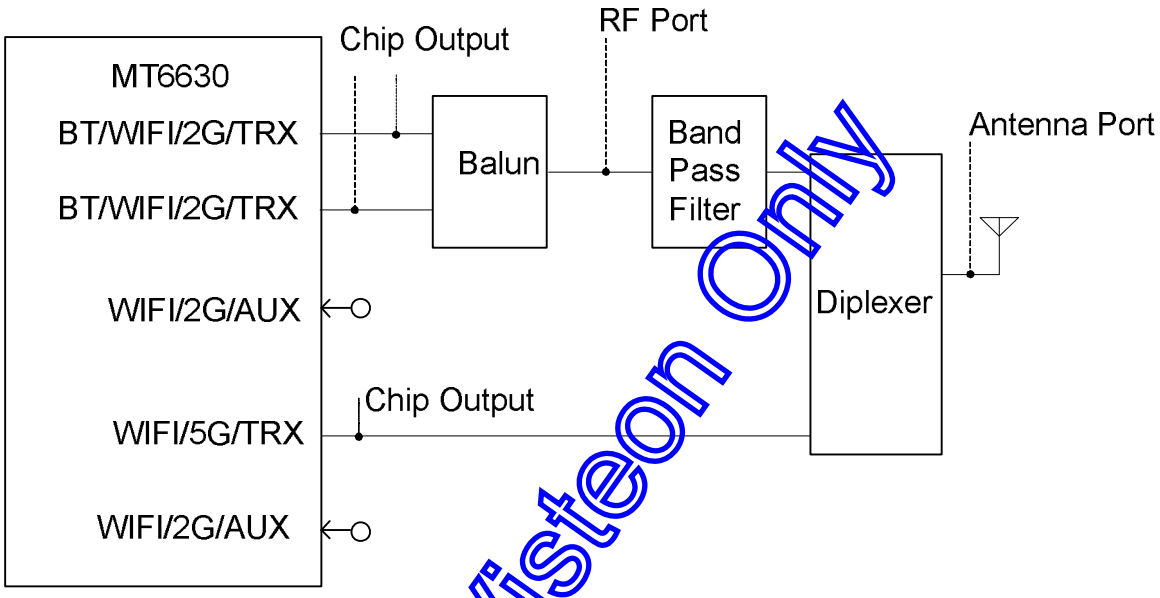

Figure 39. WiFi spec. measurement diagram

6.1.1 2.4GHz Receiver Specification (Main)

Note:

(1) The specification value is valid at room temperature (25°C).

(2) All specifications are reference to chip output unless otherwise specified.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
RX sensitivity[a]	1 Mbps DSSS		-98		dBm
	2 Mbps DSSS		-95		dBm
	5.5 Mbps DSSS		-93		dBm
	11 Mbps DSSS		-90		dBm
RX Sensitivity[a]	6 Mbps OFDM		-95		dBm
	9 Mbps OFDM		-93		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
	12 Mbps OFDM		-92		dBm
	18 Mbps OFDM		-89.5		dBm
	24 Mbps OFDM		-86.5		dBm
	36 Mbps OFDM		-83		dBm
	48 Mbps OFDM		-79		dBm
	54 Mbps OFDM		-77.5		dBm
RX sensitivity[b] BW = 20MHz Green field 800nS guard interval Non-STBC	MCS 0		-94.5		dBm
	MCS 1		-91.5		dBm
	MCS 2		-89		dBm
	MCS 3		-86		dBm
	MCS 4		-82.5		dBm
	MCS 5		-78		dBm
	MCS 6		-76.5		dBm
	MCS 7		-75.5		dBm
RX sensitivity[b] BW = 40MHz Green field 800nS guard interval Non-STBC	MCS 0		-91.5		dBm
	MCS 1		-88.5		dBm
	MCS 2		-86		dBm
	MCS 3		-82.5		dBm
	MCS 4		-79.5		dBm
	MCS 5		-75		dBm
	MCS 6		-73.5		dBm
	MCS 7		-72.5		dBm
Maximum receive level	11 Mbps DSSS			-5	dBm
	6 Mbps OFDM			-10	dBm
	54 Mbps OFDM			-10	dBm
	MCS0			-10	dBm
	MCS7			-10	dBm
Adjacent channel rejection (30MHz offset)	1 Mbps DSSS		40	40	dB
Adjacent channel rejection (25MHz offset)	11 Mbps DSSS		40	40	dB
Adjacent channel rejection (25MHz offset)	6 Mbps OFDM		34		dB
	54 Mbps OFDM		22		dB
Adjacent channel rejection (25MHz offset), BW = 20MHz	MCS 0		25		dB
	MCS 7		5		dB
Adjacent channel rejection (40MHz offset), BW = 40MHz	MCS 0		26		dB
	MCS 7		1		dB

Table 29. 2.4GHz receiver specification(Main)

a: Degraded by 1.5dB at 85°C
b: Sensitivity degradation at different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

6.1.2 2.4GHz Receiver Specification (Aux)

Note:
(1) The specification value is valid at room temperature (25°C).
(2) All specifications are measured at the RF port unless otherwise specified.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
RX sensitivity[c]	1 Mbps DSSS		-100		dBm
	2 Mbps DSSS		-97		dBm
	5.5 Mbps DSSS		-95		dBm
	11 Mbps DSSS		-92		dBm
RX Sensitivity[c]	6 Mbps OFDM		-97		dBm
	9 Mbps OFDM		-94.5		dBm
	12 Mbps OFDM		-94		dBm
	18 Mbps OFDM		-91.5		dBm
	24 Mbps OFDM		-88		dBm
	36 Mbps OFDM		-84.5		dBm
	48 Mbps OFDM		-80.5		dBm
	54 Mbps OFDM		-79		dBm
RX sensitivity[d] BW = 20MHz Green field 800nS guard interval Non-STBC	MCS 0		-96		dBm
	MCS 1		-93		dBm
	MCS 2		-90.5		dBm
	MCS 3		-87.5		dBm
	MCS 4		-84		dBm
	MCS 5		-79.5		dBm
	MCS 6		-78.5		dBm
	MCS 7		-77		dBm
RX sensitivity[d] BW = 40MHz Green field 800nS guard interval Non-STBC	MCS 0		-93		dBm
	MCS 1		-90.5		dBm
	MCS 2		-88		dBm
	MCS 3		-84.5		dBm
	MCS 4		-81		dBm
	MCS 5		-76.5		dBm
	MCS 6		-75.5		dBm
	MCS 7		-74		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
Maximum receive level	11 Mbps DSSS			-5	dBm
	6 Mbps OFDM			-10	dBm
	54 Mbps OFDM			-10	dBm
	MCS0			-10	dBm
	MCS7			-10	dBm
Adjacent channel rejection (30MHz offset)	1 Mbps DSSS		40	40	40
Adjacent channel rejection (25MHz offset)	11 Mbps DSSS		40	40	dB
Adjacent channel rejection (25MHz offset)	6 Mbps OFDM		34		dB
	54 Mbps OFDM		22		dB
Adjacent channel rejection (25MHz offset), BW = 20MHz	MCS 0		35		dB
	MCS 7		5		dB
Adjacent channel rejection (40MHz offset), BW = 40MHz	MCS 0		26		dB
	MCS 7		1		dB

Table 30. 2.4GHz receiver specification (Aux)

c: Degraded by 1.5dB at 85°C

d: Sensitivity degradation at different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

6.1.3 5GHz receiver specification (Main)

Note:

(1) The specification value is valid at room temperature (25°C).

(2) All specifications are measured at the chip output unless otherwise specified.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		4900	-	5915	MHz
RX Sensitivity[e]	6 Mbps OFDM		-94		dBm
	9 Mbps OFDM		-92		dBm
	12 Mbps OFDM		-91		dBm
	18 Mbps OFDM		-88.5		dBm
	24 Mbps OFDM		-85.5		dBm
	36 Mbps OFDM		-82		dBm
	48 Mbps OFDM		-78		dBm
	54 Mbps OFDM		-76.5		dBm
RX Sensitivity[f] BW=20MHz Green Field	MCS 0		-93.5		dBm
	MCS 1		-90.5		dBm
	MCS 2		-88		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
800nS Guard Interval Non-STBC (HT20/VHT20)	MCS 3		-85		dBm
	MCS 4		-81.5		dBm
	MCS 5		-77		dBm
	MCS 6		-75.5		dBm
	MCS 7		-74.5		dBm
	MCS 8		-70		dBm
RX Sensitivity[f] BW=40MHz Green Field 800nS Guard Interval Non-STBC (HT40/VHT40)	MCS 0		-90.5		dBm
	MCS 1		-87.5		dBm
	MCS 2		-85		dBm
	MCS 3		-81.5		dBm
	MCS 4		-78.5		dBm
	MCS 5		-74		dBm
	MCS 6		-72.5		dBm
	MCS 7		-71.5		dBm
	MCS 8		-67		dBm
	MCS 9		-65.5		dBm
RX Sensitivity[f] BW=80MHz Green Field 800nS Guard Interval Non-STBC (VHT80)	MCS 0		-87.5		dBm
	MCS 1		-84		dBm
	MCS 2		-81.5		dBm
	MCS 3		-78.5		dBm
	MCS 4		-75		dBm
	MCS 5		-70.5		dBm
	MCS 6		-69		dBm
	MCS 7		-68		dBm
	MCS 8		-63.5		dBm
	MCS 9		-62		dBm
Maximum Receive Level	6 Mbps OFDM		-10		dBm
	54 Mbps OFDM		-15		dBm
	MCS0		-15		dBm
	MCS9		-15		dBm
Adjacent Channel Rejection (20MHz offset)	6 Mbps OFDM		24		dB
	54 Mbps OFDM		7		dB
Adjacent Channel Rejection (20MHz offset), BW=20MHz	MCS 0		24		dB
	MCS 8		1		dB
Adjacent Channel Rejection (40MHz offset), BW=40MHz	MCS 0		24		dB
	MCS 9		3		dB
Adjacent Channel Rejection (80MHz	MCS 0		24		dB
	MCS 9		3		dB

Parameter	Description	Min.	Typ.	Max.	Unit
offset), BW=80MHz					

Table 31. 5GHz receiver specification(Main)

e: Degraded by 1.5dB at 85°C
f: Sensitivity degradation at different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

6.1.4 5GHz receiver specification (Aux)

Note:
(1) The specification value is valid at room temperature (25°C).
(2) All specifications are measured at the chip output unless otherwise specified.

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		4900	-	5925	MHz
RX Sensitivity[g]	6 Mbps OFDM		-96		dBm
	9 Mbps OFDM		-93.5		dBm
	12 Mbps OFDM		-93		dBm
	18 Mbps OFDM		-90.5		dBm
	24 Mbps OFDM		-87		dBm
	36 Mbps OFDM		-84		dBm
	48 Mbps OFDM		-79.5		dBm
	54 Mbps OFDM		-78		dBm
RX Sensitivity[h] BW=20MHz Green Field 800nS Guard Interval Non-STBC (HT20/VHT20)	MCS 0		-95		dBm
	MCS 1		-92		dBm
	MCS 2		-89.5		dBm
	MCS 3		-86.5		dBm
	MCS 4		-83		dBm
	MCS 5		-78.5		dBm
	MCS 6		-77		dBm
	MCS 7		-76		dBm
	MCS 8		-71.5		dBm
RX Sensitivity[h] BW=40MHz Green Field 800nS Guard Interval Non-STBC (HT40/VHT40)	MCS 0		-92		dBm
	MCS 1		-89		dBm
	MCS 2		-86.5		dBm
	MCS 3		-83		dBm
	MCS 4		-80		dBm
	MCS 5		-75.5		dBm
	MCS 6		-74		dBm
	MCS 7		-73		dBm
	MCS 8		-68.5		dBm
	MCS 9		-67		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
RX Sensitivity[h] BW=80MHz Green Field 800nS Guard Interval Non-STBC (VHT80)	MCS 0		-89		dBm
	MCS 1		-85.5		dBm
	MCS 2		-83		dBm
	MCS 3		-80		dBm
	MCS 4		-76.5		dBm
	MCS 5		-72		dBm
	MCS 6		-70.5		dBm
	MCS 7		-69.5		dBm
	MCS 8		-65		dBm
	MCS 9		-63.5		dBm
Maximum Receive Level[d]	6 Mbps OFDM		-10		dBm
	54 Mbps OFDM		-15		dBm
	MCS0		-15		dBm
	MCS9		-15		dBm
Adjacent Channel Rejection (20MHz offset)	6 Mbps OFDM		24		dB
	54 Mbps OFDM		7		dB
Adjacent Channel Rejection (20MHz offset), BW=20MHz	MCS 0		24		dB
	MCS 8		1		dB
Adjacent Channel Rejection (40MHz offset), BW=40MHz	MCS 0		24		dB
	MCS 9		3		dB
Adjacent Channel Rejection (80MHz offset), BW=80MHz	MCS 0		24		dB
	MCS 9		3		dB

Table 32 5GHz receiver specification(Aux)

g: Degraded by 1.5dB at 85°C

h: Sensitivity degradation at different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

6.1.5 2.4GHz Transmitter Specification

Note:

(1) The specification value is valid at room temperature (25°C).

(2) All specifications are measured at the RF port unless otherwise specified.

(3) Typical output power degradation around 3dB at FCC band edge channels

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz

Parameter	Description	Min.	Typ.	Max.	Unit
Output power VBAT = 3.8V	802.11b, 1~11 Mbps DSSS		22		dBm
	802.11g, 6 ~54Mbps OFDM		20		dBm
	802.11n, HT20 MCS0~7		18.5		dBm
	802.11n, HT40 MCS0~7		17.5		dBm
EVM	802.11b, 1~11 Mbps DSSS @Pout=22dBm		25		%
	802.11g, 6 ~54Mbps OFDM @Pout=20dBm		-28		dB
	802.11n, HT20 MCS0~7 @Pout=18.5dBm		-30		dB
	802.11n, HT40 MCS0~7 @Pout=17.5dBm		-30		dB
TX power accuracy	-40~85 °C,5~22dBm			±1.5	dB
Loadpull variation at VSWR = 2:1	Output power variation			±1.5	dB
	EVM degradation		4		dB
Transmitted power (Data rate = 6M, Pout = 20dBm)	76 ~ 108 MHz		-142		dBm/Hz
	776 ~ 794 MHz		-142		dBm/Hz
	869 ~ 960 MHz		-142		dBm/Hz
	925 ~ 960 MHz		-142		dBm/Hz
	1,570 ~ 1,580 MHz		-140		dBm/Hz
	1,805 ~ 1,880 MHz		-131		dBm/Hz
	1,930 ~ 1,990 MHz		-126		dBm/Hz
	2,110 ~ 2,170 MHz		-125		dBm/Hz
Harmonic output power (Data rate = 1M, Pout = 23dBm) [i]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

Table 33. 2.4GHz transmitter specification

i:Measurement at antenna port with a 2.4G BPF and a duplexer

6.1.6 5GHz transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency Range		4900	-	5925	MHz
Output Power VBAT=3.8V Spectral mask and EVM compliance[e]	6 ~54Mbps OFDM		18.5		dBm
	HT20/VHT20 MCS0~MCS7		17.5		dBm
	HT40/VHT40 MCS0~MCS7		17.5		dBm
	VHT20 MCS8		16		dBm
	VHT40 MCS9		15		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
	VHT80 MCS9		15		dBm
EVM	OFDM 54M @18.5dBm		-28		dB
	HT20/VTH20 MCS7@17.5dBm		-30		dB
	HT40/VTH40 MCS7@17.5dBm		-30		dB
	VHT20 MCS8@16dBm		-31		dB
	VHT40 MCS9@15dBm		-33		dB
	VHT80 MCS9@15dBm		-33		dB
TX Power Accuracy				±2	dB
Carrier Suppression				30	dBc
Return Loss					dB
Transmitted Power	76~108 MHz		-135		dBm/Hz
	776~794MHz		-135		dBm/Hz
	869~960 MHz		-135		dBm/Hz
	925~960 MHz		-135		dBm/Hz
	1570~1580 MHz		-135		dBm/Hz
	1805~1880MHz		-135		dBm/Hz
	1930~1990MHz		-135		dBm/Hz
	2110~2170MHz		-135		dBm/Hz
	2400~2483MHz		-135		dBm/Hz
Harmonic Output Power (Data rate = 6M, Pout = 18.5dBm)[j]	2nd Harmonic		-50		dBm/MHz

Table 3.4: 5GHz Transmitter Specification

j: Measure at antenna port with a diplexer

6.2 Bluetooth Radio Characteristics

6.2.1 Basic Data Rate

6.2.1.1 Receiver Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity	BER < 0.1%		-94		dBm
Max. usable signal	BER < 0.1%	-20	-5		dBm
C/I co-channel	Co-channel selectivity (BER	-	6	11	dB

Parameter	Description	Min.	Typ.	Max.	Unit
	< 0.1%)				
C/I 1MHz	Adjacent channel selectivity (BER < 0.1%)	-	-7	0	dB
C/I 2MHz	2nd adjacent channel selectivity (BER < 0.1%)	-	-40	-30	dB
C/I ≧3MHz	3rd adjacent channel selectivity (BER < 0.1%)	-	-43	-40	dB
C/I image channel	Image channel selectivity (BER < 0.1%)	-	-20	-9	dB
C/I image 1MHz	1MHz adjacent to image channel selectivity (BER < 0.1%)	-	-35	-20	dB
Out-of-band blocking*	30MHz to 2,000MHz	-4			dBm
	2,001MHz to 2,339MHz	-1			dBm
	2,501MHz to 3,000MHz	-8			dBm
	3,001MHz to 12.75GHz	1			dBm
Intermodulation	Max. interference level to maintain 0.1% BER	-30			dBm

Table 35. Basic data rate receiver specification

6.2.1.2 Transmitter Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power	At max power output level		8		dBm
Power control step		2	4	8	dB
ICFT	Initial carrier frequency drift	-75	±18	75	kHz
Carrier frequency drift	One slot packet (DH1)	-25	±10	25	kHz
	Three slot packet (DH3)	-40	±10	40	kHz
	Five slot packet (DH5)	-40	±10	40	kHz
	Max. drift rate	-	200	400	Hz/us
Modulation characteristic	$\triangle f1_{avg}$	140	156	175	kHz
	$\triangle f2_{max}$ (for at least 99% of all $\triangle f2_{max}$)	115	145	-	kHz
	$\triangle f2_{avg}/\triangle f1_{avg}$	0.8	0.98	-	
20-dB bandwidth		-	922	1,000	kHz
In-band spurious emission	±2MHz offset		-38	-20	dBm
	±3MHz offset		-43		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
	>±3MHz offset		-45		dBm
Out-of-band spurious emission**	30MHz to 1GHz			-64	dBm
	1GHz to 12.75GHz			-50	dBm
	1.8GHz to 1.9GHz			-50	dBm
	5.15 to 5.3GHz			-50	dBm

Table 36. Basic data rate transmitter specification

6.2.2 Enhanced Data Rate

6.2.2.1 Receiver Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	π/4 DQPSK (BER < 0.01%)	-	-95	-70	dBm
	8PSK (BER < 0.01%)		-89	-70	dBm
Max. usable signal	π/4 DQPSK (BER < 0.1%)	-20	-5	-	dBm
	8PSK (BER < 0.1%)	-20	-5	-	dBm
C/I co-channel	π/4 DQPSK (BER < 0.1%)	-	9	13	dB
	8PSK (BER < 0.1%)	-	16	21	dB
C/I 1MHz	π/4 DQPSK (BER < 0.1%)	-	-12	0	dB
	8PSK (BER < 0.1%)	-	-6	5	dB
C/I 2MHz	π/4 DQPSK (BER < 0.1%)	-	-40	-30	dB
	8PSK (BER < 0.1%)	-	-36	-25	dB
C/I ≧3MHz	π/4 DQPSK (BER < 0.1%)	-	-43	-40	dB
	8PSK (BER < 0.1%)	-	-40	-33	dB
C/I image channel	π/4 DQPSK (BER < 0.1%)	-	-20	-7	dB
	8PSK (BER < 0.1%)	-	-15	0	dB
C/I image 1MHz	π/4 DQPSK (BER < 0.1%)	-	-40	-20	dB
	8PSK (BER < 0.1%)	-	-30	-13	dB

Table 37. Enhanced data rate receiver specification

6.2.2.2 Transmitter Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Output power	π/4 DQPSK		9		dBm
	8PSK		9		dBm

Parameter	Description		Min.	Typ.	Max.	Unit
Relative transmit power	π/4 DQPSK		-4	-1.7	1	dB
	8PSK		-4	-1.7	1	dB
Frequency stability	ω_0	π/4 DQPSK	-10	±4	10	kHz
		8PSK	-10	±4	10	kHz
	ω_i	π/4 DQPSK	-75	±18	75	kHz
		8PSK	-75	±18	75	kHz
	$\lvert\omega_0+\omega_i\rvert$	π/4 DQPSK	-75	±20	75	kHz
		8PSK	-75	±20	75	kHz
Modulation accuracy	RMS DEVM	π/4 DQPSK	-	8	20	%
		8PSK	-	8	13	%
	99% DEVM	π/4 DQPSK	-	11	30	%
		8PSK	-	11	20	%
	Peak DEVM	π/4 DQPSK	-	15	35	%
		8PSK	-	15	25	%
In-band spurious emission	±1MHz offset	π/4 DQPSK		-29		dB
		8PSK		-29		dB
	±2MHz offset	π/4 DQPSK		-23		dBm
		8PSK		-23		dBm
	±3MHz offset	π/4 DQPSK		-40		dBm
		8PSK		-40		dBm

Table 38. Enhanced data rate transmitter specification

6.2.3 Bluetooth LE Radio Performance

6.2.3.1 Receiver Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity (*)	PER < 30.8%		-98	-70	dBm
Max. usable signal	PER < 30.8%	-10	-5		dBm
C/I co-channel	Co-channel selectivity (PER < 30.8%)		6	21	dB
C/I 1MHz	Adjacent channel selectivity (PER < 30.8%)		-7	15	dB
C/I 2MHz	2nd adjacent channel selectivity (PER < 30.8%)		-30	-17	dB
C/I ≧3MHz	3rd adjacent channel selectivity		-33	-27	dB

Parameter	Description	Min.	Typ.	Max.	Unit
	(PER < 30.8%)				
C/I Image channel	Image channel selectivity (PER < 30.8%)		-20	-9	dB
C/I Image 1MHz	1MHz adjacent to image channel selectivity (PER < 30.8%)		-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz			-30	dBm
	2,001MHz to 2,339MHz			-35	dBm
	2,501MHz to 3,000MHz			-35	dBm
	3,001MHz to 12.75GHz			-30	dBm

Table 39. Bluetooth LE receiver specification

6.2.3.2 Transmitter Specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power(*)	At max. power output level	-20	3	10	dBm
Carrier frequency offset and drift	Frequency offset	-150	±10	150	kHz
	Frequency drift	-50	±10	50	kHz
	Max. drift rate	-20	±10	20	Hz/us
Modulation characteristic	$\triangle f1_{avg}$	225	251	275	kHz
	$\triangle f2_{max}$ (For at least 99% of all $\triangle f2_{max}$)	185	215		kHz
	$\triangle f2_{avg}/\triangle f1_{avg}$	0.8	0.88		
In-band spurious emission	±2M offset		-35	-20	dBm
	±3MHz offset		-40	-30	dBm

(*) means chip RF terminals.

Table 40. Bluetooth LE transmitter specification

* The measurement is not include exceptions in these band. Exceptions can pass Bluetooth SIG spec.

** The measurement is at Bandpass filter output.

6.3 GPS Radio Characteristics

6.3.1 RX chain

Parameter	Condition	Min.	Typ.	Max.	Unit

RF input frequency (GPS/Galileo)		-	1575.4	-	MHz
RF input frequency (BEIDOU)			1561.098		MHz
RF input frequency (GLONASS)			1601.71		MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Differential input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)		80	76	70	dB
NF		-	2.2	-	dB

Table 41. RX chain specification

6.3.2 GPS Performance

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Horizontal position accuracy (a)	Without aid		3.0		Meter
	DGPS		2.5		Meter
Velocity accuracy	Without aid		0.1		Meter/Sec
	DGPS		0.05		Meter/Sec
Sensitivity	Autonomous acquisition		-148		dBm
	Warm acquisition		-151		dBm
	Hot acquisition		-163		dBm
	Tracking		-165		dBm
Time To First Fix (b)	Cold start: Autonomous		< 35		Sec
	Warm start: Autonomous		< 34		Sec
	Hot start: Autonomous		<1		Sec
Time To First Fix (b)	MS based: GSM coarse time		< 20		Sec
	MA based: GSM coarse time		< 20		Sec

(a) 2D RMS

(b) Signal power = -130dBm, Fu 0.5 ppm, Tu ±2s, Pu 30km

Table 42. GPS receiver performance

6.4 FM Radio Characteristics

6.4.1 FM RX Radio Characteristics

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98MHz, default register settings and under recommended operating conditions. The min/max specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

Description	Condition	Min.	Typ.	Max.	Unit
Input frequency range		65		108	MHz
Sensitivity (long antenna)[1,3]	SINAD= 26dB, unmatched		3		dBμVemf
	SINAD= 26dB, matched		2		dBμVemf
RDS sensitivity (long antenna)	Δf = 2kHz, BLER < 5%, unmatched		18		dBμVemf
Sensitivity (short antenna)[1,3]	(S+N)/N = 26dB, unmatched		3		dBμVemf
RDS sensitivity (short antenna)	Δf = 2kHz, BLER < 5%, unmatched		19		dBμVemf
LNA input resistance[4]	Long antenna port		2.4k		Ohm
LNA input capacitance[4]	Long antenna port		8		pF
AM suppression[1,4]	m = 0.3		58		dB
Adjacent channel selectivity[1,4]	±200kHz		53		dB
Alternate channel selectivity[1,4]	±400kHz		66		dB
Spurious response rejection[4]	In-band		55		dB
Maximum input level				130	dBμVemf
Audio mono SINAD[1,3,4]		56	60		dB
Audio stereo SINAD[2,3,4]		51	55		dB
Audio stereo separation[4]	Δf = 75kHz		45		dB
Audio output load resistance	Single-ended at AFR/AFL outputs		10k		Ohm
Audio output load capacitance	Single-ended at AFR/AFL outputs		12.5		pF
Audio output voltage[1,4]	At AFR/AFL outputs		80		mVrms
Audio output THD[1,4]			0.05	0.1	%
Audio output frequency range	3dB corner frequency	30		15k	Hz

Description	Condition	Min.	Typ.	Max.	Unit
[1] Δf = 22.5kHz, fm = 1kHz, mono, L = R					
[2] Δf = 22.5kHz, fm = 1kHz, 50μs de-emphasis, stereo					
[3] A-weighting, BW = 300Hz to 15kHz					
[4] Vin = 60dBμVemf					
[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, it is recommended to use a reference clock of accuracy within ±100ppm so as not to affect the quality of channel scan.					

Table 43. FM receiver specification

6.4.2 FM TX Radio Characteristics

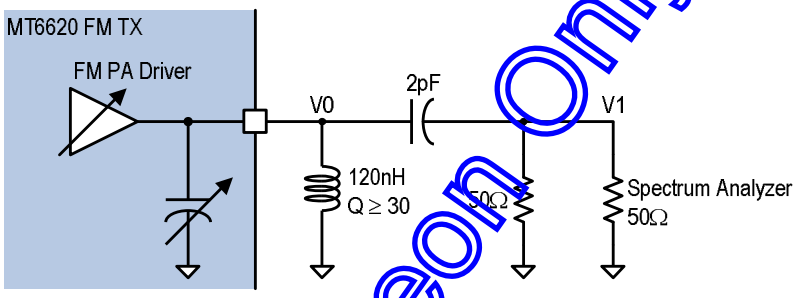

Figure 40 FM TX spec. measurement diagram

Unless otherwise stated, all transmitter characteristics are applicable under recommended operating conditions or typ. operating conditions. Measured at 50Ω load (node V1 in Figure 42) after automatic PA frequency tuning; default test condition is Pout=120dBuVrms (node V0 in Figure 42), unless otherwise specified.

Description	Condition	Min.	Typ.	Max.	Unit
TX Frequency Range		65		108	MHz
TX Frequency Accuracy	The same as XTAL accuracy			100	ppm
Maximum transmit output level	Output into an antenna with L = 120 nH, Q ≧30, and a 2.8V supply		120		dBμV
Output Power Accuracy	Over entire output range	-2		+2	dB
Output Power Temperature Coefficient			0.025		dB/°C
Channel Edge Power	±100kHz[1,3]			-20	dBc
Adjacent Channel Power	±200kHz[1,3]		-35	-30	dBc
Alternate Channel Power	±400kHz[1,3]		-50	-45	dBc
Output Capacitance		5		40	pF
Pre-emphasis Time	75μs pre-emphasis		75		μs

Constant	50μs pre-emphasis		50		
Audio Mono SNR[2]			57		dB
Audio Stereo SNR[3]			52		dB
Audio THD Mono[2]			0.08		%
Audio THD Stereo[3]			0.1		%
Audio Stereo Separation[3]		40	42		dB
Sub-carrier Rejection Ratio[3]			65		dB
Pilot Modulation Rate Accuracy[3]			+/- 2	+/- 5	%
Audio Modulation Rate Accuracy[3]			+/- 5	+/- 8	%
Spurious Emissions[1,2]	200kHz BW				dBm
	746-764 MHz		-86		
	869-894MHz		-110		
	925-960MHz		-91		
	1570-1580MHz		-103		
	1805-1880MHz		-105		
	1930-1990MHz		-105		
	2110-2170MHz		-91		
	2400-2500MHz		-110		
[1] 200kHz BW, pre-emphasis OFF					
[2] Δf=22.5kHz, fm=1kHz, 75μs de-emphasis, mono, L=R, limiter OFF					
[3] Δf=22.5kHz, Δfpilot=6.75kHz, fm=1kHz, 75μs de-emphasis, stereo, L only, limiter OFF					
[4] Δf=75kHz, fm=1kHz, 75μs de-emphasis, mono, L=R, limiter OFF					
[5] Δf=68.25kHz, Δfpilot=6.75kHz, fm=1kHz, 75μs de-emphasis, stereo, L only, limiter OFF					
[6] Δf=68.25kHz, Δfpilot=6.75kHz, fm=1kHz, 75μs de-emphasis OFF, stereo, L only, limiter OFF					

Table 44. FM transmitter specification

6.5 Current Consumption

6.5.1 WLAN Current Consumption

Description	Performance	
	Typ.	Unit
OFF	NA	μA
RX active, BW40, HT40 MCS7	59.2	mA
RX active, BW20, HT20 MCS7	53.6	mA
RX listen	47	mA
RX sleep	0.1	μA

RX power saving, DTIM = 1	0.6	mA
TX HT40, MCS7@19.5dBm	229	mA
TX HT20, MCS7@19.5dBm	230	mA
TX OFDM, 54M@18dBm	247	mA
TX CCK, 11M@21dBm	311	mA

Table 45. WLAN 2.4GHz current consumption

Description	Performance	
	Typ.	Unit
RX active, BW40, VHT40 MCS9	83	mA
RX active, BW80, VHT80 MCS9	95	mA
RX listen	47	mA
RX power saving, DTIM = 1	0.6	mA
TX HT40, MCS9@16.5dBm	402.6	mA
TX HT80, MCS9@16.5dBm	409.5	mA

Table 46. WLAN 5GHz current consumption

6.5.2 BT Current Consumption

Description	Performance	
	Typ.	Unit
Sleep	100	µA
Standard 2.56s inquiry scan	250	µA
2.56s inquiry scan & 1.28s page scan	588	µA
2.56s inquiry scan & 1.28s page scan (low-power scan)	395	uA
500ms sniff (master)	370	µA
500ms sniff (slave)	310	uA
HV3 + 500ms Sniff + 2.56s inquiry scan & 1.28s page scan (master)	22	mA
2-EV3 (Tesco = 12) + 500ms sniff + 2.56s inquiry scan & 1.28s page scan (master)	17	mA
DH1 transmit (test mode)	73	mA
DH3 transmit (test mode)	73	mA

Table 47. BT current consumption

Description	Performance	
	Typ.	Unit
RX current consumption (test mode)	29	µA

TX current consumption (0dBm output power @test mode)	55	μA
TX current consumption (-10dBm output power @test mode)	41	μA
TX current consumption (-20dBm output power @test mode)	35	uA

Table 48. ANT T/RX current consumption

6.5.3 GPS Current Consumption

Description	Performance	
	Typ.	Unit
GPS acquisition	16.5	mA
GPS track	13.2	mA

Table 49. GPS power consumption

6.5.4 FM Current Consumption

Description	Performance	
	Typ.	Unit
FM Receiver	12.6	mA
FM Transmitter	13.8	mA

Table 50. FM current consumption

ESD CAUTION

MT6630QA is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT6630 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.

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