
Platform : ATX

P54C,P55C,6X86,K5

SIMM : SOCKET 2 X 72 Pins

SIMM :5V - EDO,FPM DRAM

CACHE : ON BOARD 256K/512K PBSRAM/M-CACHE

BIOS : 5V,12V FLASH ROM,2 Mbits FLASH ROM

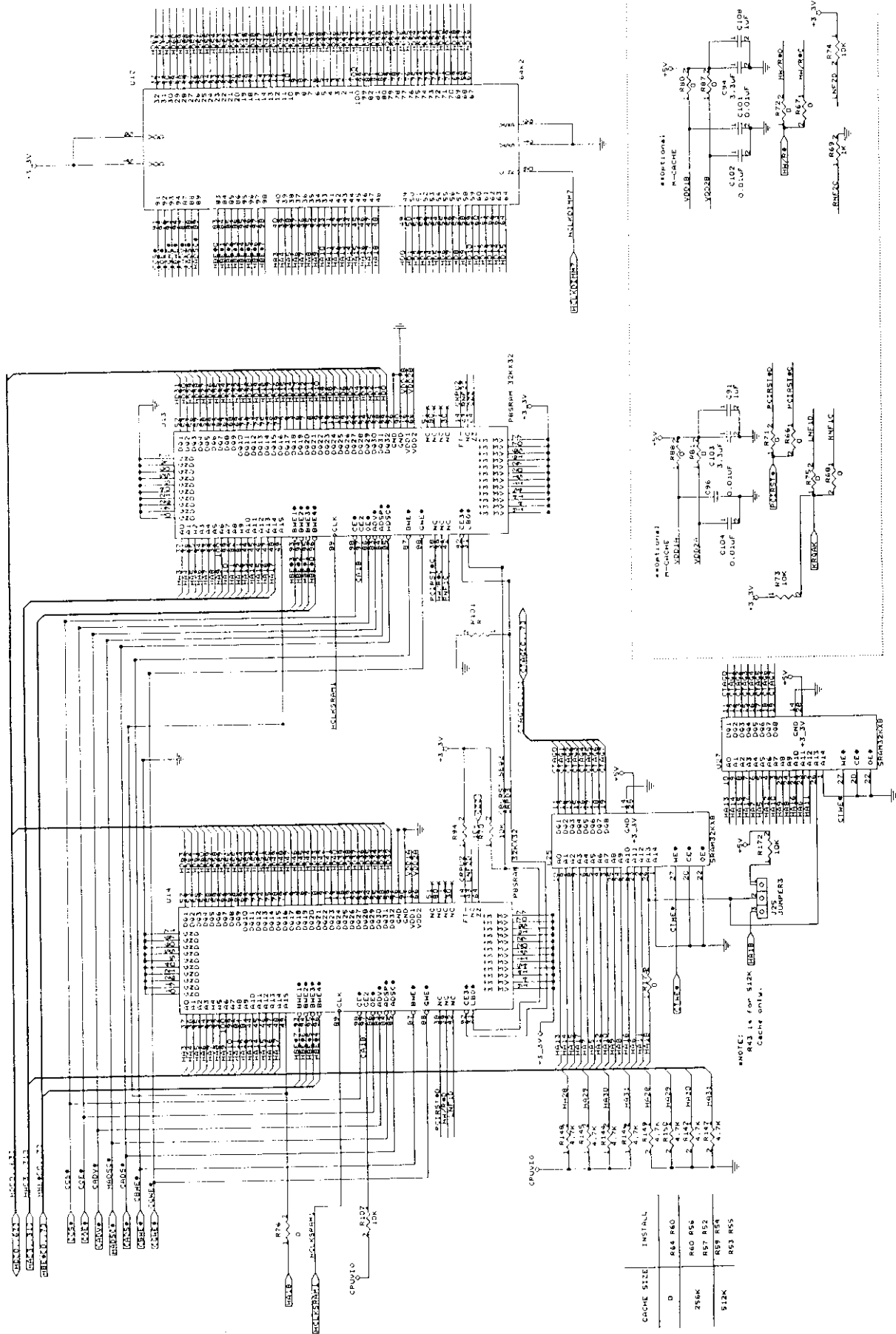
USB : 2

IO : SMC 37C672

ULTRA DMA 33 IDE PORT X 2

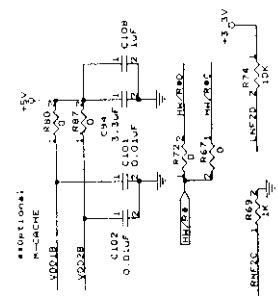
ILINK
IP54C.SCH
ISYSCLK.SCH
IMTXC_A.SCH
IMTXC_B.SCH
ICACHE.SCH
ISIMM.SCH
PIIX4_A.SCH
PIIX4_B.SCH
IDE&USB.SCH
ISUPER_IO.SCH
ICDM_PORT.SCH
IBIOS.SCH
IPOWER.SCH
IVOLT_REG.SCH
IDECUP.SCH
IPULLUP.SCH
IRTC_KBC.SCH
IT2_ISA16.SCH

NOTE: PIN 30, 39, 42, 43 & 44 MUST BE CONNECTED FOR PB 38MM

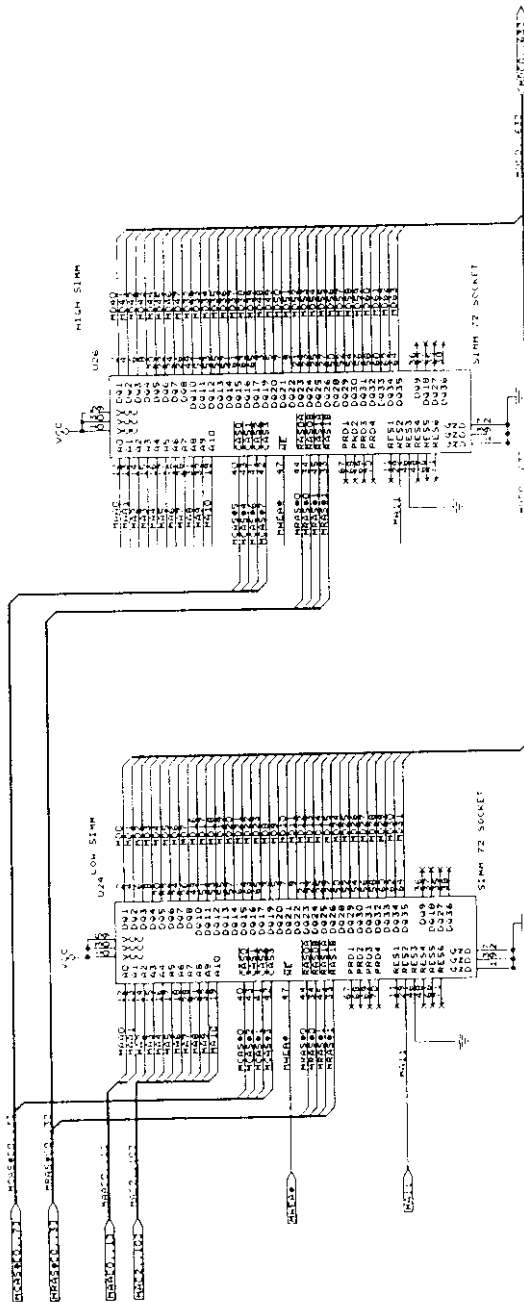


CACHE SIZE	INSTALL
D	844 860
256K	860 856
512K	856 854
	854 855

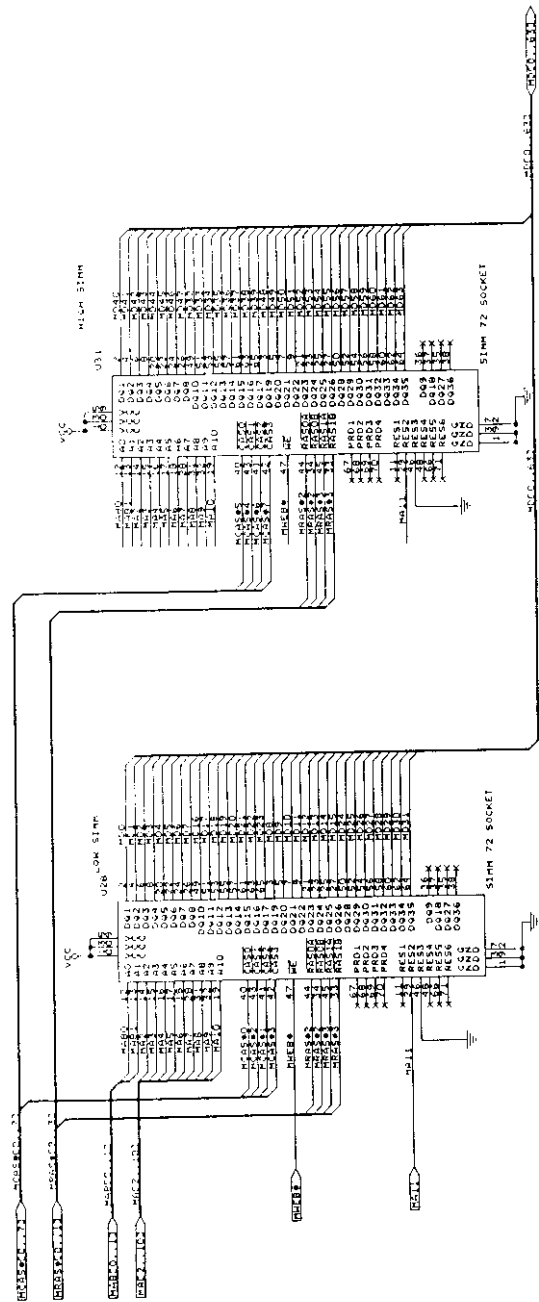
NOTE: R43 is for 512K cache only.

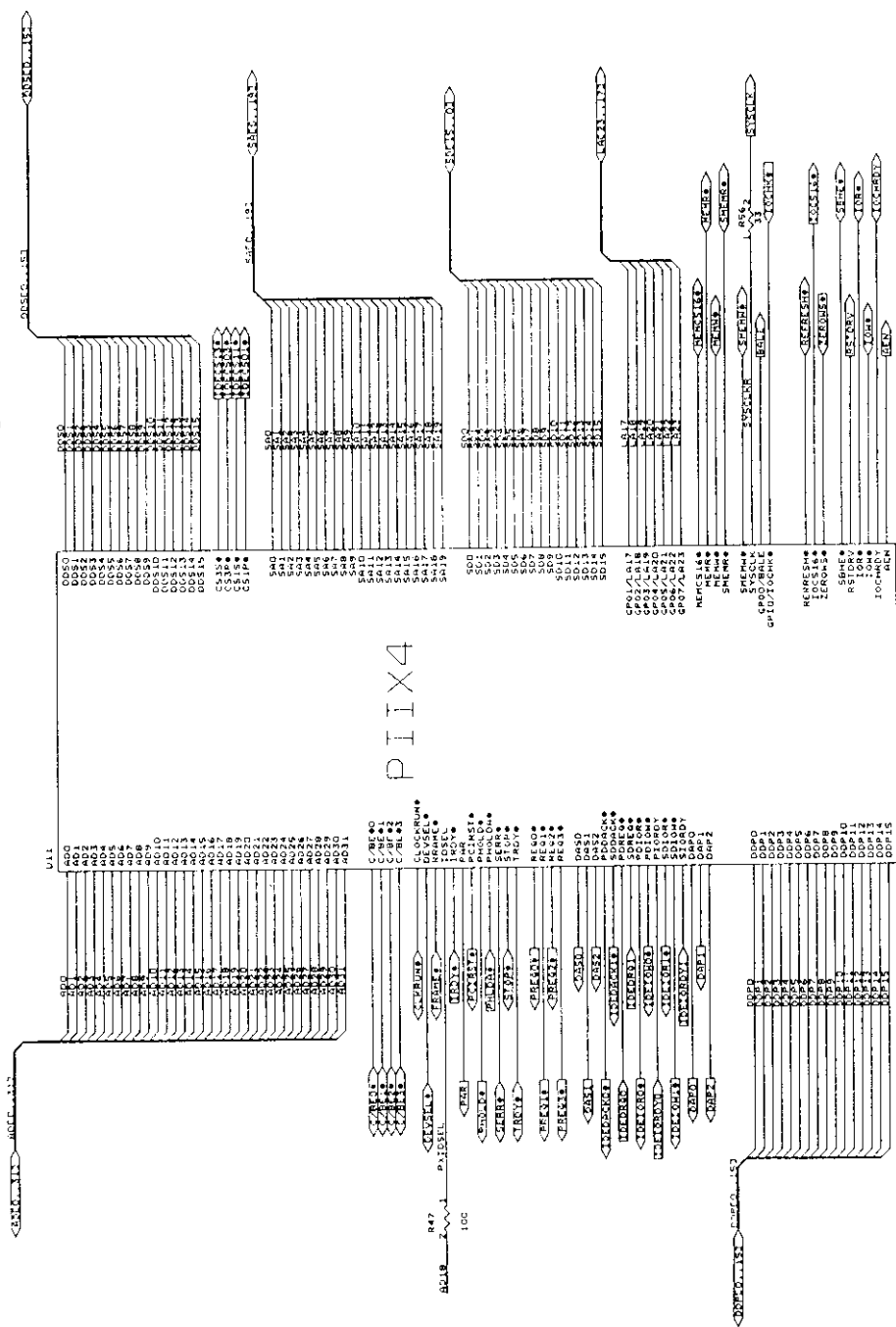


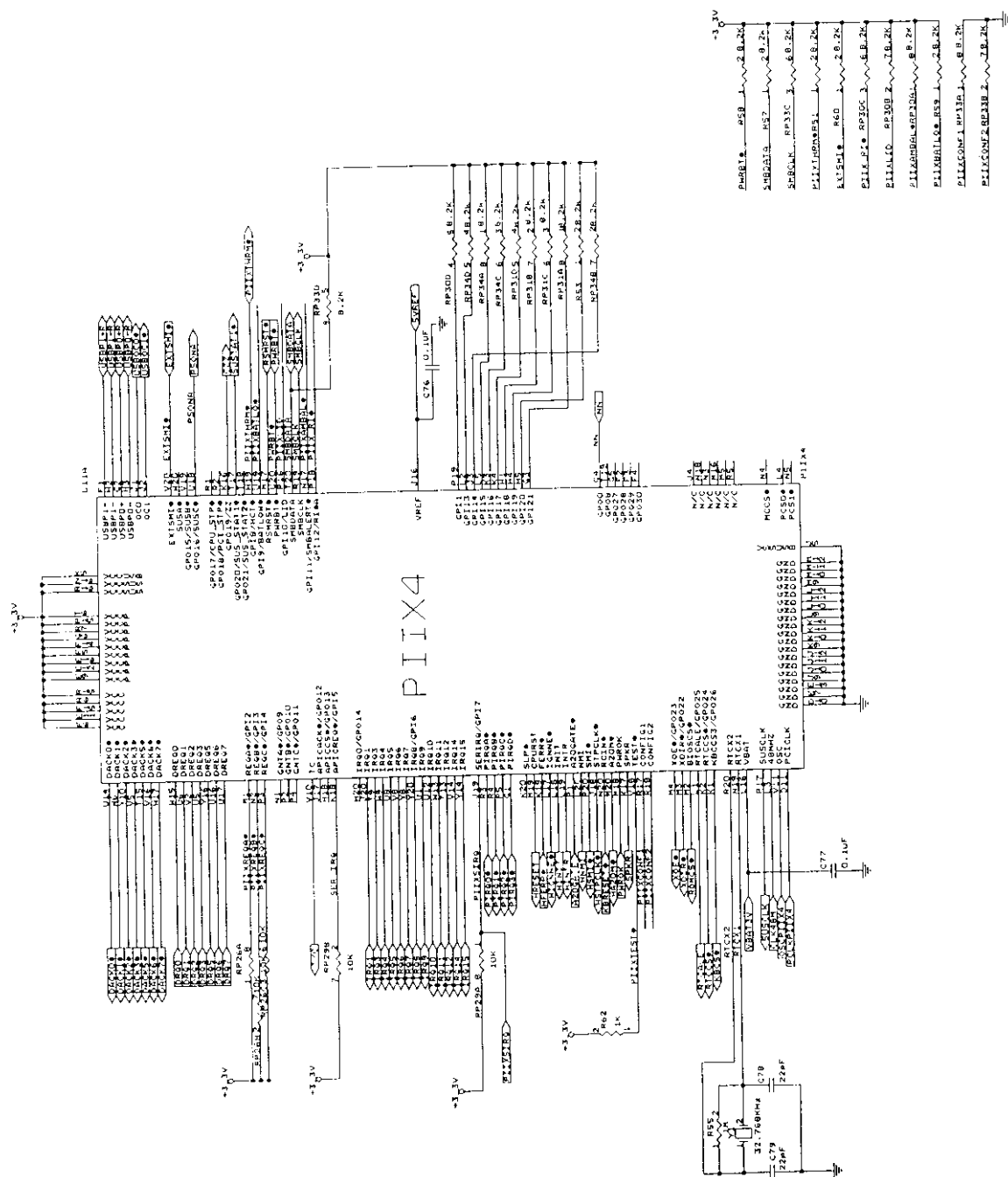
SIMM BANK 0

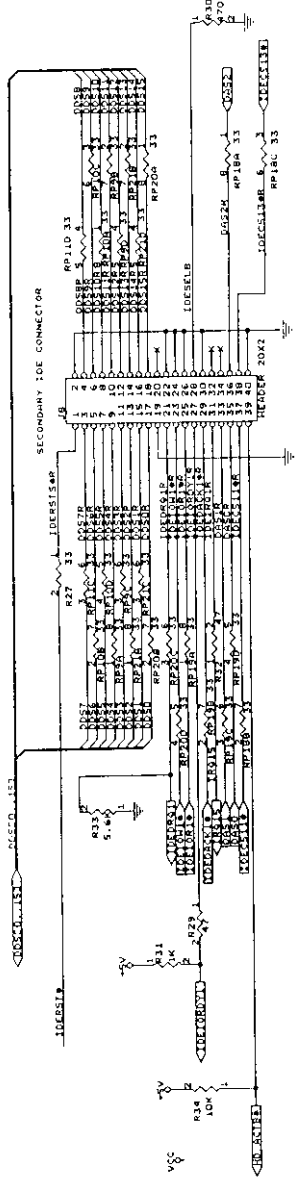
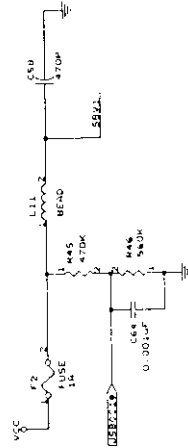
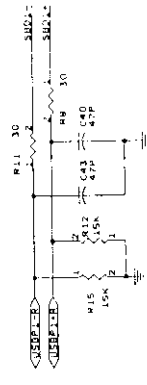
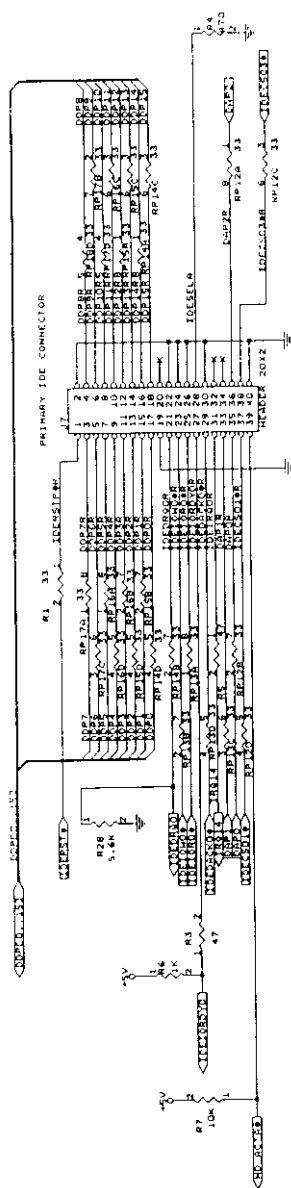


SIMM BANK 1

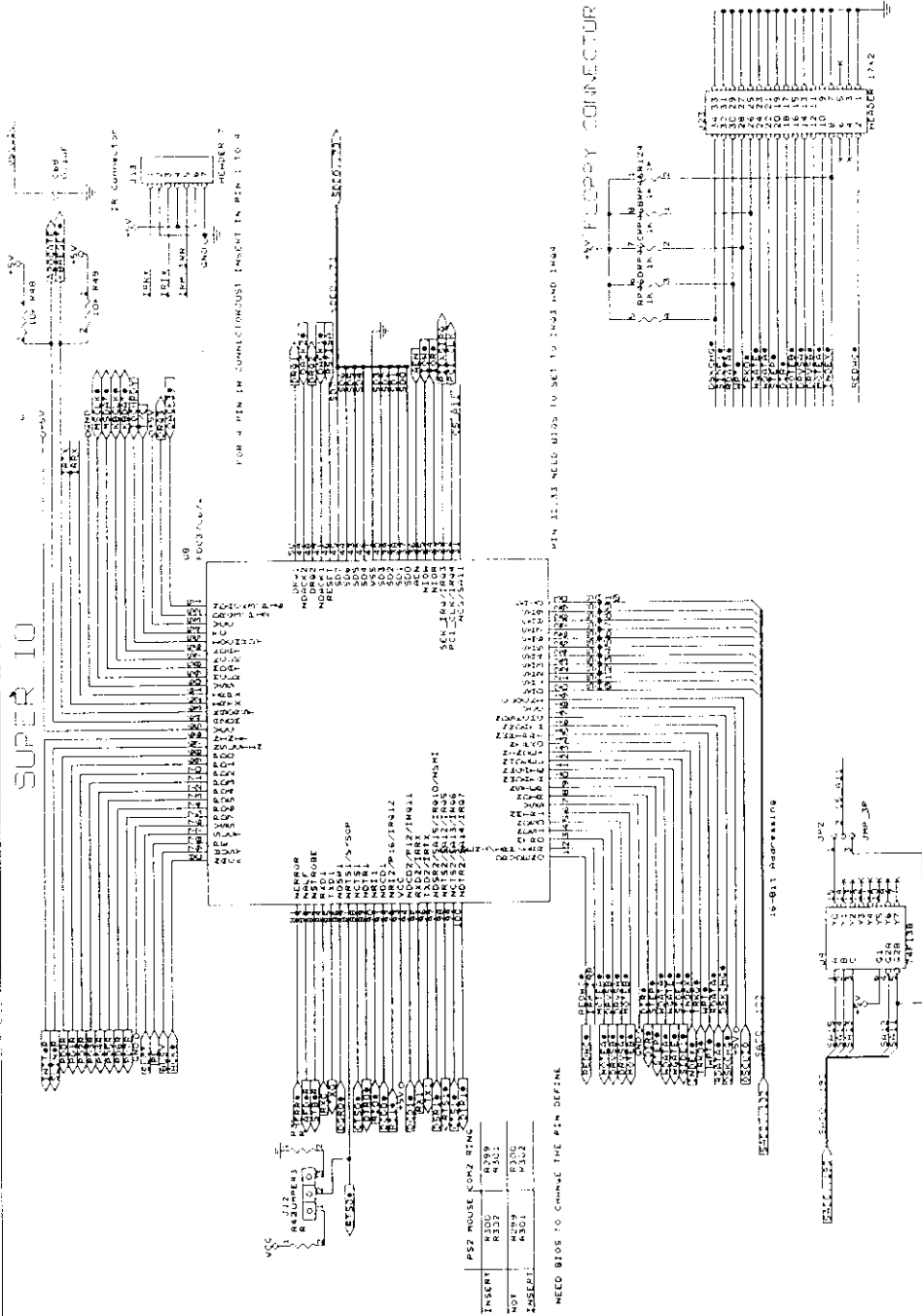


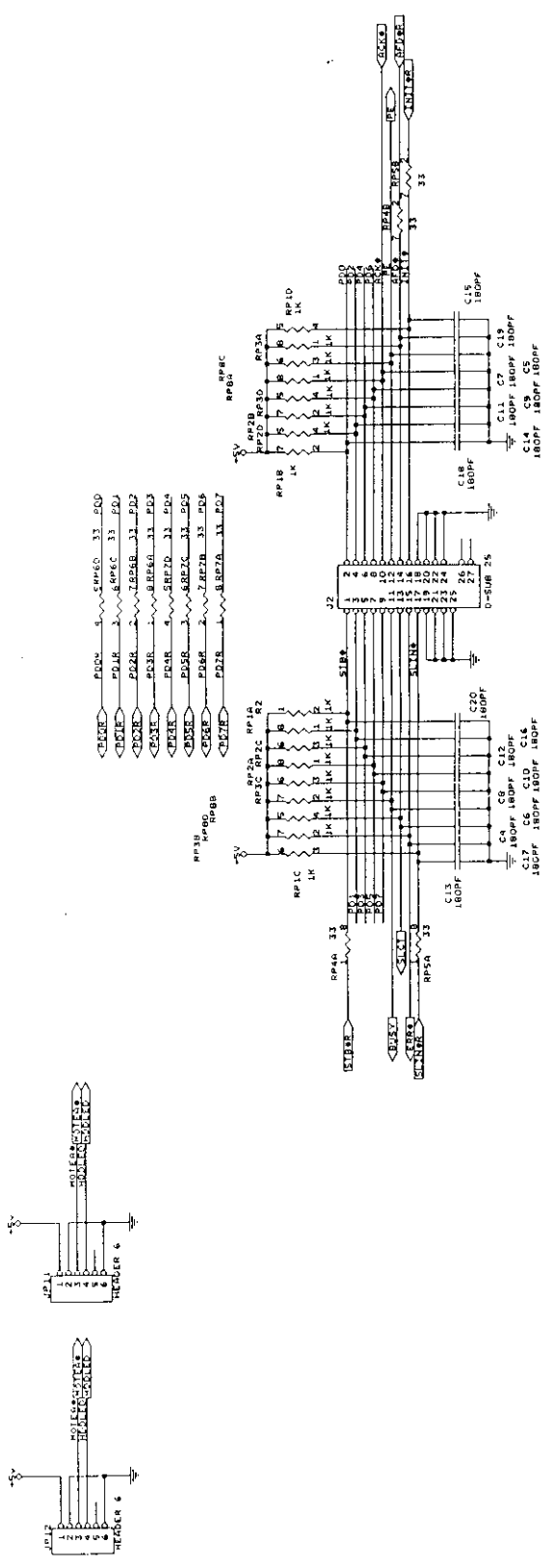
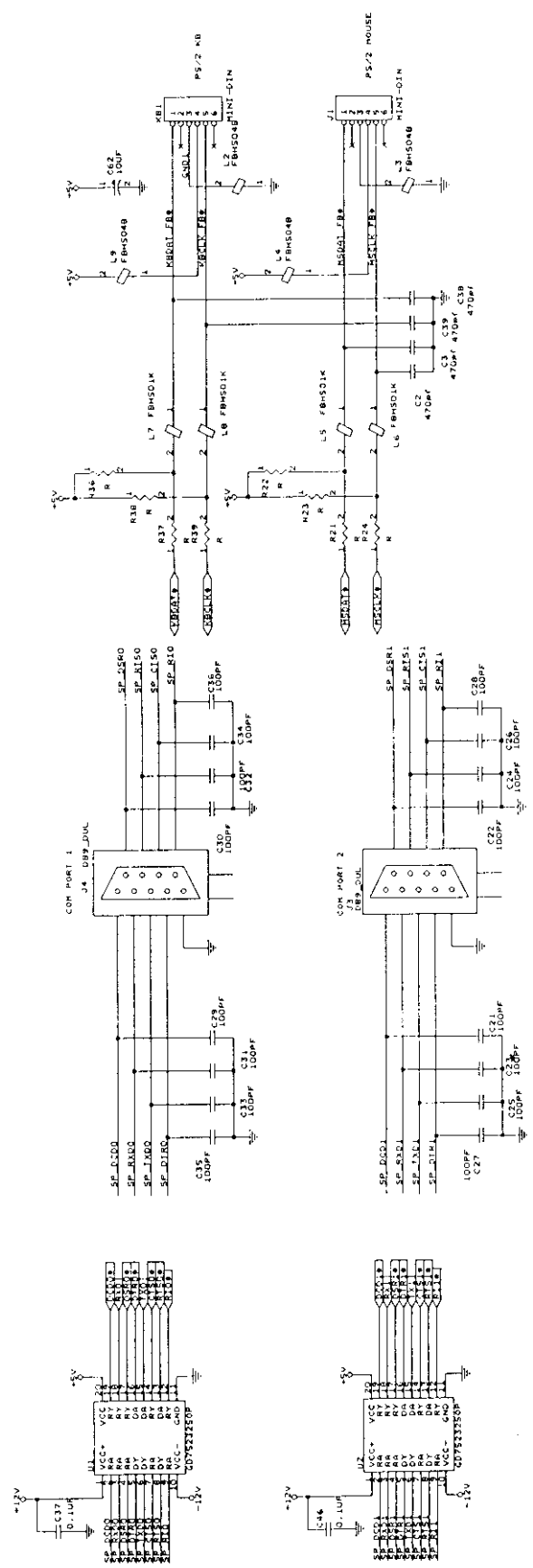




[illegible]

USB CONNECTOR





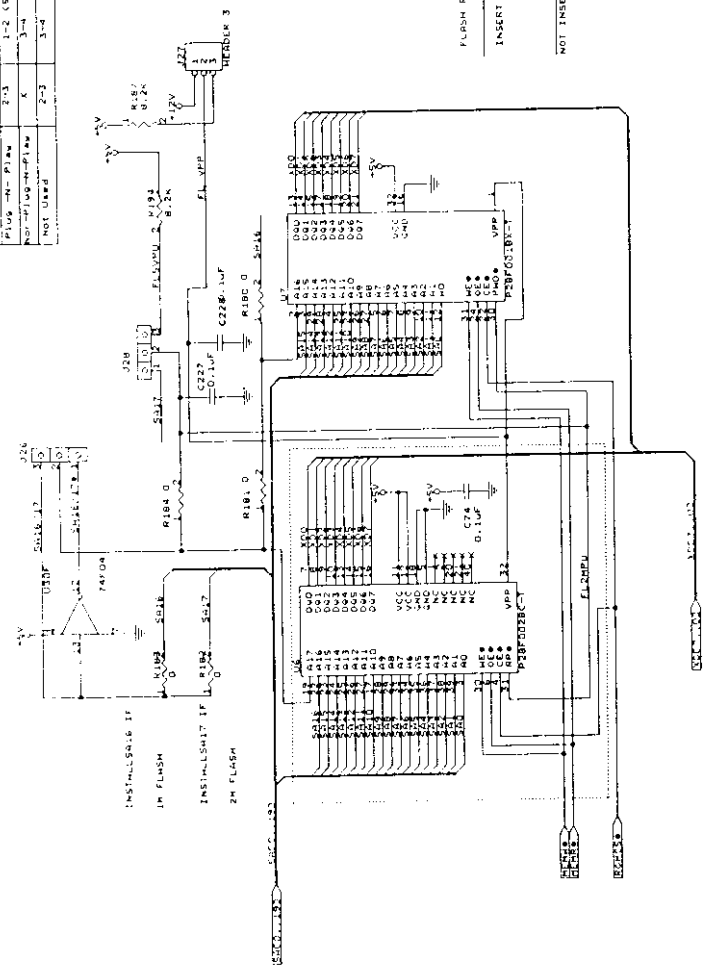
PARALLEL PORT

MODE	POS.
NORMAL	2-3
RECOVERY	1-2

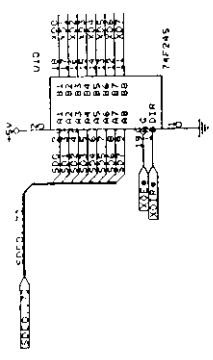
J1

NOTE: The X denotes a don't care.

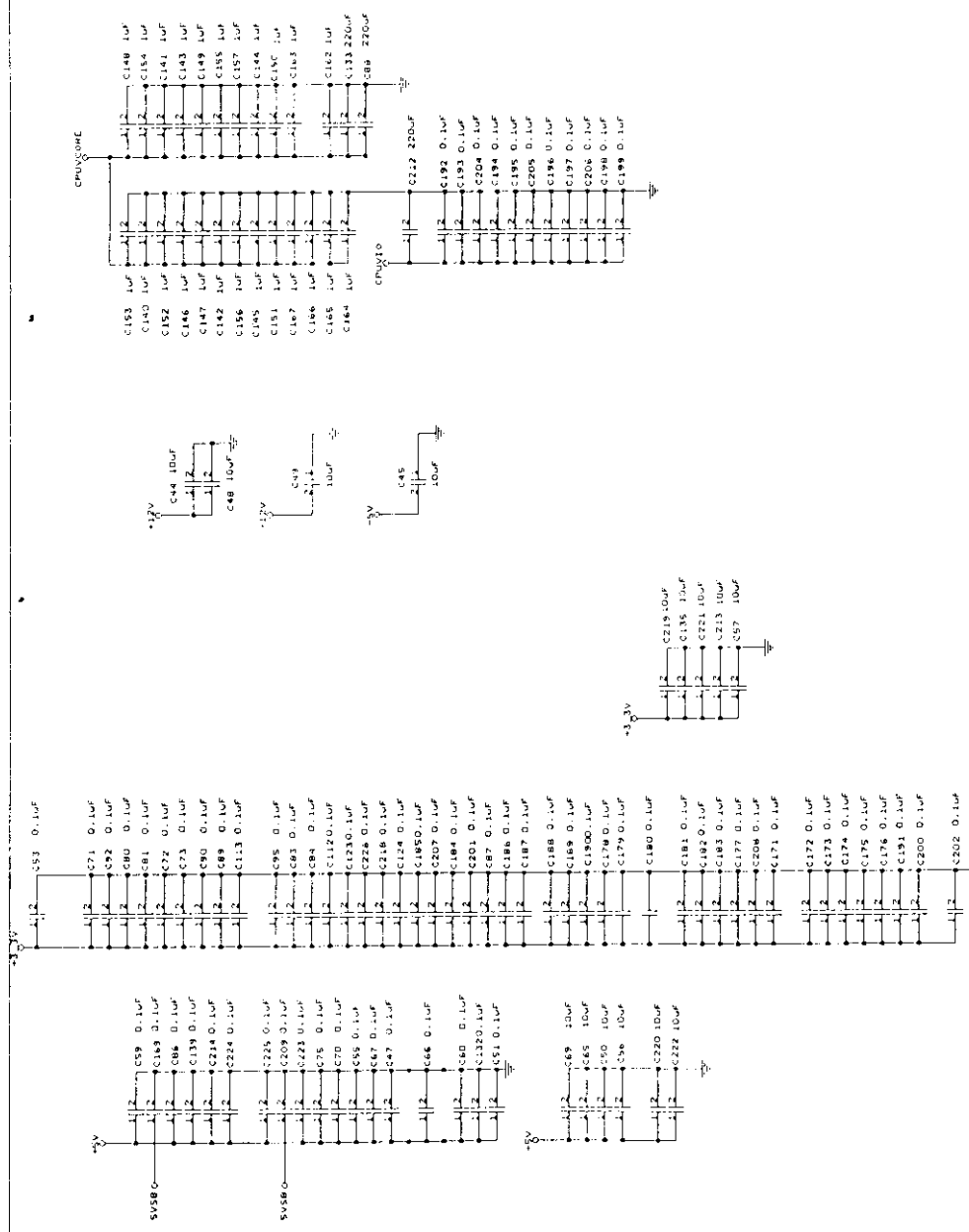
MODE	J1	J6
Program Device	1-2	1-2
Plug-in Pin	2-3	1-2 (ON AND 2M bits)
Not Used	2-3	3-4
NOT USED	2-3	3-4

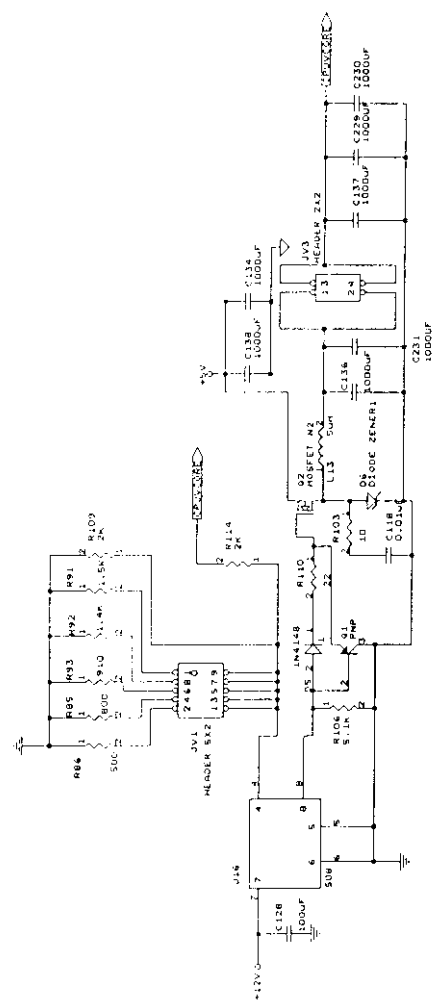
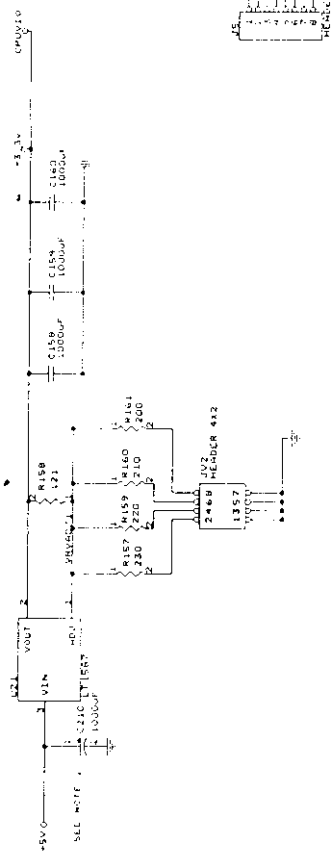


OPTIONAL 2M FLASHED PIN - 401P



FLASH ROM	INTEL	28010	28020
INSERT	R1	R2	R2
NOT INSERT	R2	R1	R2





Resistors are implemented as copper traces on inter layer.
 For 10% copper:
 Note 1: trace widths are 50 mils, 1.24" long.
 Note 2: trace widths are 50 mils, 0.83" long.

1. The first part of the document is a list of names and addresses of the members of the committee.

2. The second part of the document is a list of names and addresses of the members of the committee.

3. The third part of the document is a list of names and addresses of the members of the committee.

