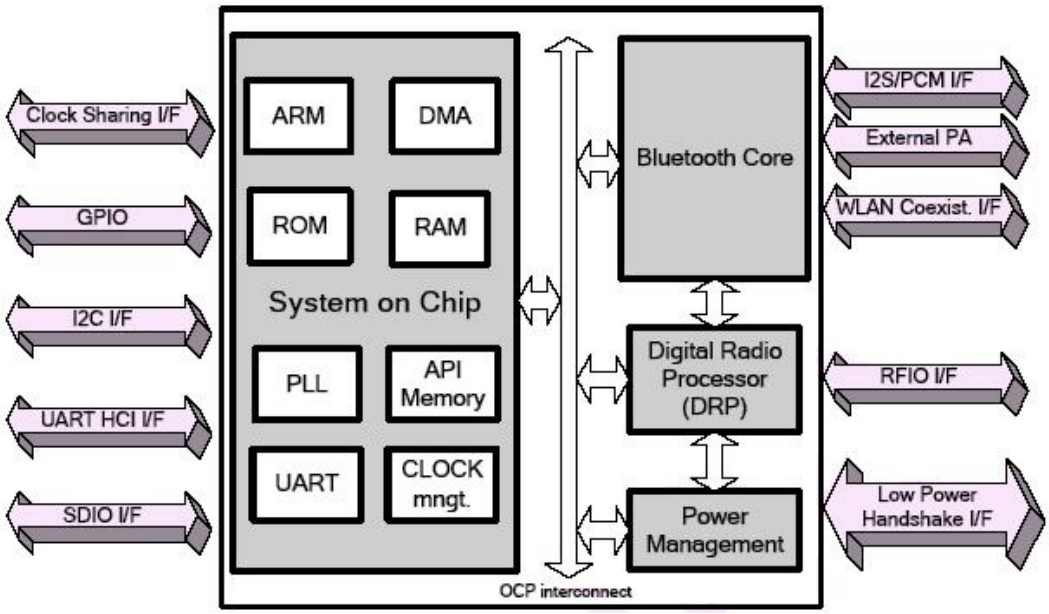
Bluetooth Hardware Structure

1.1. Block Diagram



1.2. BRF6300

The BRF6300 chip is a highly integrated single-chip CMOS Bluetooth device that forms a complete standalone Bluetooth wireless communication system. The BRF6300 is based on the BRF6150 and is pin-to-pin backwards compatible with the BRF6150 device when VDD_IO of 1.8V is used. The BRF6300 is the third generation of TI's single chip device, succeeding the BRF6150 and the BRF6100.

This device implements and advanced solution for the Bluetooth protocol with easy interfacing to a host system. The BRF6300 comprises:

-Digital Radio Processor (DRP)

-Embedded Bluetooth point-to-multipoint hardware core for highly optimized execution of the Bluetooth protocol according to Bluetooth Specification 1.1 and 1.2 and 2.0 (including EDR 2/3Mbps)

-On-chip ROM

-On-chip RAM

-Embedded ARM7TDMIE Microprocessor

Transmitter

The transmitter is based on an all-digital sigma-delta PLL with a digitally controlled oscillator (DCO) at 2.4GHz as the RF frequency clock. The modulation is achieved by directly modulating the digital PLL within a closed loop. The power amplifier is digitally controlled.

For EDR modulation, the transmitter uses a Polar-Modulation technique. In this mode, in addition to the frequency-modulation that controls the direct-modulated ADPLL, an

amplitude controls modulates the PA. to support this, a new block called Digital-Transmitter is added. This block gets the input bit-stream and converts these signal to phase-modulated control-words. The phase-modulated digital signal is than processed to provide frequency-modulation control to the ADPLL.

Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. The external Balun is followed by an internal RF switch and a differential LNA (low-noise amplifier). This signal is than passed to a Sampling Mixer which down-converts the signal onto an IF, followed by a filter and an amplifier. This signal is quantized by a sigma-delta ADC. This quantized signal is than further processed to reduce the level of interference.

The demodulator then digitally down converts the signal to zero IF and recovers the data bit-streams by an adaptive decision mechanism. This demodulation includes EDR process with a state-of the art performance. This demodulator includes an MLSE (mean least square evaluation) for improved performance of GFSK sensitivity (in Basic-Rate) and an Adaptive-Equalization for enhancing EDR modulated signal reception.