T 020-MS-OM-A2 IRF9096DS
T 021-MS-OM-A2 IRF9192DS
T 022-MS-OM-A2 IRF9250DS

Single VCO 900MHz RF Module

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1999/6/8

InnoMedia IRF9XXXDS

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INTRODUCTION

InnoMedia IRF9XXXDS RF Module is a radio transceiver that provides all of the baseband-to-RF and RF-to-baseband signal conversion functions needed for 902 - 928 MHz digital communication. It can accompany the ALFA AIC9001 Spread Spectrum Transceiver integrated circuit to support either digital voice or data communication, in both full-duplex and half-duplex operations. The IRF9XXXDS's high performance, compact size and low power consumption make it ideal for portable, battery-powered wireless products such as digital cordless phone and wireless modem. It also can meet FCC part requirements to let your wireless products get FCC approval easily. Figure 1 and 2 show the typical system applications for cordless phone and wireless modem.

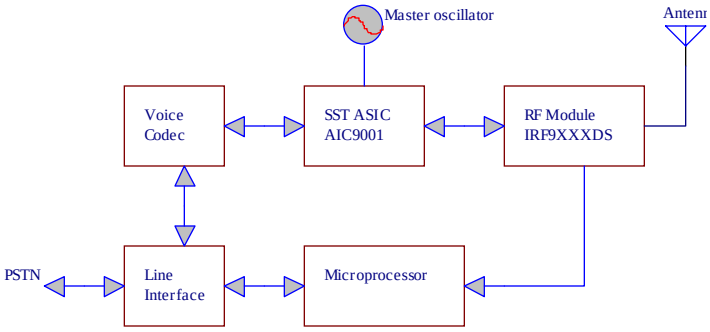


Figure 1. Block diagram of Cordless phone

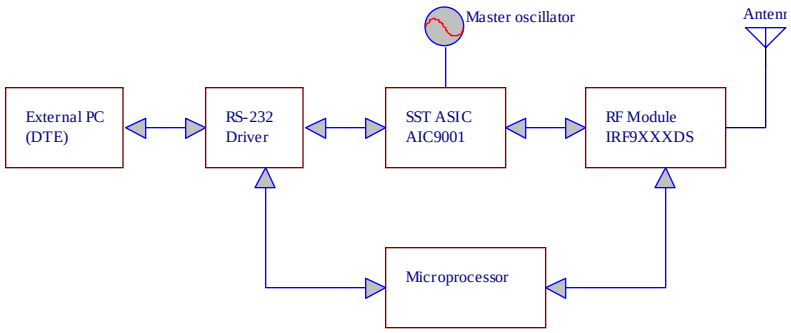


Figure 2. Block diagram of Wireless modem

FEATURES

- Designed for 902-928 MHz wireless communication systems.
- Time Division Duplexing (TDD).
- GMSK Modulation/Demodulation.
- Single conversion receiver.
- Conforms to FCC part 15 requirements.
- Power management for supply current minimization.
- Low material cost.
- Two tuning points only.
- Provides 8/4/3 non-overlapping channels with AIC9001 SST chip.
- Compact size (45mm x 60mm x 10 mm)

RF MODULE BLOCK DIAGRAM

The IRF9XXXDS RF Module is a complete combination of transmitter and receiver . The functional block diagram is shown in Figure 3.

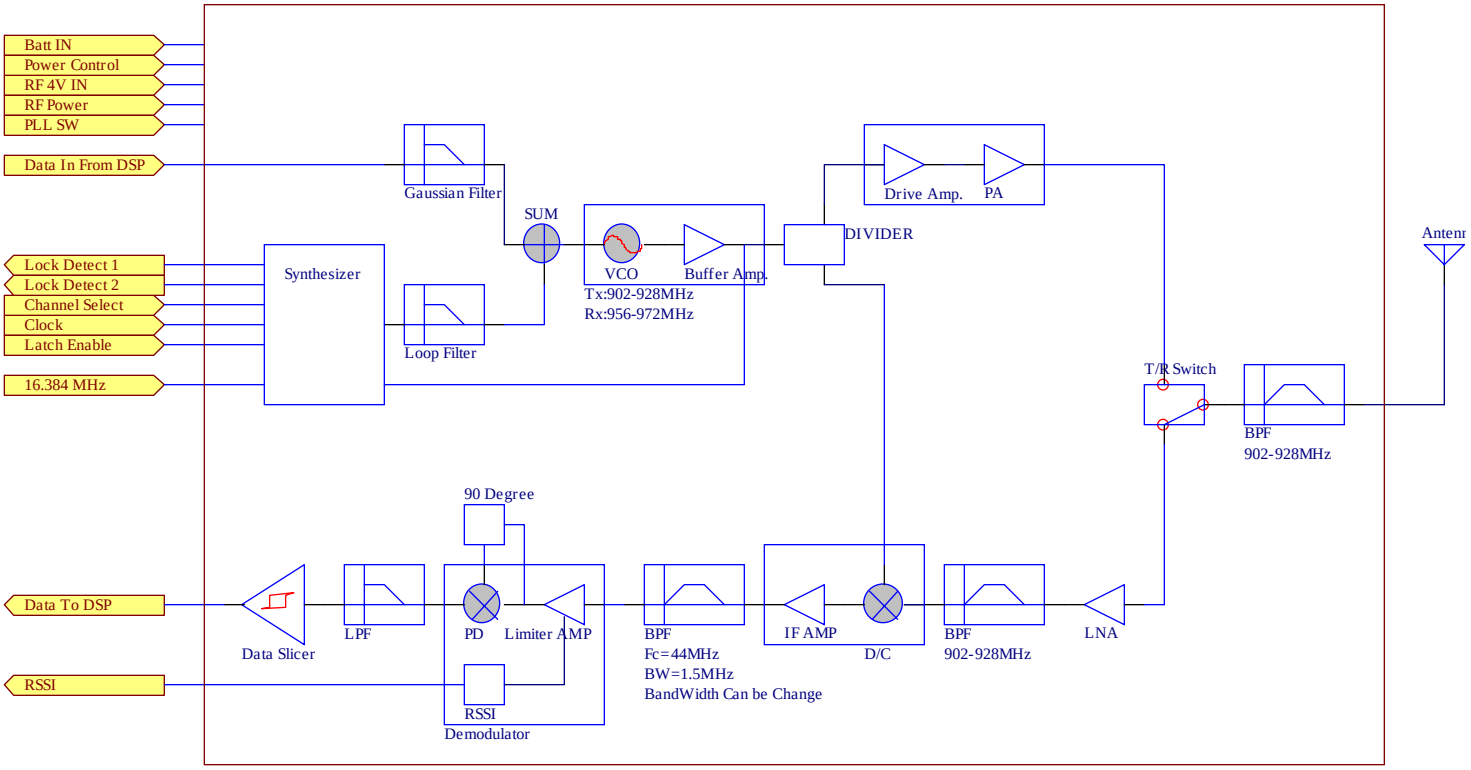


Figure3:Block Diagram of RF Module

A) TRANSMITTER

The module employs a T/R switch to switch between transmit and receive in the time domain. The MODOUT spread baseband digital data signal is filtered and up-converted to RF by the GMSK modulator. Due to the following properties: constant envelope, compact spectrum, fast roll-off of higher-order sideband, and easy detection, GMSK is used herein. High or low PA output power levels are selectable via the PWR CTL control pin. Then the PA output routes through the transmit/receive (T/R) switch and a ceramic band pass filter is used to remove out-band harmonics before exiting the module at the antenna port.

B) RECEIVER

From the antenna port, the RF signal passes through the ceramic bandpass and the T/R switch to remove the signals outside the 902-928 MHz band before entering the low noise amplifier (LNA). It then is down-converted to IF signals and filtered by a very high selective SAW filter to reject the out-band spurious and interference. Before going to the Discriminator Demodulator, the IF signals is processed by a limiting amplifier with a gain over 70 dB to improve the noise performance. It finally passes through the LPF and Comparator to get the raw data information. The Receiving Signal Strength Indicator (RSSI) coming out of the limiter can be used as a power control reference for the baseband microprocessor (uP).

C) VCO's & SYNTHESIZER

A single frequency synthesizer is used together with Single voltage controlled oscillator (VCO's) to form synthesized phase locked loop (PLL's) for transmission and receiving channel selection. Channel selection is done by programming a control register in the MB15E03SL serial interface by a microcontroller. The PLL specification and related information is described in a later section. Detailed specifications for the MB15E03SL can be found in data books from Fujitsu.

SPECIFICATIONS OF RF MODULE

- Frequency Band : 902 to 928 MHz
- Air Data Rate: 96K/192K/250K
- Channel Spacing : 2.304MHz/4.608MHz/6MHz
- Non-overlapping channels: 8/4/3 (with the AIC9001 SST chip)
- Frequency Stability +/- 50 ppm (depends on input reference)
- Phase Noise : -90 dBc/Hz @ 100 KHz (depends on input reference)
- PLL Lock Up Time : < 300 us
- Transmission Data Rate : 1.536Mbps/3.072Mbps/4Mbps
- Power Output : 20+/-2 dBm/high power (with BATT IN >= 4.8V)
- Modulation : GMSK
- Dynamic Range : -30 to -90 dBm @ BER < 10 e-3 (typically)
- Emission : FCC part 15 compliance
- Current Consumption : 150 mA /TX (Typical)
  70 mA /RX (Typical)
- T/R Access : TDD
- T/R Time Frame/ Time Slot : 9.0 ms/ 4.5 ms

MECHANICAL & ENVIRONMENTAL

- Module Dimensions : 45 mm x 60 mm x 10 mm (including shield case)
- Operating Temperature : 0°C to + 50°C
- Storage Temperature : -30°C to + 70°C

RECOMMENDED ANTENNA SPECIFICATION

- Frequency Range : 890 to 940 MHz
- Frequency Center : 915 MHz
- Gain : 2 dBi
- VSWR : 2:1

RF-BASEBAND INTERFACE DESCRIPTIONS & ASSIGNMENTS

The RF Module interface defined herein is the interface to the baseband portion and it is a 16-pin male connector (refer to appendix A). The pin-assignment and description of RF-to-BASEBAND interface is explained as follows and the pin-allocation diagram is depicted in appendix C :

Pin#	Pin Name	Type	Description
1	**BATT IN**	**Input**	DC power supply input (min 4.4 V) to provide the DC power of the power amplifiers. current consumption : 100 mA @ 5 V (Typical)
2	**18.432 MHz/ 9.216MHz/ 12MHz**	**Input**	Input as the reference source of the synthesizer. frequency stability: +/- 50 ppm phase noise : < -110 dBc @ +/- 5 KHz spurious : < -70 dBc @ +/- 500 KHz BW < -45 dBc @ +/- 10 MHz BW
3	**GND**		Grounding.
4 *	**CH SEL**	**Input**	Serial data input to the divider in the synthesizer to set the operation channel. CMOS Level.
5 *	**CLOCK**	**Input**	Clock input to synthesizer. CMOS Level.
6 *	**LE**	**Input**	Load Enable**,** rising edge trigger. When LE is HIGH or OPEN, data stored in the shift register is loaded to the appropriate latch. CMOS Level.
7	**DATA to DSP (DI)**	**Output**	Demodulated data output to DSP (SST chip). CMOS Level.
8 **	**RF PWR**	**Input**	Transmitter on (HIGH) and off (LOW) control. CMOS Level.
9	**ZC**	**Input**	Open Loop(PLL)
10	**DATA from DSP (MODOUT)**	**Input**	Data input from DSP(SST chip). As it affects the RF Module transmitter modulation index, the HIGH Level output of it needs to be fixed at 4 +/- 0.2 V. HIGH input : 4 +/- 0.2 V LOW input : 0 V

11			Not-used
12			Not-used.
13	**RSSI**	**Output**	Receiving signal strength indicator. (Voltage various range from 0.7 ~ 1.5 V)
14	****PLLSW**	**Input**	Transmitter VCO on (HIGH) and off (LOW) control. CMOS Level. Also used as Receiver on (LOW) and off (HIGH) control.
15	***LD**		Not-used.
16	**RF4V**	**Input**	Regulated 4 +/-0.2 Volts power supply input. (50 mA /TX and 70 mA /RX (Typical))

NOTE :1.***** denote synthesizer dependent.
2.****** denote RF Module TDD control signal from SST chip.
3. I/O pin type is reference to RF Module.

PIN #	Assignment	PIN #	Assignment
1	**BATT IN**	**9**	**ZC**
2	**18.432/9.216/12MHz**	**10**	**DATA from DSP**
3	**GND**	**11**	
4	**CH SEL**	**12**	
5	**CLOCK**	**13**	**RSSI**
6	**LE**	**14**	**PLL SW**
7	**DATA to DSP**	**15**	**LD**
8	**RF PWR**	**16**	**RF4V**

RF-ANTENNA INTERFACE DESCRIPTIONS & ASSIGNMENTS

The only other interface for the RF Module is the antenna port and it is a 2-pin male connector. The pin-assignment and descriptions of RF-to-ANTENNA interface is explained as follows and the pin-allocation diagram is depicted in appendix C :

Pin#	Pin Name	Type	Description
1	**GND**	**Output**	Grounding.
2	**RF OUT**	**Output**	900 MHz RF signal output and output impedance is 50 ohms.

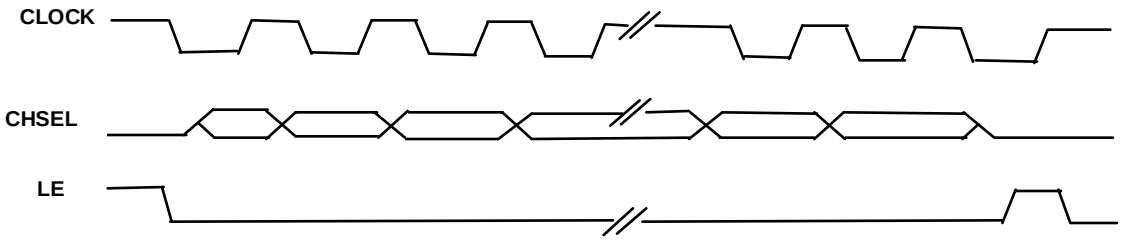
FREQUENCY SYNTHESIZED PLL SPECIFICATIONS , CONTROL REGISTER BIT ALLOCATION FOR MB15E03SL AND CHANNEL ASSIGNMENT

A) SYNTHESIZER SPECIFICATIONS

Operation Frequency	TX: 902 to 928 MHz RX: 950 to 970MHz
Channel Spacing	2.304 MHz 4.608MHz/ 6.0MHz
Channel Scanning Speed	< 300 us
Frequency Stability	+/-50 ppm
Phase Noise	-90 dBC/Hz @ 100 KHz
Reference Frequency	18.432MHz/ 9.216MHz/ 12MHz
Reference Input Power	-10 to +6 dBm

B) REGISTER CONTROL (uses CH SEL, CLOCK, LE)

a) The control signal timing of MB15E03SL(see Fujitsu data sheet for detail)



b) Set Parameter

Table for IRF9096DS

Reference Frequency	18.432E+06
Loop Reference Frequency	256.000E+0
Referenc Divider Ratio	72

MSB LSB

CS	LDS	FC	SW		CNT	HEX
0	0	1	1	00000001001000	1	8091

TX VCO Divider Ratio

					MSB			LSB
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	906.24MHz	3540	55	20	0000110111	0010100	0	03728
CH1	908.544MHz	3549	55	29	0000110111	0011101	0	0373A
CH2	910.848MHz	3558	55	38	0000110111	0100110	0	0374C
CH3	913.152MHz	3567	55	47	0000110111	0101111	0	0375E
CH4	917.76MHz	3585	56	1	0000111000	0000001	0	03802
CH5	920.064MHz	3594	56	10	0000111000	0001010	0	03814
CH6	922.624MHz	3604	56	20	0000111000	0010100	0	03828
CH7	94.976MHz	3613	56	29	0000111000	0011101	0	0383A

RX VCO Divider Ratio

					MSB			LSB
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	950.272E+06	3712	58	0	0000111010	0000000	0	03A00
CH1	952.576E+06	3721	58	9	0000111010	0001001	0	03A12
CH2	954.880E+06	3730	58	18	0000111010	0010010	0	03A24
CH3	957.184E+06	3739	58	27	0000111010	0011011	0	03A36
CH4	961.792E+06	3757	58	45	0000111010	0101101	0	03A5A
CH5	964.096E+06	3766	58	54	0000111010	0110110	0	03A6C
CH6	966.656E+06	3776	59	0	0000111011	0000000	0	03B00
CH7	968.960E+06	3785	59	9	0000111011	0001001	0	03B12

NOTE : Relatively detailed document and control signals timing for MB15E03SL, please refer to MB15E03SL data sheets from Fujitsu.

b) Set Parameter

Table for IRF9192DS

Reference Frequency 9.216E+06

Loop Reference Frequency 256.000E+0

Referenc Divider Ratio 36

MSB						LSB
CS	LDS	FC	SW		CNT	HEX

0 0 1 1 00000000100100 1 8049

TX VCO Divider Ratio

					MSB			LSB
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	906.240E+06	3540	55	20	0000110111	0010100	0	03728
CH1	910.848E+06	3558	55	38	0000110111	0100110	0	0374C
CH2	917.504E+06	3584	56	0	0000111000	0000000	0	03800
CH3	922.624E+06	3604	56	20	0000111000	0010100	0	03828

RX VCO Divider Ratio

					MSB			LSB
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	950.272E+06	3712	58	0	0000111010	0000000	0	03A00
CH1	954.880E+06	3730	58	18	0000111010	0010010	0	03A24
CH2	961.536E+06	3756	58	44	0000111010	0101100	0	03A58
CH3	966.656E+06	3776	59	0	0000111011	0000000	0	03B00

NOTE： Relatively detailed document and control signals timing for MB15E03SL, please refer to MB15E03SL data sheets from Fujitsu.

b) Set Parameter

Table for IRF9250DS

Reference Frequency 12E+06

Loop Reference Frequency 250.000E+0

Referenc Divider Ratio 48

MSB LSB

CS LDS FC SW CNT HEX

0 0 1 1 00000000110000 1 8061

TX VCO Divider Ratio

					MSB		LSB	
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	907.000E+06	3628	56	44	0000111000	0101100	0	03858
CH1	913.000E+06	3652	57	4	0000111001	0000100	0	03908
CH2	919.000E+06	3676	57	28	0000111001	0011100	0	03938

RX VCO Divider Ratio

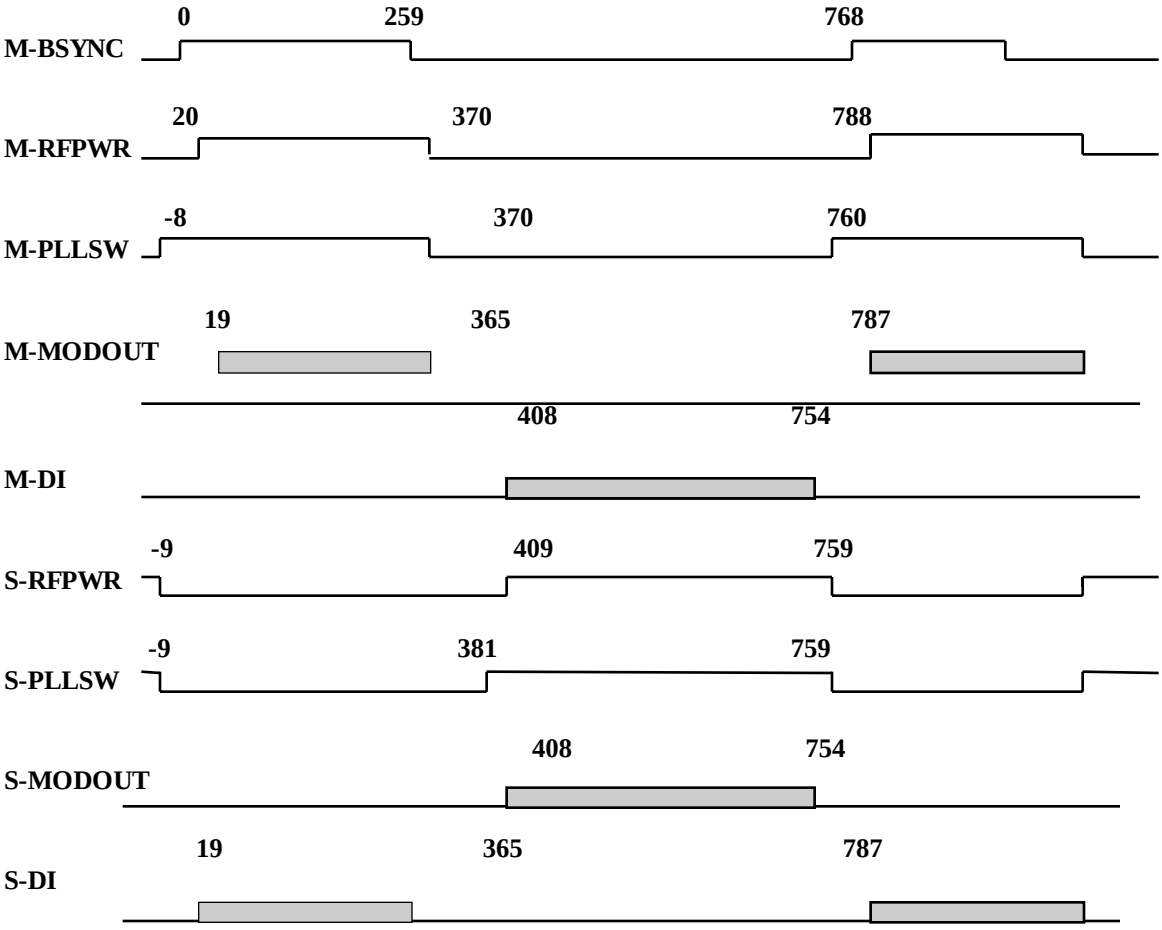
					MSB		LSB	
Channel	Frequency	Divider Ratio	N	A	N11 to N1	A7 toA1	CNT	HEX
CH0	952.000E+06	3808	59	32	0000111011	0100000	0	03B40
CH1	958.000E+06	3832	59	56	0000111011	0111000	0	03B70
CH2	964.000E+06	3856	60	16	0000111100	0010000	0	03C20

NOTE : Relatively detailed document and control signals timing for MB15E03SL, please refer to MB15E03SL data sheets from Fujitsu

RF MODULE & SST CHIP INTERFACE TIMING CHART

The RF Module interfaces with the ASIC SST chip through the following pins: DI, MODOUT, PLLSW, and RFPWR. PLLSW and RFPWR are used to switch the PLL and VCO of the transceiver and to power on/off the transmitter power amplifiers. The timing diagram for the PLLSW and RFPWR are shown in Figure 4 when it is used with AIC9001 SST chip for operation in two-way (full-duplex) communication mode, and the timing is assumed that there is no air propagation delay between master and slave. However, when operated in half-duplex

communication mode, the PLLSW and RFPWR are always ON (High) when the Module is set as Master (Transmitter) and OFF (Low) when it is set as Slave mode.



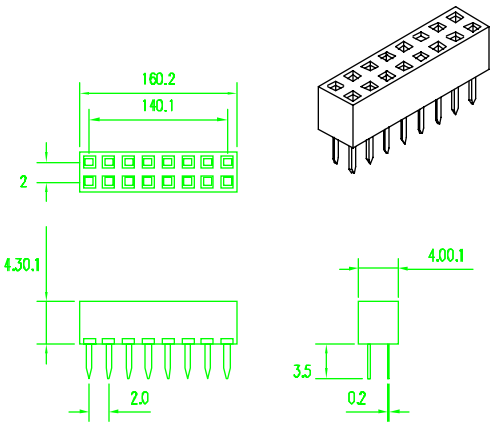
NOTE: 1. The timing is expressed as numbers of bits.
2. The total number of bits per burst is fixed and equal for both the master and slave.
3. The total Time Frame is 768 bits long.
4. 1-bit duration = 11.7 us.
5. Refer to AIC9001 data sheet for detail Frame timing information.

Figure 4. The timing diagram of the PLLSW and RFPWR.

MECHENICAL DRAWING AND INTERFACE PIN-LOCATION

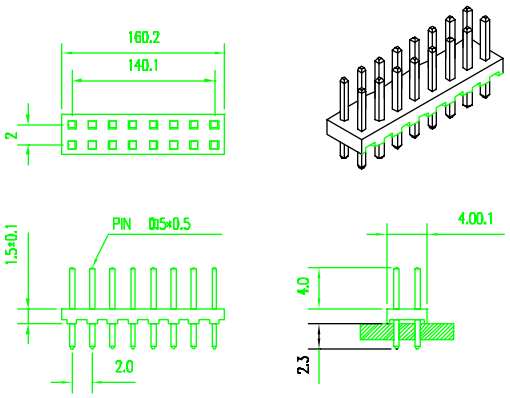
Appendix C show the drawing and interface pin-location.

APPENDIX A



SPECIFICATIONS
Current Rating: 1 Amps
Insulator resistance: 1000M OHM MIN at 500V DC
Dielectric withstanding voltage: 500V AC for one minute
Operating Temperature: -40°—+105Operating Temperature: -40°C
Contact resistance: 30 Milliohm max at 6V DC 0.3A
Insulator Material: PBT & Glass-Fiber reinforced, UL 94V-0
Contact Material: Copper alloy

APPENDIX B



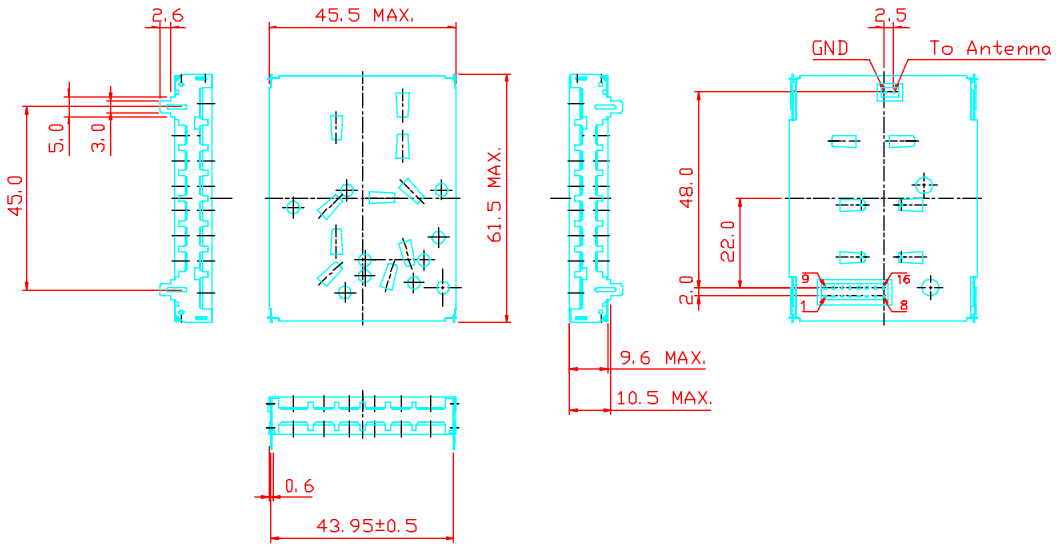
APPLICATION AND FEATURES

1. Side and end stackable (on unbroken edges)
2. Notches for easy breakable
3. Variable pin length gold or tin plated.
4. Standoffs facilitate post solder cleaning.
5. Mates with P C Board connectors e.g PLA parts No.PTF2-PTR2-

SPECIFICATIONS

Current Rating: 1 Amps
Insulator resistance 5000 Megohms min
Dielectric withstanding AC 500 V
Operating Temperature -40°-+105Operating Temperature -40°C
Contact Material: Brass or phosphor bronze
Insulator Material: Polyester. UL 94V-0

APPENDIX C


2.6
45.5 MAX.
2.5
GND
To Antenna
5.0
3.0
45.0
61.5 MAX.
48.0
22.0
2.0
9
16
1
8
9.6 MAX.
10.5 MAX.
0.6
43.95±0.5