Circuit Description

Model: KX-TC1467 LA (SERIES)

The following circuit description is based on the circuit diagram and block diagram of KX-TC1467 LA.

Handset:

1. Receiving Path

The receiving path is established by below sections.

Antenna and Duplexer

The quarter-wavelength Phosphorous-Nickel-plated rod antenna detects electro-magnetic signals at radio frequencies. These signals are further filtered into usable frequency for the receiving path through the Surface-Acoustic-Wave (SAW) duplexer.

Low Noise Amplifier (LNA)

RF signal is filtered by the SAW Duplexer DP1, and input to the Low Noise Amplifier Q3.

TB31262 RF COMBO IC

A single package IC which involves three systems about RF, IF, and AF. Receiving Path included Internal LNA, Double-balance Mixer, Phase Comparator, IF Amplifier, FM demodulator, Expander, and AF Amplifier.

INTERNAL LNA

The amplified RF signal from Q3 is fed to the second stage LNA which is internal to the TB31262 IC for further amplification.

DOUBLE-BALANCE Mixer

The amplified RF signal is streamed down to IF frequency by the Double-balanced Mixer. In this process, the RF signal is mixed with the Local Oscillator Frequency resulting to an IF of 10.7MHz.

IF Amplifier

The 10.7MHz IF is trimmed through a Ceramic Filter CF1. The composite IF is fed and further amplified by the IF Amplifier section of U1 (input pin 30). The amplified

IF is again trimmed through the 2nd Ceramic Filter CF2.

FM Demodulator and Expander

The 2nd composite IF is demodulated by the Quadrature tank coil IF1. The recovered audio is then fed to the Expander section of U1 for de-emphasis.

AF Amplifier

The de-emphasized signal is then trimmed and amplified through the AF Amp section of U1 (output pin 51) before being output to the Speaker.

2. Transmitting Path

The transmitting path is established by below sections.

Microphone Amplifier and Compressor

Audio Frequency picked up by the handset microphone is amplified by internal Mic Amplifier section of U1 through input pin 9. The amplified AF signal is then fed to the compressor section of U1 for pre-emphasis, after which the signal is fed to the Modulator circuit (Phase Comparator).

Modulator and TXVCO

The Transmitter Local Oscillator is composed by TX Loop Filters and internal circuitry of U1. Both AF and Data signals are fed to the Comparator circuit which will cause Frequency Modulation to progress.

RF power amplifier

The Frequency Modulated signal is amplified by the RF Amplifier internal to U1, which also acts as a frequency doubler, and is propagated through the Antenna via the Duplexer DP1.

3. Power Supply Circuitry

The supply voltages to various parts of the circuit are controlled by the following blocks:

Power-down Block

The RF combo IC monitors the battery voltage level. When the battery voltage becomes low to a pre-determined level, the combo IC sends a power_down signal to the MCU. The MCU then changes all port impedance to HI, and goes to stop mode. At

the same time, the RF combo IC goes to power down mode. This activity results to a very low total current consumption.

RX/TX VCC Block

Transistor Q2 acts as the RX-VCC control switch, while Q1 as the TX-VCC control switch. Both transistors work independently to supply the voltage to RF IC.

4. Ringer ON/OFF Switch

The ringer can be switch ON and OFF manually by a SPDT switch SW1.

Base Unit:

1. Receiving Path

The receiving path is established by below sections.

Antenna and Duplexer

The quarter-wavelength AWG18 antenna detects electro-magnetic signals at radio frequencies. These signals are further filtered into usable frequency for the receiving path through the Surface-Acoustic-Wave (SAW) duplexer.

Low Noise Amplifier (LNA)

RF signal is filtered by the SAW Duplexer DP1, and input to the Low Noise Amplifier Q3.

TB31262 RF COMBO IC

A single package IC which involves three systems about RF, IF, and AF. Receiving Path included Internal LNA, Double-balance Mixer, Phase Comparator, IF Amplifier, FM demodulator, Expander, and AF Amplifier.

INTERNAL LNA

The amplified RF signal from Q3 is fed to the second stage LNA which is internal to the TB31262 IC for further amplification.

DOUBLE-BALANCE Mixer

The amplified RF signal is streamed down to IF frequency by the Double-balanced

Mixer. In this process, the RF signal is mixed with the Local Oscillator Frequency resulting to an IF of 10.7MHz.

IF Amplifier

The 10.7MHz IF is trimmed through a Ceramic Filter CF1. The composite IF is fed and further amplified by the IF Amplifier section of U1 (input pin 30). The amplified IF is again trimmed through the 2nd Ceramic Filter CF2.

FM Demodulator and Expander

The 2nd composite IF is demodulated by the Quadrature tank coil IF1. The recovered audio is then fed to the Expander section of U1 for de-emphasis.

AF Amplifier

The de-emphasized signal is then trimmed and amplified through the AF Amp section of U1 (output pin 51) before being output to the Line Interface circuitry.

2. Transmitting Path

The transmitting path is established by below sections.

Microphone Amplifier and Compressor

Audio Frequency from the Line Interface circuitry is amplified by internal Mic Amplifier section of U1 through input pin 9. The amplified AF signal is then fed to the compressor section of U1 for pre-emphasis, after which the signal is fed to the Modulator circuit (Phase Comparator).

Modulator and TXVCO

The Transmitter Local Oscillator is composed by TX Loop Filters and internal circuitry of U1. Both AF and Data signals are fed to the Comparator circuit which will cause Frequency Modulation to progress.

RF power amplifier

The Frequency Modulated signal is amplified by the RF Amplifier internal to U1, which also acts as a frequency doubler, and is propagated through the Antenna via the Duplexer DP1.

3. Telephone Line Interface

The Telephone Line Interface is established by below sections.

Audio Power Amplifier

Q11 and Q13 are configured as AF Power Amplifier for a higher AF level output requirement of the Line Interface.

Line Isolation Transistors and Line Seizure Circuit

Q12 is utilized as Line Isolation Transistor. Both AF input and output are coupled to the Line Interface through this transistor. Q15 is for line seizing, which is controlled through MCU (U1) pin 24. This is also the circuit performing the Pulse Dialing process.

Ring Detect Circuit

IC2-A and IC2-B are configured as a differential amplifier to pick up the ring signal, which is coupled through two 20M ohm resistors (R44 and R45) to isolate the circuit from the Telephone Line.

Over-voltage / Over-current protector

Posistor F1 and Surge Protector VDR2 formed the over-voltage and over-current protector for the line interface.

Handset Frequency Table			
Channel	Tx Freq. (MHz)	Rx Freq. (MHz)	LO Freq. (MHz)
1	925.90	902.10	891.40
2	925.95	902.15	891.45
3	926.00	902.20	891.50
4	926.05	902.25	891.55
5	926.10	902.30	891.60
6	926.15	902.35	891.65
7	926.20	902.40	891.70
8	926.25	902.45	891.75
9	926.30	902.50	891.80
10	926.35	902.55	891.85
11	926.40	902.60	891.90
12	926.45	902.65	891.95
13	926.50	902.70	892.00
14	926.55	902.75	892.05
15	926.60	902.80	892.10
16	926.65	902.85	892.15
17	926.70	902.90	892.20
18	926.75	902.95	892.25
19	926.80	903.00	892.30
20	926.85	903.05	892.35
21	926.90	903.10	892.40
22	926.95	903.15	892.45
23	927.00	903.20	892.50
24	927.05	903.25	892.55
25	927.10	903.30	892.60
26	927.15	903.35	892.65
27	927.20	903.40	892.70
28	927.25	903.45	892.75
29	927.30	903.50	892.80
30	927.35	903.55	892.85
31	927.40	903.60	892.90
32	927.45	903.65	892.95
33	927.50	903.70	893.00
34	927.55	903.75	893.05
35	927.60	903.80	893.10
36	927.65	903.85	893.15
37	927.70	903.90	893.20
38	927.75	903.95	893.25
39	927.80	904.00	893.30
40	927.85	904.05	893.35

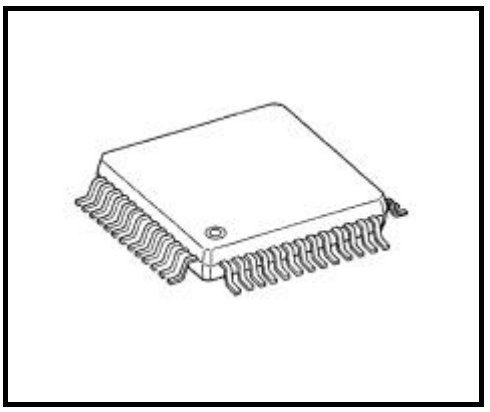
Base Unit Frequency Table			
Channel	Tx Freq. (MHz)	Rx Freq. (MHz)	LO Freq. (MHz)
1	902.10	925.90	936.60
2	902.15	925.95	936.65
3	902.20	926.00	936.70
4	902.25	926.05	936.75
5	902.30	926.10	936.80
6	902.35	926.15	936.85
7	902.40	926.20	936.90
8	902.45	926.25	936.95
9	902.50	926.30	937.00
10	902.55	926.35	937.05
11	902.60	926.40	937.10
12	902.65	926.45	937.15
13	902.70	926.50	937.20
14	902.75	926.55	937.25
15	902.80	926.60	937.30
16	902.85	926.65	937.35
17	902.90	926.70	937.40
18	902.95	926.75	937.45
19	903.00	926.80	937.50
20	903.05	926.85	937.55
21	903.10	926.90	937.60
22	903.15	926.95	937.65
23	903.20	927.00	937.70
24	903.25	927.05	937.75
25	903.30	927.10	937.80
26	903.35	927.15	937.85
27	903.40	927.20	937.90
28	903.45	927.25	937.95
29	903.50	927.30	938.00
30	903.55	927.35	938.05
31	903.60	927.40	938.10
32	903.65	927.45	938.15
33	903.70	927.50	938.20
34	903.75	927.55	938.25
35	903.80	927.60	938.30
36	903.85	927.65	938.35
37	903.90	927.70	938.40
38	903.95	927.75	938.45
39	904.00	927.80	938.50
40	904.05	927.85	938.55

TOSHIBA Bi- CMOS Integrated Circuit Silicon Monolithic

T B 3 1 2 6 2 F

RF 1chip IC for 900 MHz Cordless Telephone

One package involve three systems about RF, IF, and AF. Involving LNA, MIX, PA, VCO (TX,RX), PLL, IF-AMP, Detecter, Compander,and 4 useful audio amplifiers. It is possible to reduce many external parts. This IC is suitable for ISM 900 MHz cordless telephone.



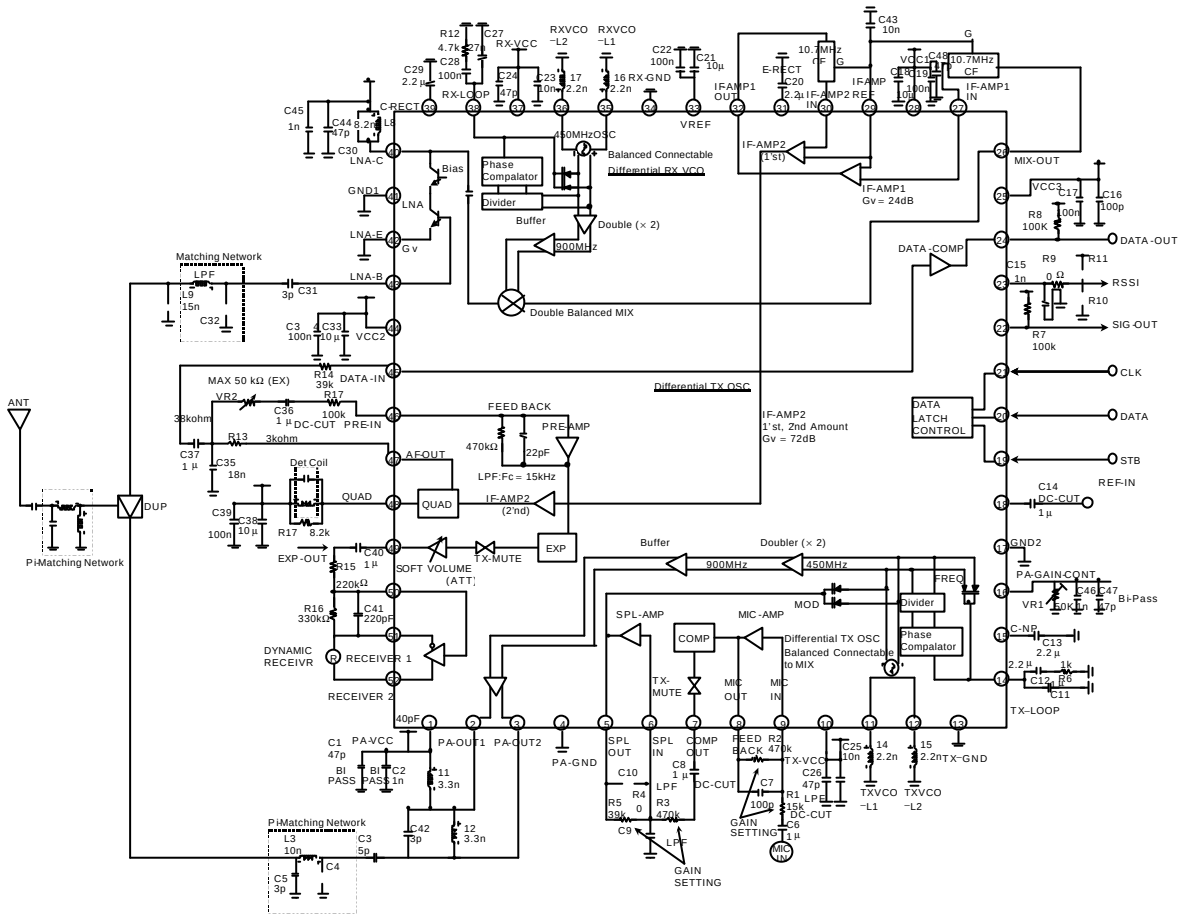
QFP52-P-1010-0.65

Features

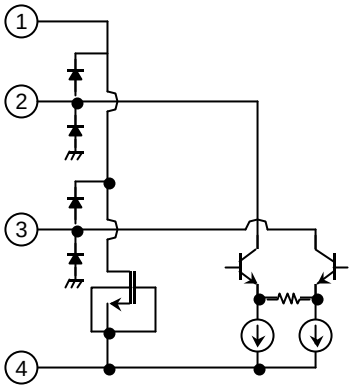
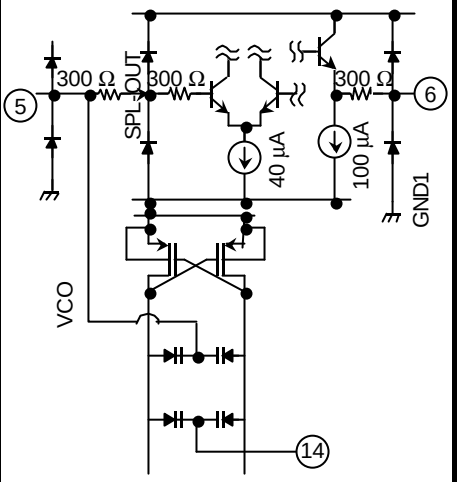
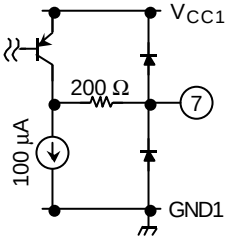
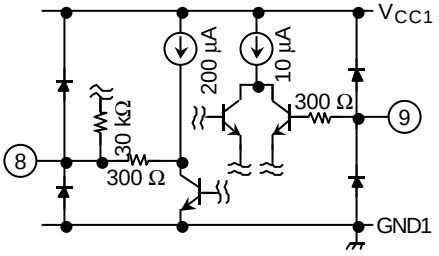
- Same system & software almost compatible as TB31261AF (Single Conversion, IF Frequency: 10.7 MHz,)
- Built-in LNA
- Built-in 1'st MIX
  → Double Balanced MIX (DBM) Type.
- Built-in Differential VCO, Variable capacitor (TX, RX) and Doubler (450 MHz × 2)
- Built-in PA
- A substitution from TB31261AF is easy
  (Same package, Software almost compatible)
- Low operating voltage: V_{CC} = 2.0~5.0 V
- Current operating current: I_{CC} = 70 mA (All On)
- PLL operating frequency :around 450 MHz
- Serial control for all status
- Built in pre-amp, receiver-amp, mic-amp, and spl-amp
- Receiver output Level adjustment.
- Variable battery alarm setting. (7 thresholds)
- Built in battery saving function for Intermittent receiving.
- Small package: QFP52pin (0.65 mm pitch)

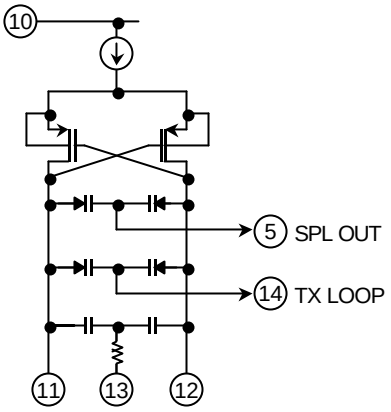
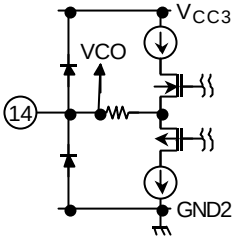
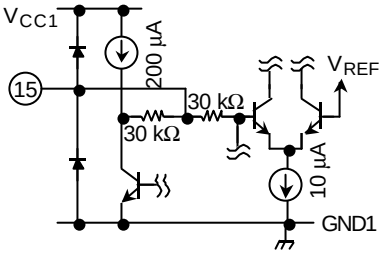
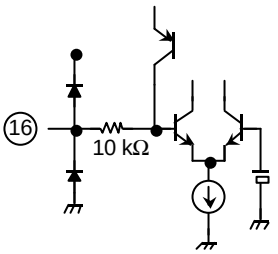
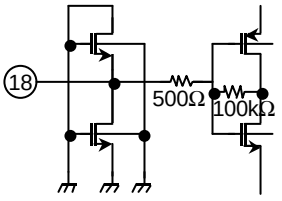
＊Handle with care to prevent devices from deterioration by static electricity.

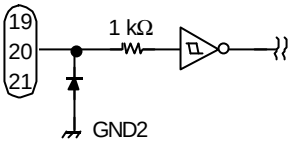
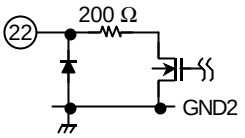
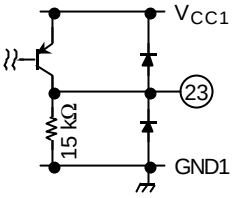
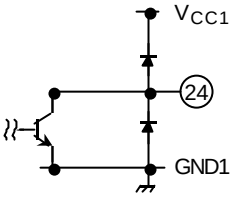
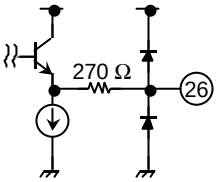
Block Diagram

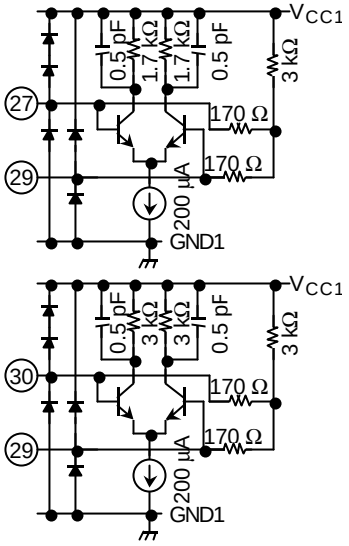
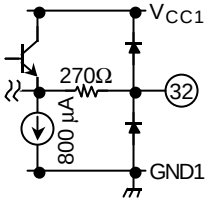
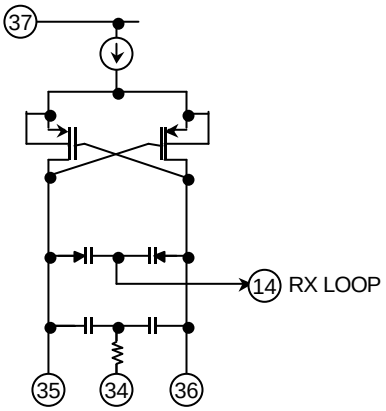
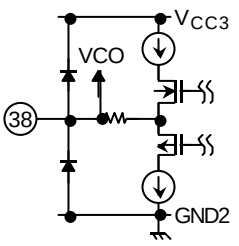


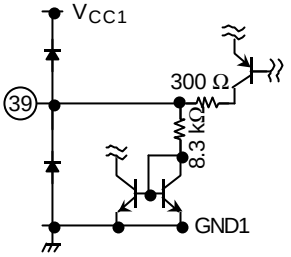
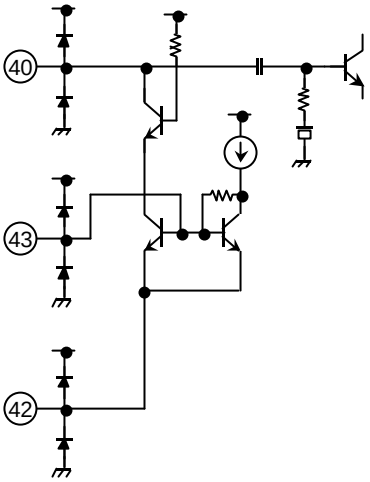
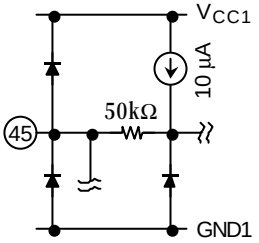
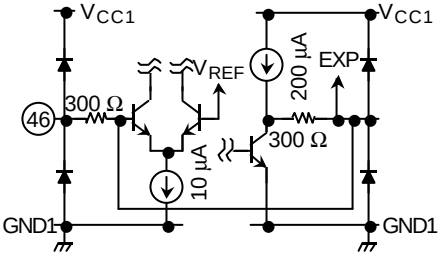
Pin Function (The values of internal components are typical)

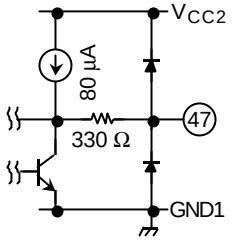
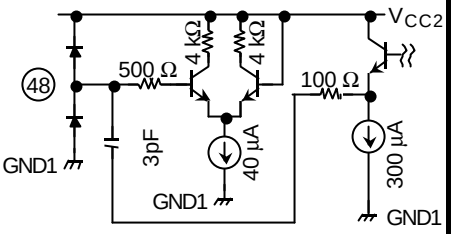
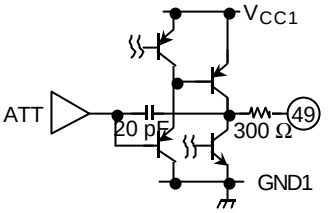
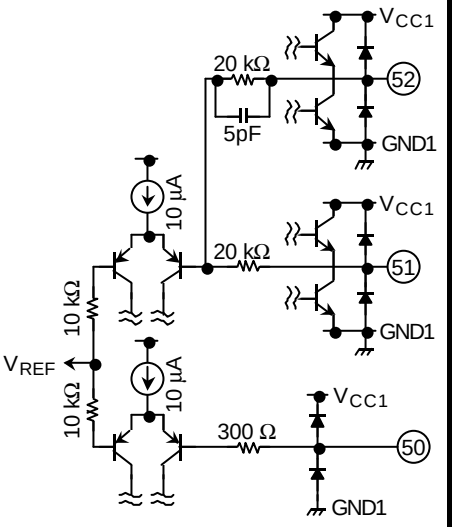
Pin No.	Pin Name	Function	Internal Equivalent Circuit
1	PA-V_{CC}	V_{CC} terminal	
2	PA-OUT1	Differential output terminal1 of Power Amp	
3	PA-OUT2	Differential output terminal2 of Power Amp	
4	PA-GND	GND terminal	
5	SPL-OUT	Output terminal of Splatter Amp	
6	SPL-IN	Input terminal of Splatter Amp	
7	COMP-OUT	Output terminal of Compressor	
8	MIC-OUT	Output terminal of MIC Amp	
9	MIC-IN	Input terminal of MIC Amp	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
10	TX-V_{CC}	V_{CC} terminal	
11	TXVCO-L1	Terminal1 for external inductor of differential TXVCO	
12	TXVCO-L2	Terminal2 for external inductor of differential TXVCO	
13	TX-GND	GND terminal	
14	TX-LOOP	Terminal1 for TX loop filter	
15	C-NF	Terminal for compressor's negative feedback capacitor	
16	PA-GAIN-CONT	PA gain control terminal for external variable resistance to GND	
17	GND2	GND terminal	—
18	REF-IN	Reference clock input terminal	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
19	STB	Strobe input terminal for serial data setting	
20	DATA	Data input terminal for serial data setting	
21	CLK	Clock input terminal for serial data setting	
22	SIG-OUT	Signal output terminal	
23	RSSI	RSSI linear output terminal	
24	DATA-OUT	Output terminal of Data comparater	
25	V_{CC3}	V_{CC} terminal	—
26	MIX-OUT	Output terminal from Mixer	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
27	IFAMP1IN	Input terminal for IF-AMP1	
28	V_{CC1}	V_{CC} terminal	
30	IFAMP2IN	Input terminal for IF-AMP2	
29	IF-AMP-REF	Reference terminal for IF-AMP1 and IF-AMP2	—
31	E-RECT	Expander's external rectifier capacitor terminal	—
32	IFAMP1OUT	Output terminal from Expander	
33	VREF	Reference voltage output terminal with external Bi-pass capacitor	—
34	RX-GND	GND terminal	
35	RX-VCOL1	Terminal1 for external inductor of differential RXVCO	
36	RX-VCOL2	Terminal2 for external inductor of differential RXVCO	
37	RX-V_{CC}	V_{CC} terminal	
38	RX-LOOP	Terminal1 for RX loop filter	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
39	C-RECT	Terminal for Compressor's rectifire capacitor	
40	LNA-C	Corrector terminal of LNA	
42	LNA-E	Emitter terminal of LNA	
43	LNA-B	Base terminal of LNA	
41	GND1	GND terminal	—
44	V_{CC2}	V_{CC} terminal	—
45	DATA-IN	Input terminal of data comparator	
46	PRE-IN	Input terminal of Pre Amp	

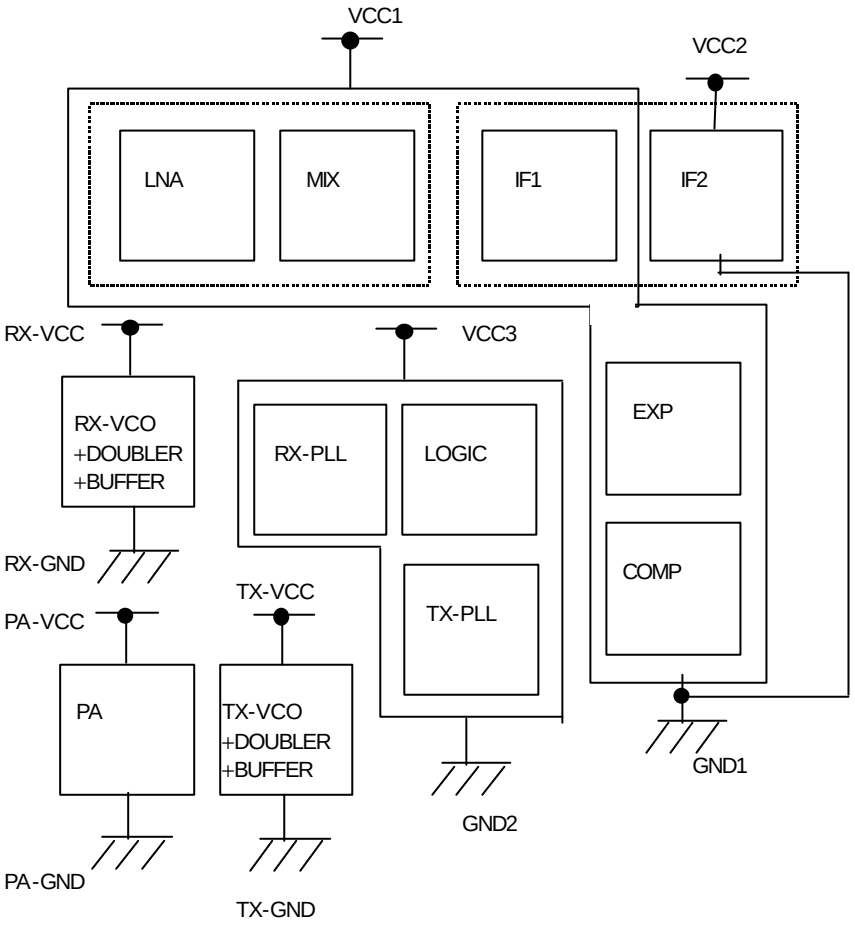
Pin No.	Pin Name	Function	Internal Equivalent Circuit
47	AF-OUT	Audio frequency output terminal of Quadrature detection	
48	QUAD	Terminal for external Quad-Coil for detection	
49	EXP-OUT	Output terminal of Expander	
50	REC-IN	Input terminal of Receiver Amp	
51	REC-OUT1	Differential output terminal1 of Receiver Amp	
52	REC-OUT2	Differential output terminal2 of Receiver Amp	

1. General Description

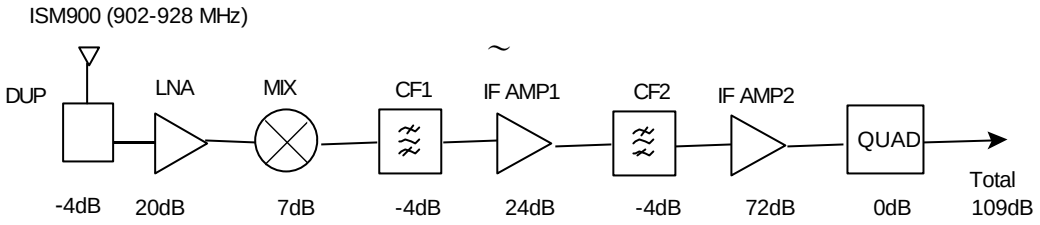
TB31262F is controlled all status by serial data. This IC is included IF detector, PLL, and compander. IF detector function is for wide-band system, dual PLL function, and compander with MIC amp and receiver amp.

+ • POWER SUPPLY BLOCK ASSIGN

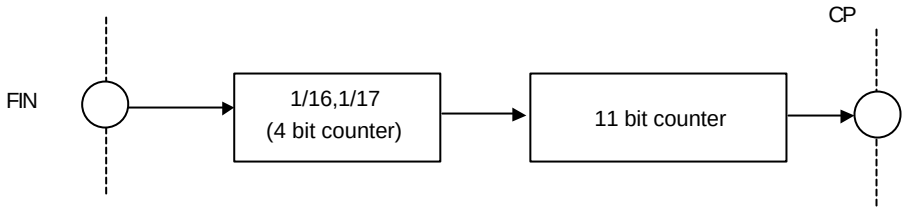
V_{CC1}	GND1	LNA, MIX, IF-AMP1, DATA-COMP, MIC-AMP, COMPRESSOR, RECEIVER-AMP PRE-AMP, EXPANDER, SPLATTER-AMP
V_{CC2}		IF-AMP2, QUAD
V_{CC3}	GND2	RX-PLL, TX-PLL, REF-INPUT, DATA LATCH CONTROL
RX-V_{CC}	RX-GND	RX-VCO + DOUBLER+BUFFER
TX-V_{CC}	TX-GND	TX-VCO + DOUBLER+BUFFER
PA-V_{CC}	PA-GND	POWER-AMP



Gv distribution for receiving



2. PLL block

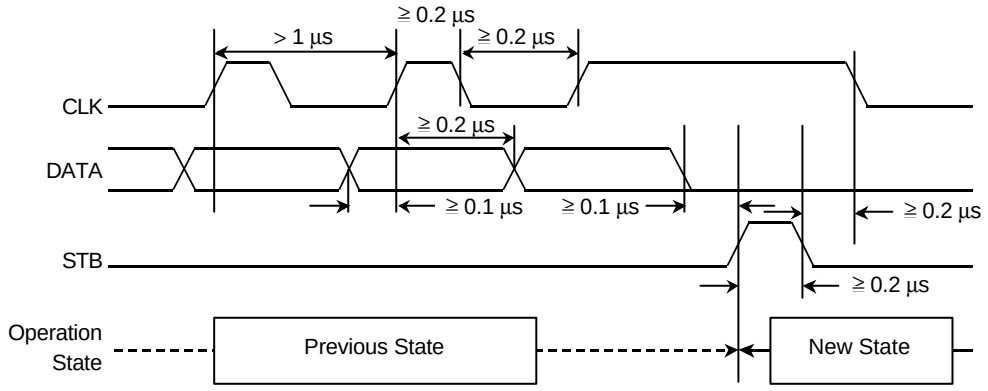


3. Data Latch Control

This block has 4 registers assigned by 2 or 3 bits CODE. DATA is read on the time of up edge of CLK. When STB receivers high signal, DATA in shift register is sent into LATCH to control block which CODE indicates and the operation starts.

INPUT TIMING FOR SERIAL DATA

When both CLK "H" and DATA "L", STB "H" leads data active.



Code			Control Block	Function
*	1	0	TX divider (18 bits)	Setting frequency for TX-PLL
*	0	1	RX divider (18 bits)	Setting frequency for RX-PLL
*	1	1	REF divider (12 bits)	Setting phase comparison frequency
0	0	0	Option control 1	Battery save, Mute control, etc
1	0	0	Option control 2	Volume control

4. Serial data format

(1) TX DIVIDER (Set VCO Doubler Output Frequency (EX 900 MHz, Not 450 MHz))

Swallow counter (4 bit)				Programmable counter (11 bit)												Code	
A0	A1	A2	A3	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	*	1	0

← 1st
*don't care
STB
$N = 2 \times (16M + A)$ (480 – 65534)
$A = A0 + 2A1 + 4A2 + 8A3$
$M = M0 + 2M1 + 4M2 + 8M3 + 16M4 + 32M5 + 64M6 + 128M7 + 256M8 + 512M9 + 1024M10$

(2) RX DIVIDER (Set VCO Doubler Output Frequency (EX 900 MHz,Not 450 MHz))

Swallow counter (4 bit)				Programmable counter (11 bit)												Code	
A0	A1	A2	A3	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	*	0	1

← 1st
*don't care
STB
$N = 2 \times (16M + A)$ (480 – 65534)
$A = A0 + 2A1 + 4A2 + 8A3$
$M = M0 + 2M1 + 4M2 + 8M3 + 16M4 + 32M5 + 64M6 + 128M7 + 256M8 + 512M9 + 1024M10$

(3) REF DIVIDER

Programmable counter (10bit)										Code	
R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	1	1

← 1st
STB
$N = R(4 – 1023)$
$R = R0 + 2R1 + 4R2 + 8R3 + 16R4 + 32R5 + 64R6 + 128R7 + 256R8 + 512R9$

(4) Option control 1

SIG OUT				TX control				RX control				BAT-ALM (Setting)			Code		
TXLD	RXLD	RSSI	BALM	RF	AF	CP	MUT	RF	AF	CP	MUTE	BA1	BA2	BA3	0	0	0

← 1st
STB

1) Battery saving (BS) control

0	Operation
1	Battery Saving (BS)

Bit	Control Block
RX-RF	RX-PLL,RX-Buffer Tr, IF AMP,QUAD,DATA COMP,RSSI, LNA, MIX, RX – VCO + DOUBLER → I_{CC} 2
RX-AF	PRE AMP,EXPANDER,RECEIVER AMP→ I_{CC} 3
TX-RF	TX-PLL,TX-Buffer Tr , PA ,TX-VCO + DOUBLER → I_{CC} 4
TX-AF	MIC AMP, COMPRESSOR, SPLATTER-FILTER → I_{CC} 5

REF INPUT = OFF at TX-RF = 1 and RX-RF = 1

2) Charge Pump Output Current Select

CP	Current
0	400 μA
1	800 μA

3) MUTE control

0	Operation
1	MUTE ON

TX-MUTE control for COMPRESSOR output.
RX-MUTE control for EXPANDER output.

4) Battery Alarm Detection Setting

This IC has 5 threshold levels for detection of battery dropping.
These threshold levels are given by below table.

BA1	BA2	BA3	DET. Voltage
1	0	1	2.15 V
0	0	0	2.25 V
0	0	1	3.00 V
0	1	0	3.15 V
0	1	1	3.30 V
1	0	0	2.85 V
1	1	0	2.75 V
1	1	1	BS

5) SIG OUT selection

SIG OUT terminal generates combination states of RX and TX LOCK DETECTOR and RSSI.

0	OFF
1	OUT PUT

BIT	FUNCTION
TXLD	TX-PLL LOCK DETECTOR
RXLD	RX-PLL LOCK DETECTOR
RSSI	RSSI COMPARATOR OUTPUT
BALM	BATTERY ALARM

(5) Option control 2

RECEIVER OUTPUT LEVEL CONTROL

It is possible to volume control to set these bits.

And this resister includes TEST bits which must be set 0 in customer side.

1.5dB steps from 0dB to –22.5dB.

Receiver Volume					Code		
VOL1	VOL2	VOL3	VOL4	TEST	1	0	0

VOL1	VOL2	VOL3	VOL4	GAIN
0	0	0	0	0dB
0	0	0	1	–1.5dB
0	0	1	0	–3.0dB
0	0	1	1	–4.5dB
0	1	0	0	–6.0dB
0	1	0	1	–7.5dB
0	1	1	0	–9.0dB
0	1	1	1	–10.5dB
1	0	0	0	–12.0dB
1	0	0	1	–13.5dB
1	0	1	0	–15.0dB
1	0	1	1	–16.5dB
1	1	0	0	–18.0dB
1	1	0	1	–19.5dB
1	1	1	0	–21.0dB
1	1	1	1	–22.5dB

MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	VCC	6	V
Power Dissipation	PD	*1) 900	mW
Operating Temperature	T opr	-20~70	°C
Storage Temperature	T stg	-50~150	°C

*1) IC single unit

TENTATIVE ELECTRICAL CHARACTERISTICS

(1) System Characteristics

– TOTAL

(V_{CC} = 3.6 V, Ta = 25°C, Δf = ±25 kHz, fmod = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating Power Supply Voltage	V_{CC} (opr)	—	—	2.0	3.6	5.0	V
Consumption Current 1	ICC1	1	ALL ON, PA-GAIN CONT = 20 kΩ	56.0	70.0	84.0	mA
Consumption Current 2	ICC2	1	RX-RF ON	18.0	26.0	34.0	mA
Consumption Current 3	ICC3	1	RX-AF ON	2.0	2.9	3.8	mA
Consumption Current 4	ICC4	1	TX-RF ON, PA-GAIN CONT = 20 kΩ	32.0	40.0	48.0	mA
Consumption Current 5	ICC5	1	TX-AFON	1.1	1.7	2.3	mA
Alarm Supply Current	ICC (A)	1	RL = 100kΩ、3.3Vmode	80	115	180	μA
Supply Current at BS	ICC (BS)	1	ALL OFF	—	0	5	μA
Data Input Threshold1	V IH	—	—	0.8 × V_{CC}	V_{CC}	4.0	V
	V IL	—	—	–0.2	0	0.2 × V_{CC}	V
Data Input Current	I IH	1	V IH = V_{CC}	—	0	1	μA
	I IL	1	V IL = GND	—	0	1	μA
CK Input Frequency	f CK	1	—	—	100	4000	KHz

– DETECTORS

(Unless Otherwise Specified, V_{CC} = 3.6 V, Ta = 25°C)

DETECTOR-1: BATTERY ALARM

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Detection Voltage0	VBAT0-L	1	—	2.07	2.15	2.23	V
	VBAT0-H		—	—	2.22	2.30	V
Detection Voltage1	VBAT1-L	1	—	2.17	2.25	2.33	V
	VBAT1-H		—	—	2.32	2.40	V
Detection Voltage2	VBAT2-L	1	—	2.67	2.75	2.83	V
	VBAT2-H		—	—	2.83	2.91	V
Detection Voltage3	VBAT3-L	1	—	2.77	2.85	2.93	V
	VBAT3-H		—	—	2.93	3.01	V
Detection Voltage4	VBAT4-L	1	—	2.92	3.00	3.08	V
	VBAT4-H		—	—	3.08	3.16	V
Detection Voltage5	VBAT5-L	1	—	3.05	3.15	3.25	V
	VBAT5-H		—	—	3.25	3.35	V
Detection Voltage6	VBAT6-L	1	—	3.20	3.30	3.40	V
	VBAT6-H		—	—	3.40	3.50	V

DETECTOR-2: DATA COMPARATOR

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Duty Ratio1	Duty1	2	VIN (Data Comparator Input) = 40mVrms, "H"Level, F = 500 kHz	42	46	50	%
Duty Ratio2	Duty2	2	VIN (Data Comparator Input) = 120mVrms, "H"Level, F = 500 kHz	43	48.5	50	%
Output Low Level Voltage	V OL2	1	I SINK = 0.2 mA	—	0.1	0.5	V
Output Leak Current	I LEAK2	1	H LEVEL	—	0	5	μA

DETECTOR-3: SIG OUT

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output Low Level Voltage	VOL3	1	I SINK = 0.2 mA	—	0.1	0.5	V
Output Leak Current	I LEAK3	1	H Level	—	0	5	μA

– PLL (Doubler Type Differential VCO System with Vari-Cap)

(Unless Otherwise Specified, V_{CC} = 3.6 V, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
PLL Operating Frequency	f IN	—	—	—	450	—	MHz
XIN Operating Frequency	fXI	1	VIN = 280mVp-p	2	4	10	MHz
XIN Input Sensitivity	VXIH	1	fIN = 4 MHz	200	280	—	mVp-p
Charge Pump Output Current	ICP1	—	VCP = 1.8 V	—	±400	—	uA
	ICP2	—	VCP = 1.8 V	—	±800	—	uA
Charge Pump Leak Current	I LEAK	1	—	—	0	5	uA

(2) RX CHARACTERISTICS

– RF

(V_{CC} = 3.6 V, Ta= 25°C, Δf = ±25 kHz, fmod = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
12dB SINAD Sensitivity	12dB SINAD	—	LNA MATCHING INPUT	—	2.5	—	dBu V_{EMF}
LNA＋MIX Gain	Gv	—		—	27	—	
IF AMP1 Gain	GIF1	—	—	—	24	—	dB
IF AMP2 Gain	GIF2	—	—	—	72	—	dB
Demodulated Output level	V OD	2	VIN (RF (DUP)) = 50dBμV_{EMF}	88	108	128	mVrms
Demodulated Output level2	ΔV OD	2	VIN (RF (DUP)) = 15dBμV_{EMF} ΔVOD≧VOD-3dB	–3.0	0	—	dB
S/N Ratio	SN	2	VIN (RF (DUP)) = 50dBμV_{EMF} with300～3kHz filter	40	47.5	—	dB
AM Rejection Ratio	AMR	—	VIN (RF (DUP)) = 50dBμV_{EMF}	—	40	—	dB
IFAMP1 input Resistance	RIF1IN	—	IF1-IN	—	330	—	Ω
IFAMP1 Output Resistance	RIF1OUT	—	IF1-OUT	—	330	—	Ω
IFAMP2 Input Resistance	RIFOUT	—	IF2-IN	—	330	—	Ω
RSSI Output Voltage	VRSSI1	2	VIN (RF (DUP)) = 15dBμV_{EMF}	0.33	0.63	0.93	V
	VRSSI2		VIN (RF (DUP)) = 50dBμV_{EMF}	1.17	1.47	1.77	V
RX VCO Control voltage	Vcont RX	2	f =936.7MHz	0.7	1.0	1.3	V

– AF

PRE AMP + EXPANDER + RECEIVER AMP

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
EXP Output Reference Level	VrefE	2	VIP = –20dBV PRE-AMP INPUT RESISTANCE: 150kΩ	–14.0	–10.0	–6.0	dBV
EXP Output Deviation	VOE	2	VOP = –45dBV	–1.0	0.0	+1.0	dB
Total Hormonic Distortion	THD R	2	RL = 150 Ω VRI = –15dBV	—	1.15	2.0	%
Output Noise Level	VNOR	2	Input -GND Short	—	–90	–65	dBV
Maximum Output Level	DR	—	THD = 3%, 150 Ωload	—	2.2	—	Vp-p
MUTE Output Level	VMUTE	—	—	—	–70	—	dBV
PRE AMP Voltage Gain Setting Range	GRNG2	—	—	0	—	20	dB
RECEIVER AMP Voltage Gain Setting Range	GRNG1	—	—	6	—	20	dB
Offset Voltage	TOF2	1	RO1・RO2	–50	0	50	mV
Crosstalk CE	CTCE	—	VIM = –10dBV	—	–65	—	dB
Attack Time	T_{AE}	—	VIP = –18 → –12dBV	—	8.5	—	ms
Recovery Time	T_{RE}	—	VIP = –12 → –18dBV	—	4.5	—	ms

(3) TX CHARACTERISTICS

– RF

(V_{CC} = 3.6 V, Ta= 25°C, Δf = ±25 kHz, fmod = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
PA OUTPUT LEVEL	PA-OUT	2	AFTER MATCHING NETWORK VR = 20 kΩ	0	+3.0	+6.0	dBm
PA GAIN CONTROL	PA-CONT	2	VR = 100 kΩ, PA-OUT Deviation	-9.0	–6.5	-4.0	dB
PA OUTPUT IMPEDANCE	PA-R-OUT	—	AFTER MATCHING NETWORK	—	50	—	Ω
PA OUTPUT CAPACITANCE	PA-C-OUT	—	AFTER MATCHING NETWORK	—	30	—	pF
TX VCO Control voltage	Vcont TX	2	f =904MHz	0.4	0.7	1.0	V
TX VCO Deviation	Δf TX	2	FILOUT=-30dBV, f =904MHz	±25	±30	±35	KHz
TX VCO Distortion	THD TX	2	FILOUT=-30dBV, f =904MHz	—	1.0	3.0	%

– AF

(Unless Otherwise Specified, V_{CC} = 3.6 V, fin = 1 kHz, Ta = 25°C)

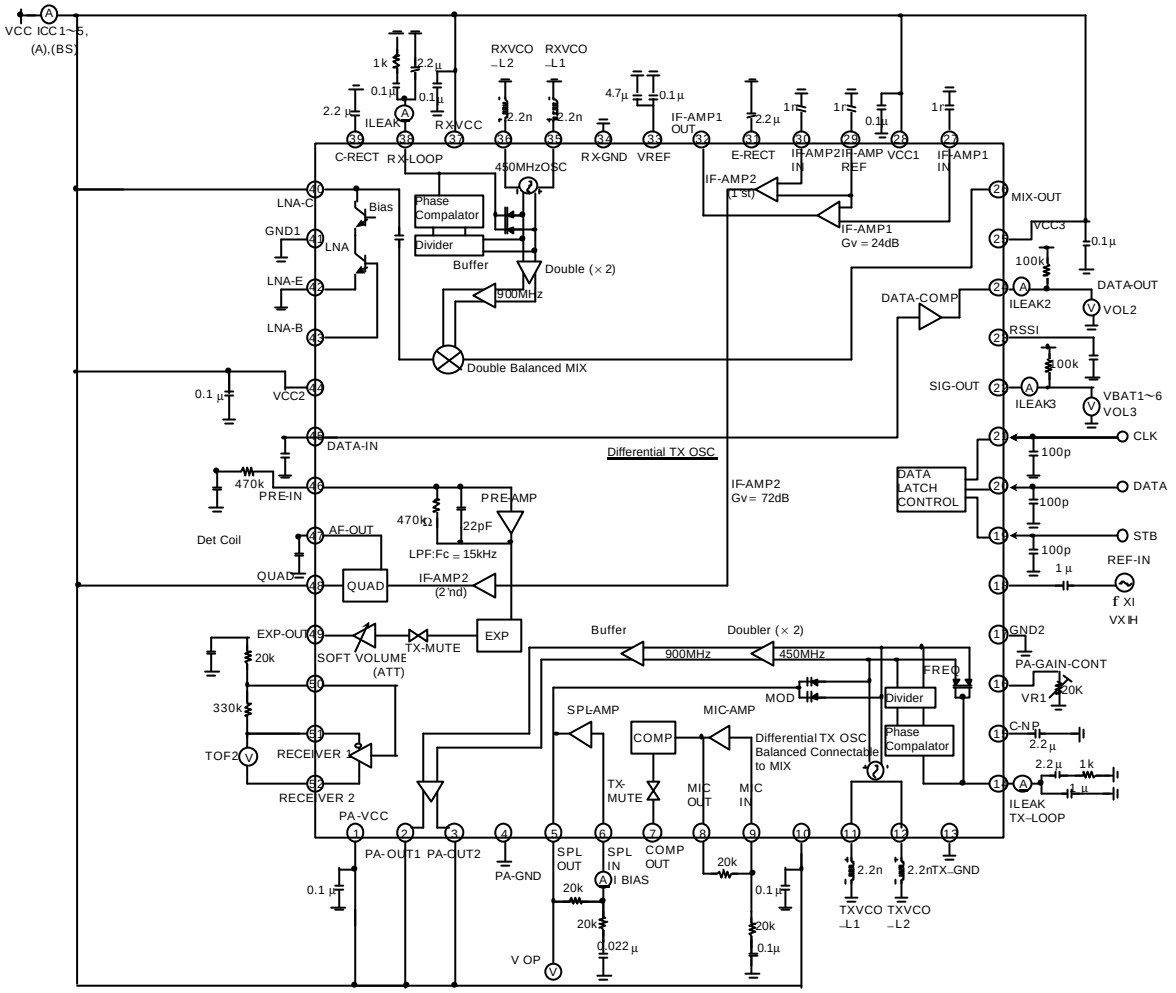
MIC AMP + COMPRESSOR

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
COMP Output Reference Level	VrefC	2	VOM = –10dBV	–11.5	–10.0	–8.5	DBV
COMP Output Deviation	VOC	2	VOM = –30dBV	–0.7	0.0	+0.7	DB
MIC AMP Voltage Gain Setting range	VGR	—		0	—	30	DB
Total Hormonic Distortion	THD C	2	VOM = –10dBV	—	0.15	1.0	%
Output Noise Level	V NOC	2	Input-GND Short	—	–61	–48	dBV
Limitting Level	V lim1	—	COMP OUT, VIM = 0dBV	—	1.3	—	Vp-p
	V lim2		MIC OUT, VIM = 0dBV	—	2.5	—	Vp-p
MUTE Output Level	V MUTE	—	—	–80	–90	—	dBV
Crosstalk EC	CTEC	—	VIP = –10dBV	—	–50.0	—	dB
Attack Time	T_{AC}	—	VIM = –46 → –34dBV	—	3.5	—	ms
Recovery Time	T_{RC}	—	VIM = –34 → –46dBV	—	5.0	—	ms

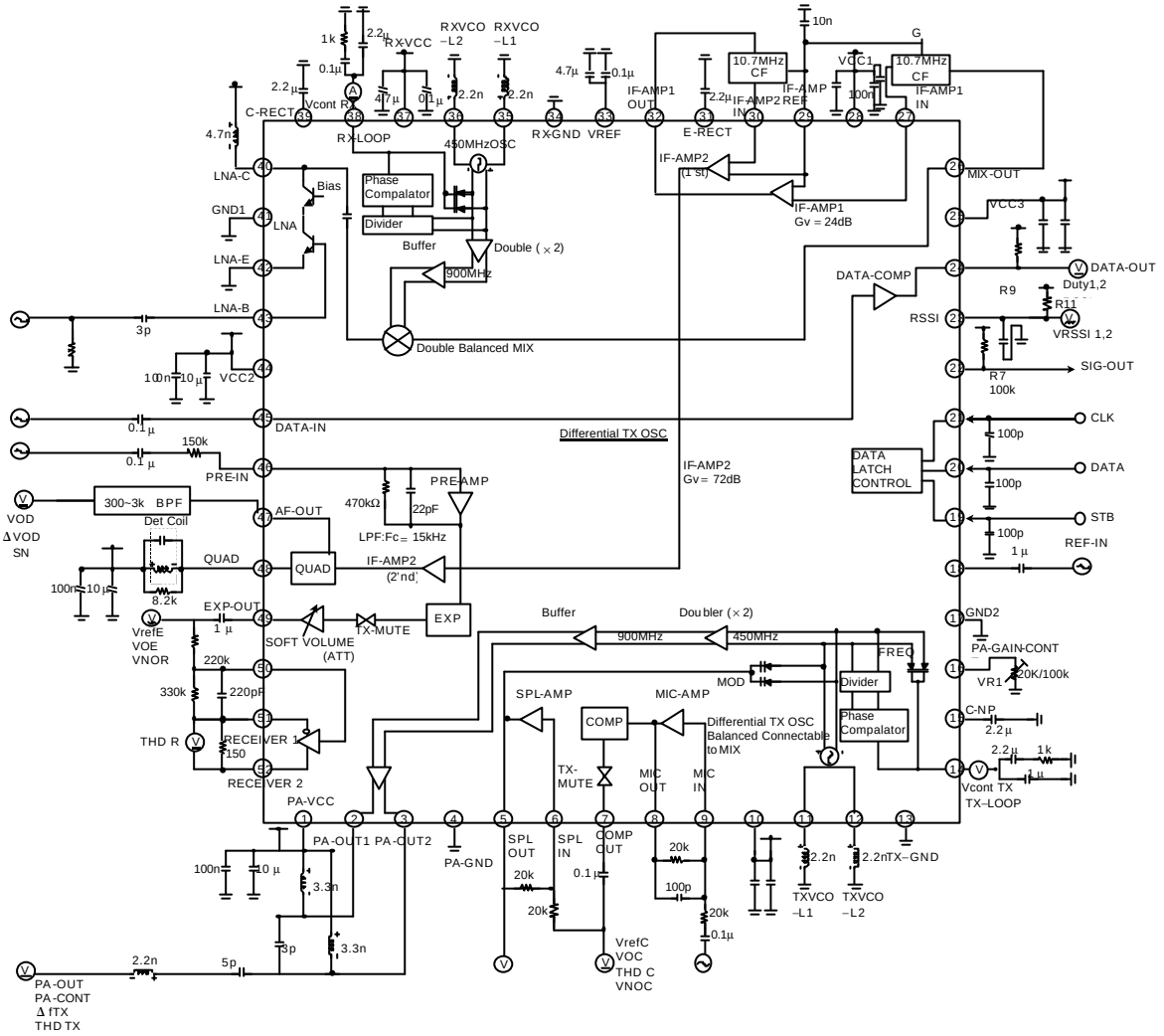
FILTER AMP

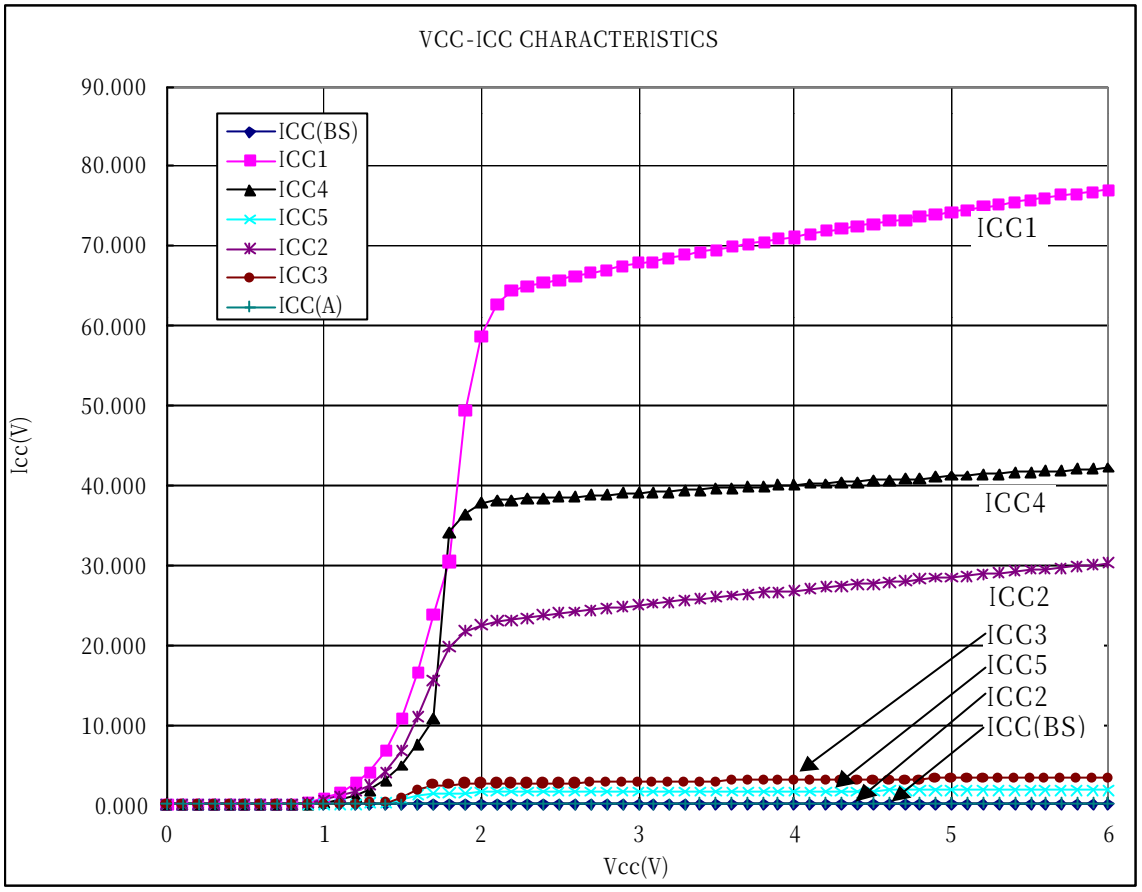
Voltage Gain	G5	—	—	—	0	—	dB
Maximum Output Level	DR5	—	THD = 3%	—	3	—	Vp-p
Input Bias Current	I BIAS	1	—	—	1.5	2.5	μA
Output DC Voltage	Vop	1	—	0.7	1.0	1.3	V

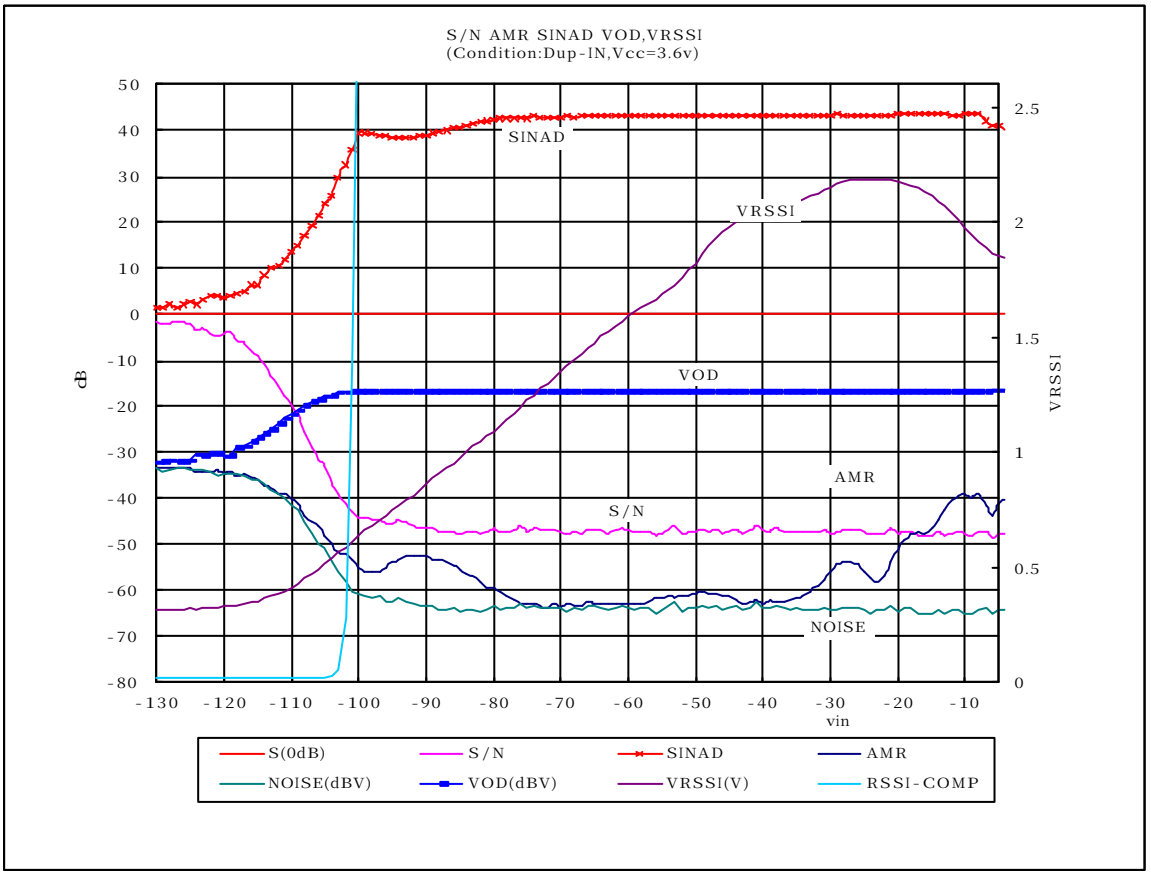
TEST CIRCUIT 1(DC)

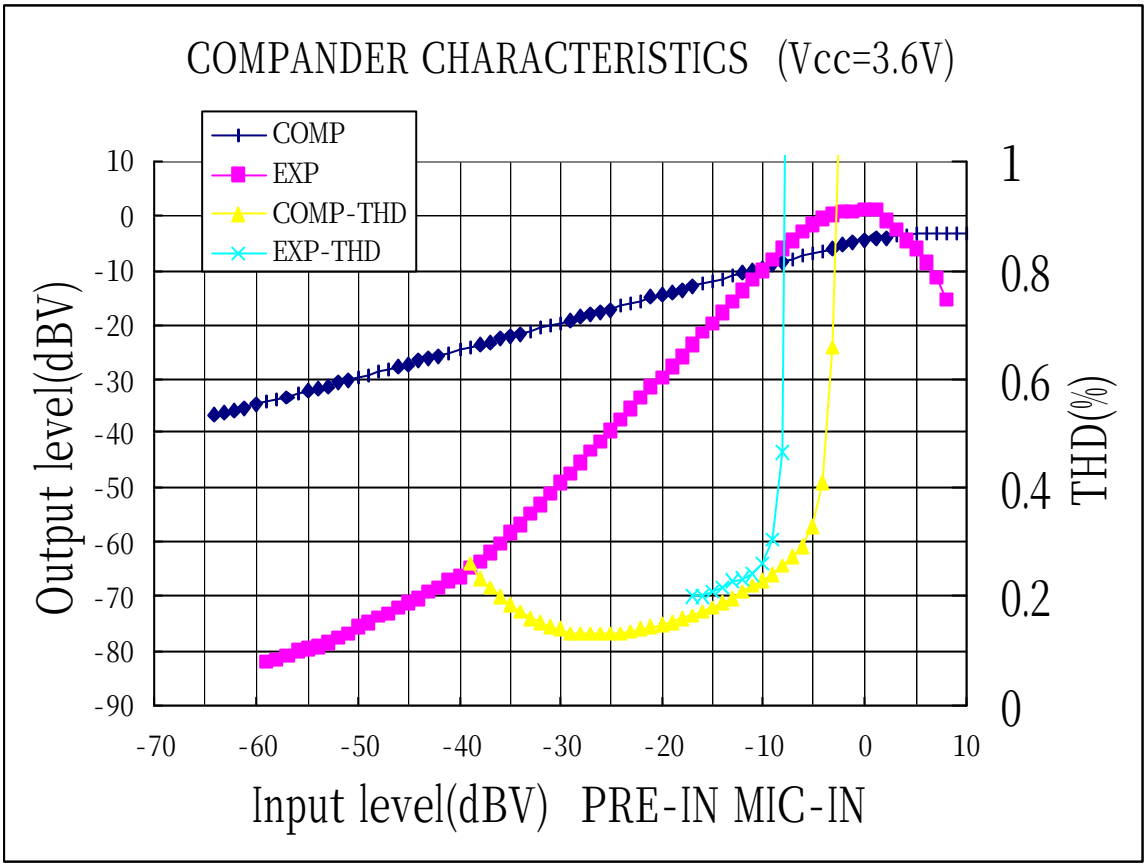


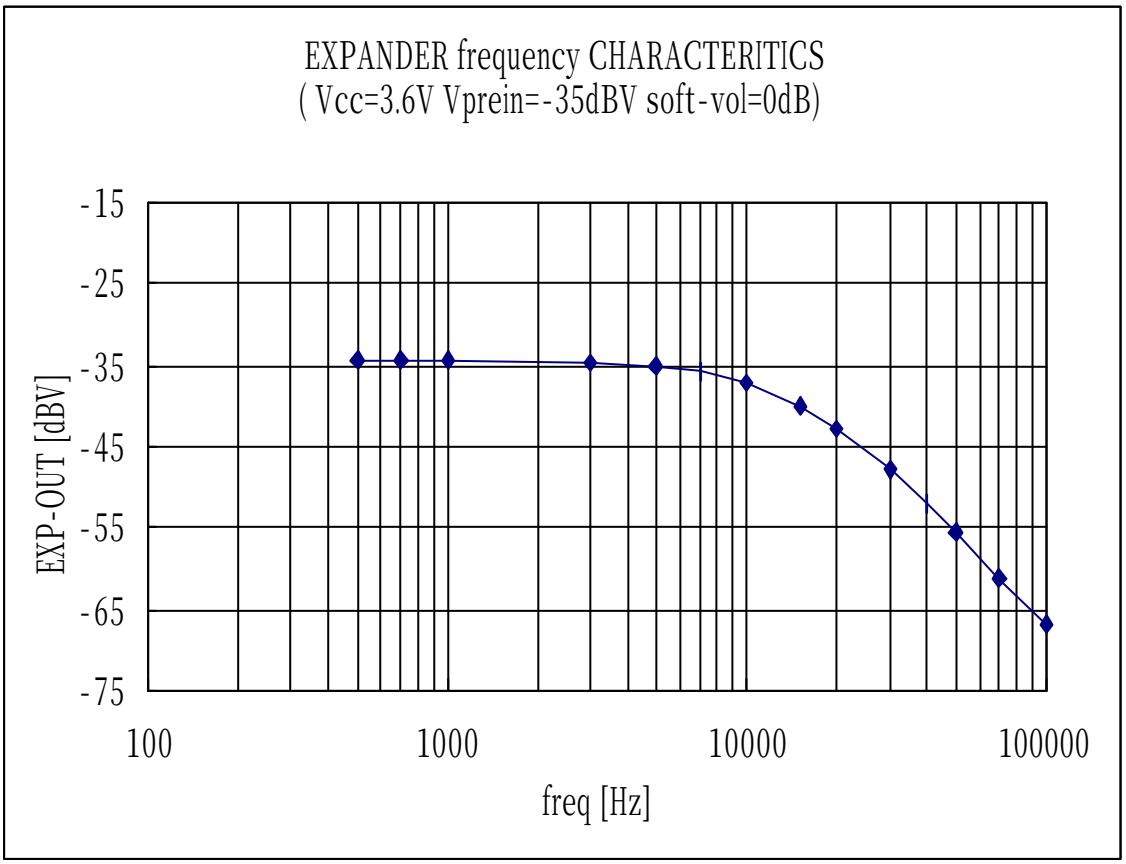
TEST CIRCUIT2(AC)

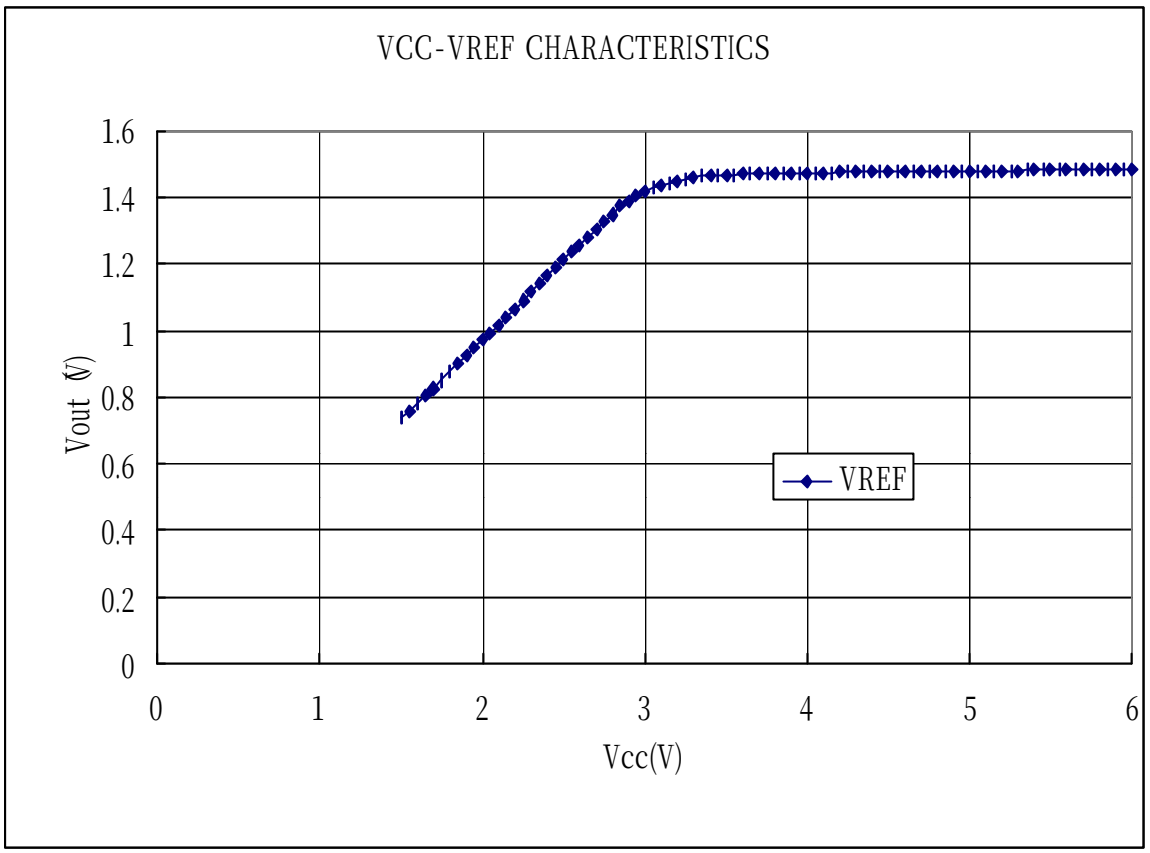


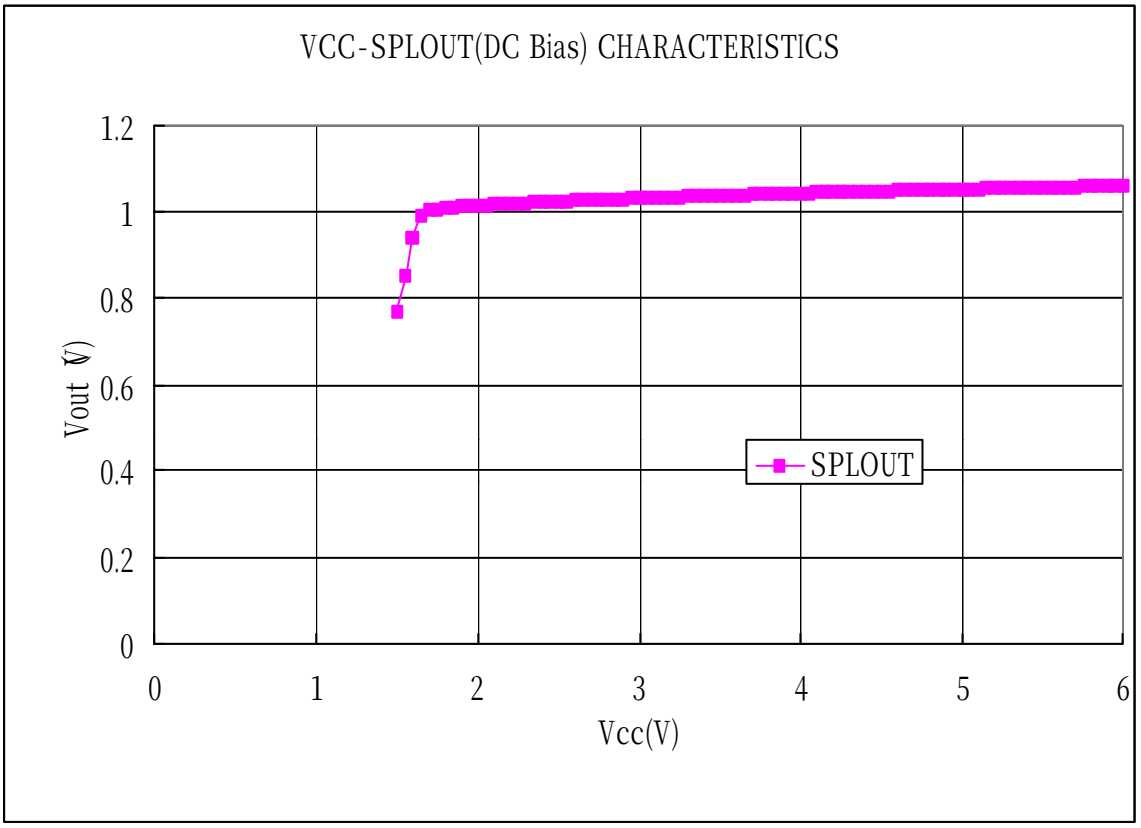

VCC-ICC CHARACTERISTICS
90.000
80.000
70.000
60.000
50.000
40.000
30.000
20.000
10.000
0.000
Icc(V)
0
1
2
3
4
5
6
Vcc(V)
ICC(BS)
ICC1
ICC4
ICC5
ICC2
ICC3
ICC(A)
ICC1
ICC4
ICC2
ICC3
ICC5
ICC2
ICC(BS)

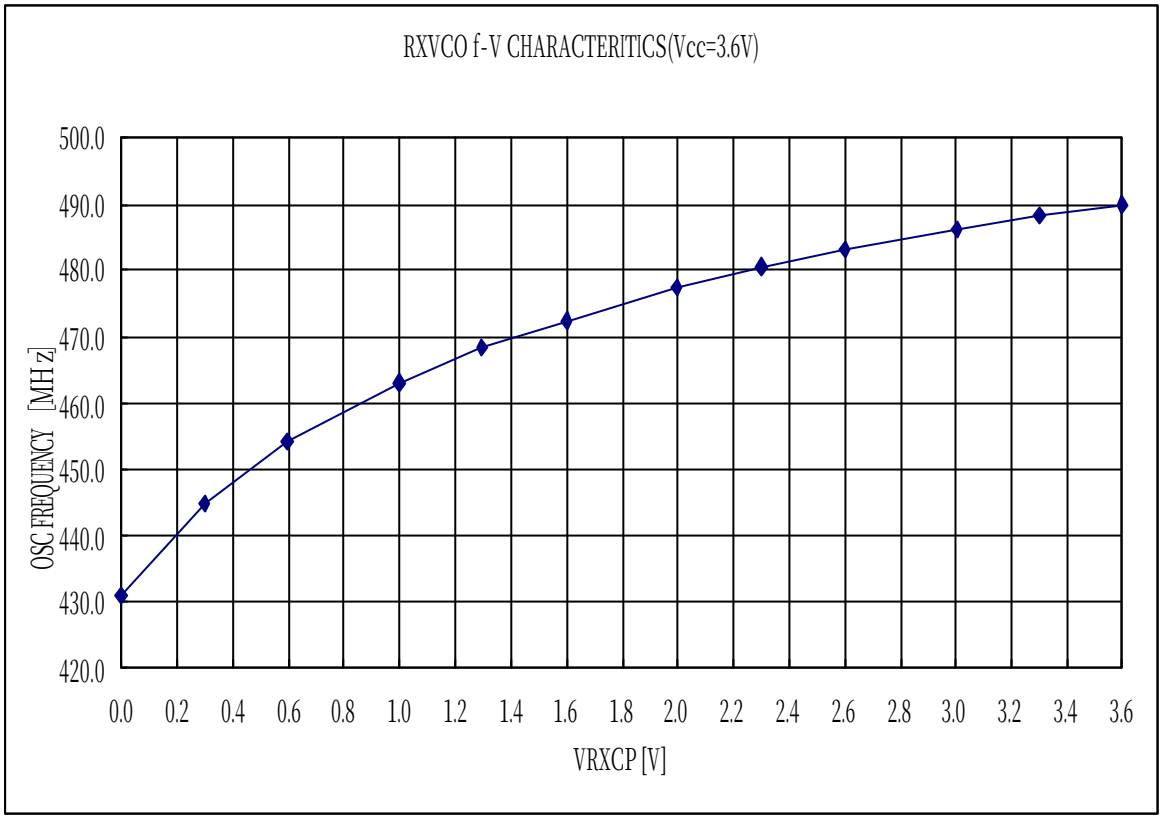

S/N AMR SINAD VOD,VRSSI
(Condition:Dup-IN,Vcc=3.6v)
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
-80
dB
2.5
2
1.5
1
0.5
0
VRSSI
-130
-120
-110
-100
-90
-80
-70
-60
-50
-40
-30
-20
-10
vin
SINAD
VRSSI
VOD
AMR
S/N
NOISE
S(0dB)
S/N
SINAD
AMR
NOISE(dBV)
VOD(dBV)
VRSSI(V)
RSSI-COMP

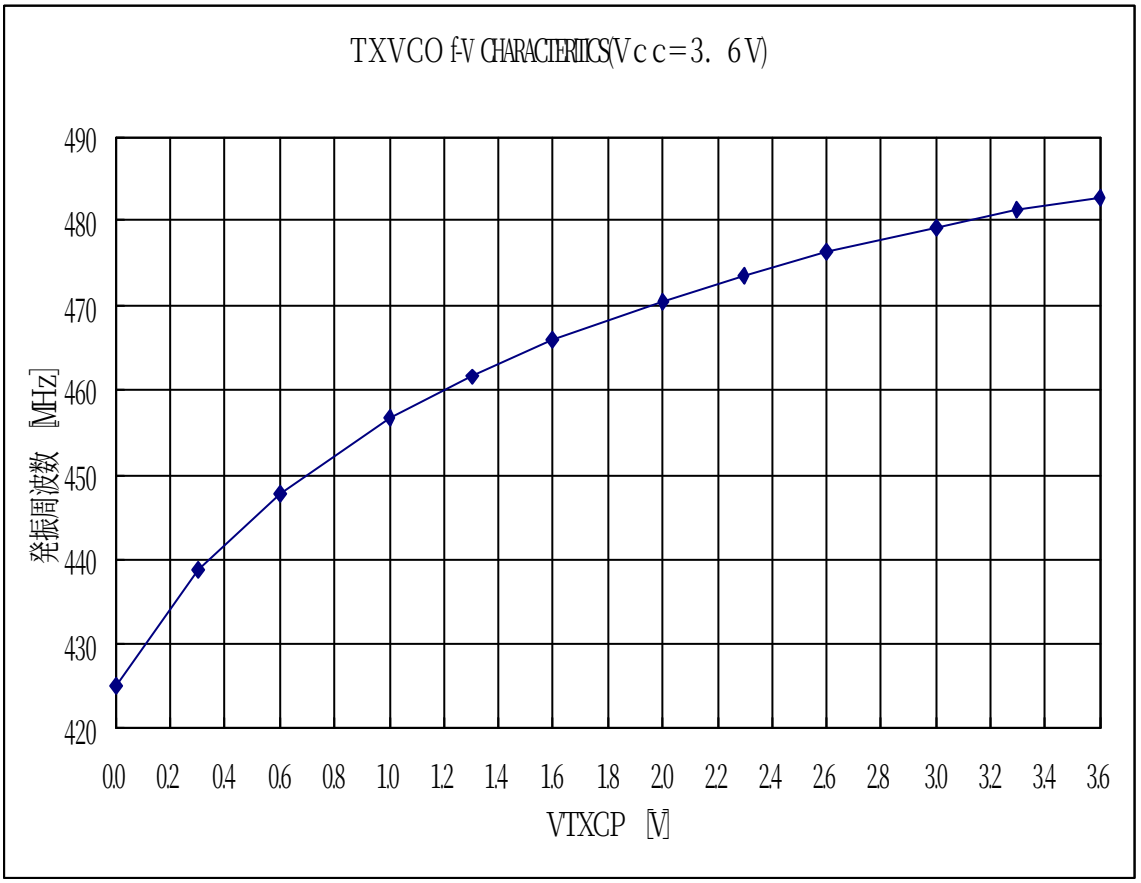

COMPANDER CHARACTERISTICS (Vcc=3.6V)
COMP
EXP
COMP-THD
EXP-THD
Output level(dBV)
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
1
0.8
0.6
0.4
0.2
0
THD(%)
-70
-60
-50
-40
-30
-20
-10
0
10
Input level(dBV) PRE-IN MIC-IN

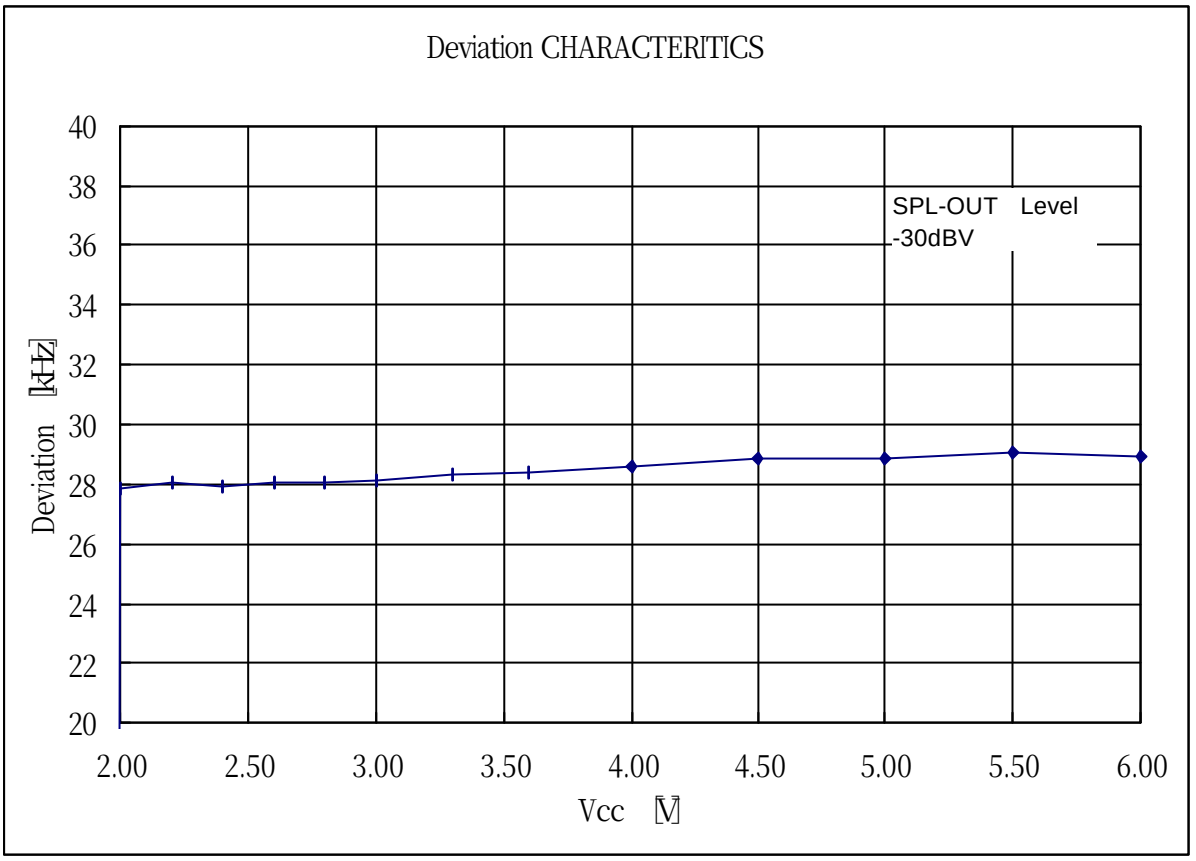

EXPANDER frequency CHARACTERITICS
(Vcc=3.6V Vprein=-35dBV soft-vol=0dB)
EXP-OUT [dBV]
-15
-25
-35
-45
-55
-65
-75
100
1000
10000
100000
freq [Hz]


VCC-VREF CHARACTERISTICS
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Vout (V)
0
1
2
3
4
5
6
Vcc(V)
VREF


VCC-SPLOUT(DC Bias) CHARACTERISTICS
1.2
1
0.8
0.6
0.4
0.2
0
Vout (V)
0
1
2
3
4
5
6
Vcc(V)
SPLOUT

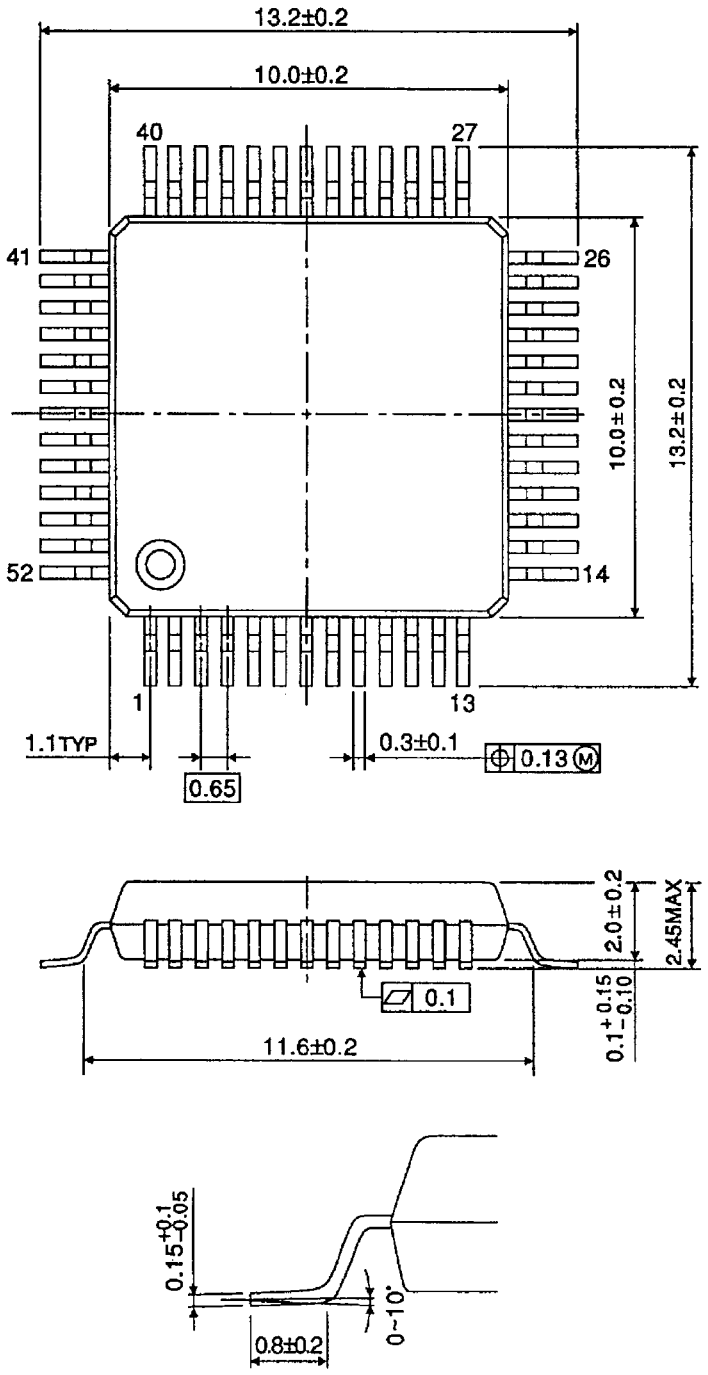

RXVCO f-V CHARACTERITICS(Vcc=3.6V)
OSC FREQUENCY [MHz]
500.0
490.0
480.0
470.0
460.0
450.0
440.0
430.0
420.0
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6
VRXCP [V]


TXVCO f-V CHARACTERITICS(Vcc=3.6V)
発振周波数 [MHz]
490
480
470
460
450
440
430
420
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6
VTXCP [V]


Deviation CHARACTERITICS
SPL-OUT Level
-30dBV
Deviation [kHz]
40
38
36
34
32
30
28
26
24
22
20
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
Vcc [V]

Outline Drawing

QFP52-P-1010-0.65 Unit : mm



RESTRICTIONS ON PRODUCT USE

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