EXHIBIT C

PAD-1000 Theory of Operation

ProNet Tracking Systems

Personal Alarm Device

Model PAD-1000

Theory of Operation

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1. Introduction

ProNet Tracking Systems' Campus-911 System is a Wireless Personal Security System developed for operation in a campus environment. The system operates in the 902 to 928 MHz frequency band, and employs frequency-hopping to obtain diversity. Personal Alarm Devices (PAD's) are battery operated, hand-held transceivers carried by subscribers, allowing them to summon help in emergency situations.

2. General Theory Of Operation

2.1 Alarm Transmit Function

In an alarm situation, the user presses both of the activation buttons on the PAD-1000 simultaneously, causing it to repeatedly generate alarm event transmissions to Campus-911 receivers. During each event, the PAD-1000 transmits on each of five different frequencies, chosen as the next five in a 50-channel pseudo-random table, and listens at the end of each transmission for an acknowledgement from the system. The reception of acknowledgements causes the PAD-1000 to blink its LED indicator to signify system reception of the alarm message. Additionally, there is a brief pause before the next event, causing events to occur at a rate of about once per second. This process is repeated indefinitely until help arrives at the alarm scene, allowing the system to accurately locate the source of the transmissions.

2.2 Test Transmit Function

The PAD-1000 may also be tested at any time by pressing the two activation buttons in sequence rather than simultaneously. This process causes the device to begin a sequence of up to ten transmissions on different frequencies (again chosen as the next ten channels from the 50-channel pseudo-random table), each being followed by a listening period in which the system may acknowledge the test. In this case, the PAD-1000 ceases its transmissions upon reception of the first acknowledgement, and blinks its LED indicator to signify a successful test.

2.3 Acknowledgement Receive Function

As mentioned above, the PAD-1000 is a transceiver, allowing it to not only transmit alarm and test events, but also to receive acknowledgements from the system. This feature permits real-time testing of the PAD-1000 and the system itself anywhere in the coverage area, and allows positive LED feedback to the user that the system has received the alarm message in an alarm situation.

3. Top Level Block Diagram and Physical Configuration

Figure 1 is the block diagram of the PAD-1000 units. Figure 2 shows the physical configuration of the PAD-1000.

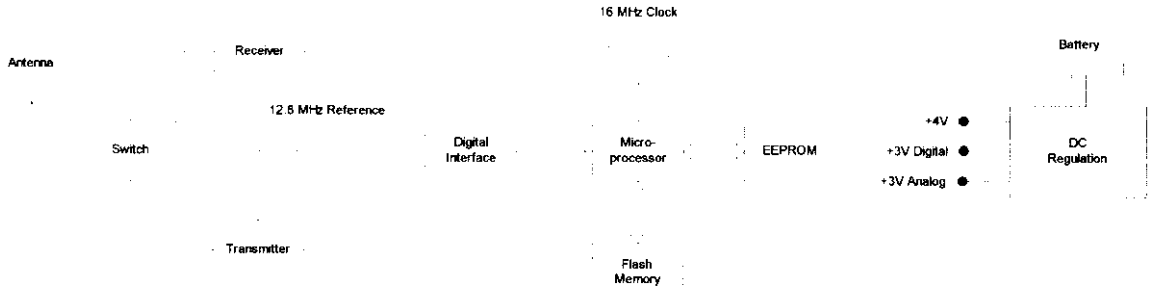

Figure 1. PAD-1000 Block Diagram

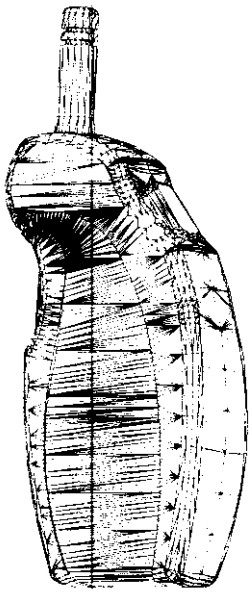

Figure 2. PAD-1000 Physical Configuration

4. Detailed Block Diagram and Functional Description

4.1 Radio Section

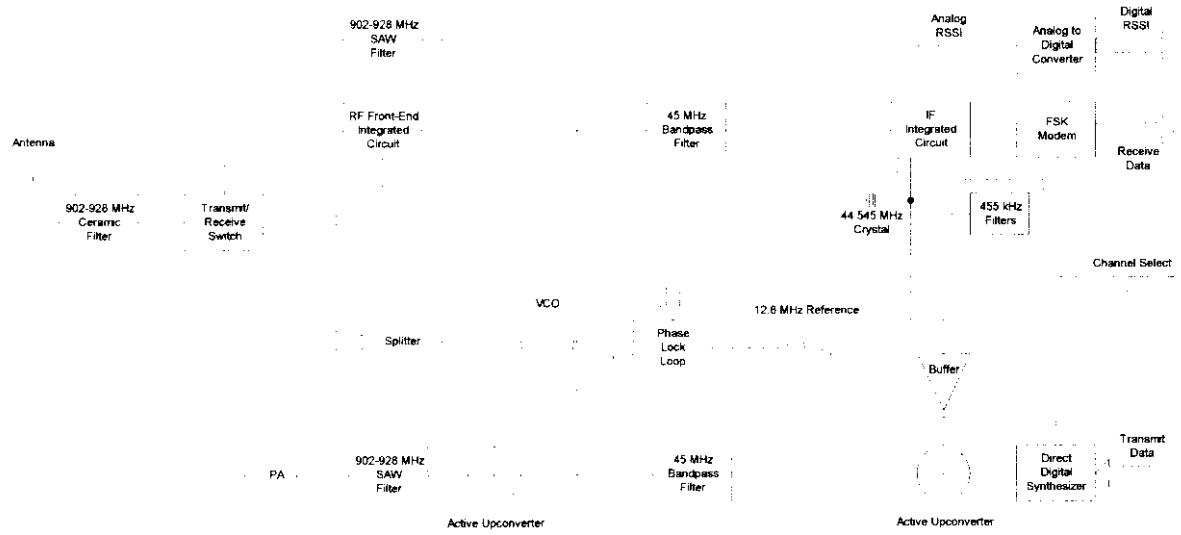

Figure 3. Block Diagram of PAD-1000 Radio Section

Figure 3. Shows the detailed block diagram of the PAD-1000 radio section. The radio uses FSK modulation at 15625 bits per second, and utilizes channels of 25 kHz bandwidth. All transmissions are hopped over 50 channels chosen from a pseudo-random table, with equal transmission time on all channels. Transmissions are typically of 40 to 90 ms duration on a given channel, and never exceed 400 ms duration. The radio is half-duplex; meaning it is either receiving or transmitting at any given time.

4.1.1 Antenna

The antenna used in the PAD-1000 is a small "rubber-duck" vertical antenna that protrudes from the top of the hand-held unit. Because of its small size and the limited size of the "ground plane" in the antenna system, the gain of this antenna configuration is -4 dBi.

4.1.2 Tunable Local Oscillator

4.1.2.1 12.8 MHz TCXO

A temperature compensated crystal oscillator (TCXO) at 12.8 MHz is used as the reference frequency for the phase-lock loop and direct digital synthesizer. This reference oscillator is specified to be accurate to within ± 2.5 PPM over the temperature range of –30 to +75 C.

4.1.2.2 Voltage Controlled Oscillator

The local oscillator signal originates in the voltage controlled oscillator, which is tuned between 859.800 and 869.750 MHz at a constant 45 MHz offset from the receive or transmit frequencies in the 904.800 to 914.750 MHz range.

4.1.2.3 Phase Lock Loop

The phase-lock loop integrated circuit tunes the voltage-controlled oscillator to a given channel based on the control words received from the microprocessor. Tuning is achieved in 600 µs.

4.1.3 Receiver

The receiver architecture is dual-downconversion, with intermediate frequencies of 45 MHz and 455 kHz. The first conversion is performed in the RF front-end integrated circuit, the second conversion is performed in the IF integrated circuit, which generates its own LO signal using a 44.545 MHz crystal oscillator.

4.1.3.1 902-928 MHz Ceramic Bandpass Filter

A three-section ceramic bandpass filter has been used at the antenna port of the radio receiver front-end. Note that this filter also appears in the transmit signal path. The selected filter has excellent out-of-band rejection to eliminate undesired signals received at the antenna and reduce emissions other than the desired RF output during transmission.

4.1.3.2 Transmit/Receive Switch

An integrated circuit GaAs MESFET switch is used to switch the antenna between transmit and receive functions. The unit does not transmit and receive simultaneously.

4.1.3.3 RF Integrated Circuit

A RF front-end integrated circuit provides both the low-noise-amplifier and first mixer functions of the PAD-1000 receiver. The mixer converts the incoming RF signals to a fixed 45 MHz first intermediate frequency using the tunable local oscillator signal.

4.1.3.4 902-928 MHz SAW Bandpass Filter

The RF front-end integrated circuit utilizes an external surface-acoustic-wave (SAW) bandpass filter between its low-noise amplifier and mixer to reduce image noise and further reduce the receiver's susceptibility to out-of-band signals.

4.1.3.5 45 MHz Bandpass Filter

At the 45 MHz intermediate frequency, a monolithic crystal filter with is used to limit the bandwidth of the signal to 30 kHz prior to passing it to the intermediate frequency integrated circuit.

4.1.3.6 Intermediate Frequency Integrated Circuit

The intermediate frequency integrated circuit (IFIC) performs several functions. Using an external crystal, the IFIC generates the second local oscillator signal at 44.545 MHz. This LO is used to convert the first IF of 45 MHz into the second IF of 455 kHz. Several stages of limiting gain and two stages of 25 kHz wide filters prepare the signal for FM demodulation. This demodulation is performed in the IFIC using an external quadrature coil. The received modulation signal is then passed on the FSK modem. Additionally, a received signal strength indicator (RSSI) signal is produced in the IFIC and passed to an analog-to-digital converter.

4.1.3.7 FSK Modem

The FSK modem integrated circuit converts the received modulating signal into a data bit stream that is passed along to the microprocessor. The conversion involves synchronization based upon zero-crossings in the modulation, which allows bit decisions to be made at optimum times.

4.1.3.8 RSSI Analog-to-Digital Converter

An eight-bit analog-to-digital converter is used to convert the RSSI signal generated by the IFIC into a digital form which can be read as desired by the microprocessor.

4.1.4 Transmitter

In a manner quite analogous to the receiver, the transmitter uses a dual-upconversion architecture. The signal originates in a direct digital synthesizer centered about 455 kHz, and is then converted to 45 MHz and finally to the desired RF frequency in the 904.800 to 914.750 MHz range. Transmit power is typically 18 dBm at the antenna port, and the antenna gain is -4 dBi.

4.1.4.1 Direct Digital Synthesizer

The FSK signal is originally generated in the direct digital synthesizer (DDS). In the PAD-1000, the DDS function is performed within a complex programmable logic device (CPLD), which is programmed according to a custom ProNet algorithm. The microprocessor directs the DDS to generate either one or the other of two tones on either side of the center frequency of 455 kHz. The 12.8 MHz TCXO signal is used as the clock, and this signal is responsible for the frequency accuracy of the two tones.

4.1.4.2 First Upconversion Mixer

In the first integrated circuit upconversion mixer, the output of the DDS is mixed with the crystal oscillator signal at 44.545 MHz that is produced by the IFIC. The result is an FSK modulated signal centered at 45 MHz.

4.1.4.3 45 MHz Bandpass Filter

A monolithic crystal bandpass filter is used to reduce the bandwidth of the transmit signal to 25 kHz, and to remove the image signal at 44.090 MHz and local oscillator signal at 44.545 MHz.

4.1.4.4 Second Upconversion Mixer

A second integrated circuit mixer is used to convert the transmit signal to the final RF frequency in the 904.800 to 914.750 MHz range. The tunable LO signal is used to select the exact channel that is used for any transmission.

4.1.4.5 902-928 MHz SAW Bandpass Filter

To reduce the levels of the local oscillator and image signals produced in the second upconversion mixer, a SAW bandpass filter is used between the mixer and the power amplifier.

4.1.4.6 Power Amplifier

An integrated circuit power amplifier boost the transmit signal level to a nominal 18 dBm at the radio output port. The transmit power level is measured on each unit in production.

4.1.4.7 902-928 MHz Ceramic Bandpass Filter

As mentioned above in the receiver section, this final filter in the transmit chain is also shared with the receive chain. The selected filter has excellent out-of-band rejection to reduce undesired emissions.

4.2 Digital Section

The microprocessor portion of the digital section is composed of a 16-bit digital signal processor, a 64k x 16 FLASH non-volatile memory for code storage and a 128-byte serial EEPROM for parameter storage. The DSP operates from a 16 MHz clock at an 8 MHz instruction rate. The functions performed include control of the radio section (frequency tuning and transmit/receive control), receive data decoding, transmit data generation, and control of the LED indicator.

A complex programmable logic device (CPLD) is used as the digital interface between the digital section and the radio section. Its primary function is address decoding and latching of commands. It also contains a section responsible for direct digital frequency synthesis.

5. Precautions Taken to Avoid Interference

5.1 RF Filtering

The transmit signal passes through a SAW bandpass and a three-section ceramic bandpass filter before reaching the output port. These filters greatly reduce spurious signals, harmonics, and out-of-band transmitter phase noise.

5.2 Shielding

The circuit boards are contained in a shielded enclosure formed by the coated plastic housing, which also provides the antenna ground plane.