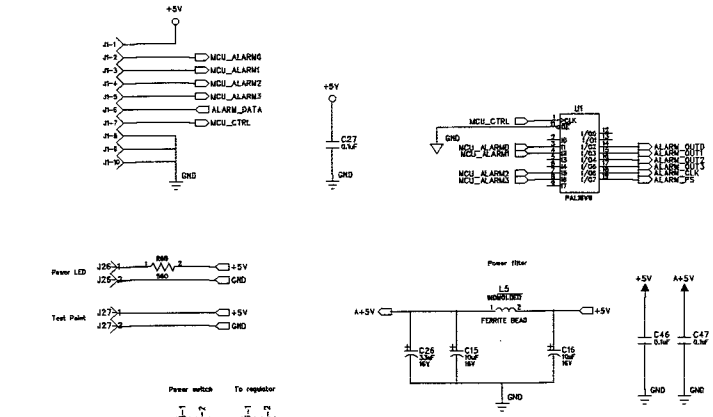
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

IO PCB

Circuit Diagram



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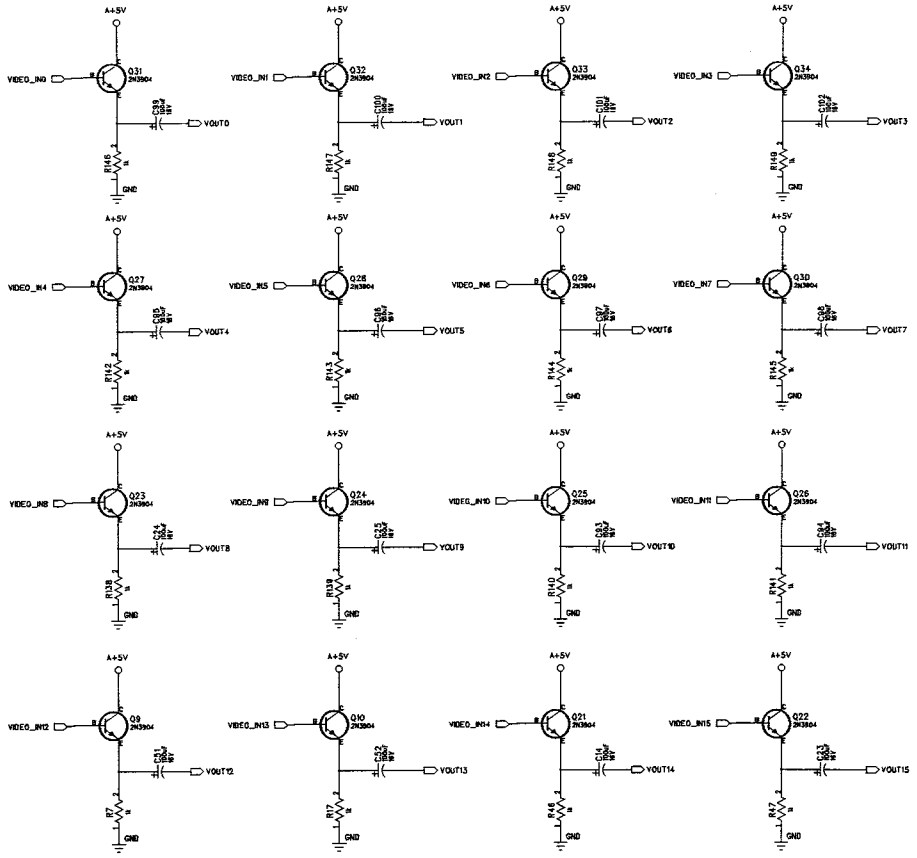
RELEASED:	DATED:	SCALE:	SHEET: 07



VR-4042
VR-4021

VR-8084
VR-8042

VR-16168
VR-16084

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY:			
TITLE:			
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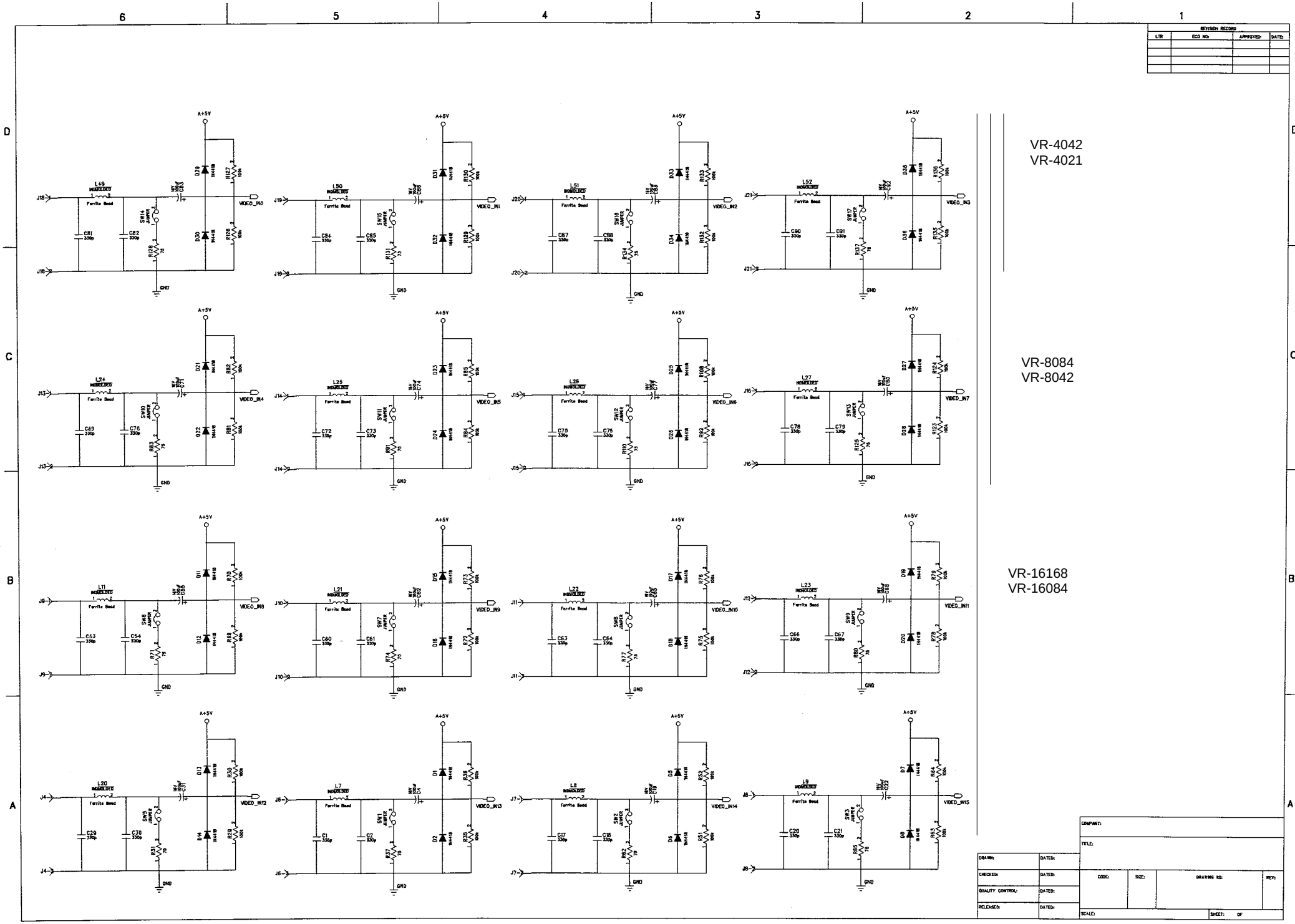
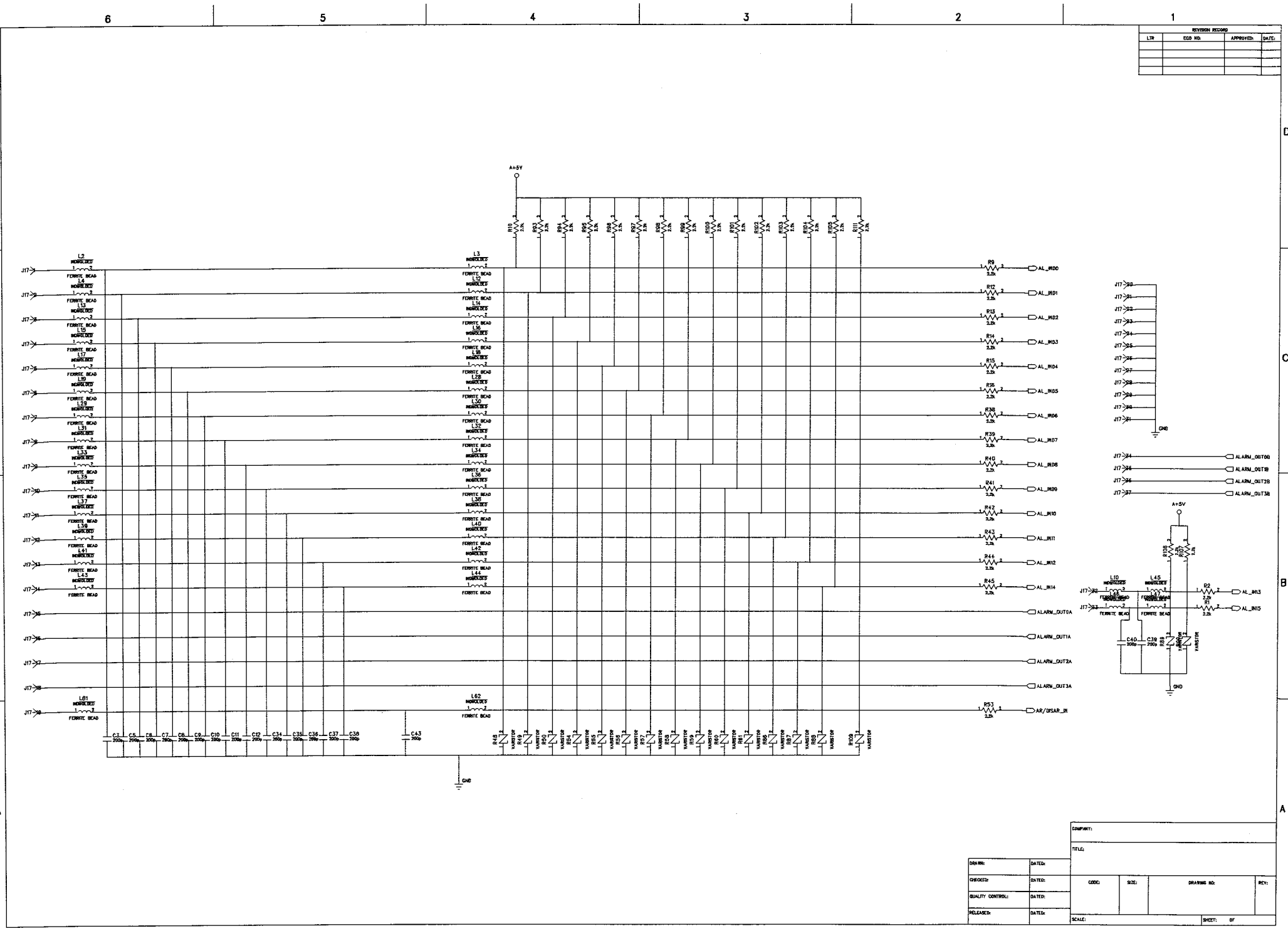


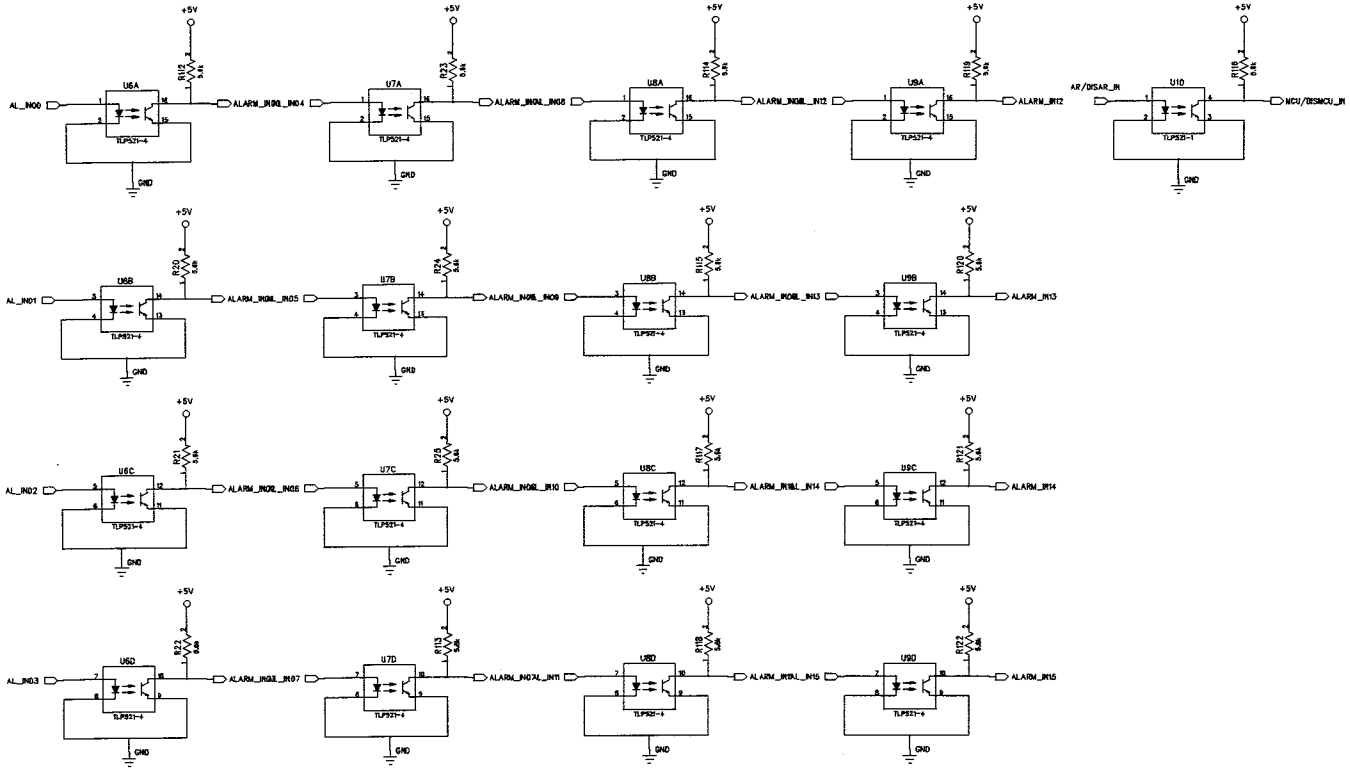
app_iob.sch-3 - Fri Aug 2 16:58:55 2002



VR-4042
VR-4021

VR-8084
VR-8042

VR-16168
VR-16084



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COMPANY:					
TITLE:					
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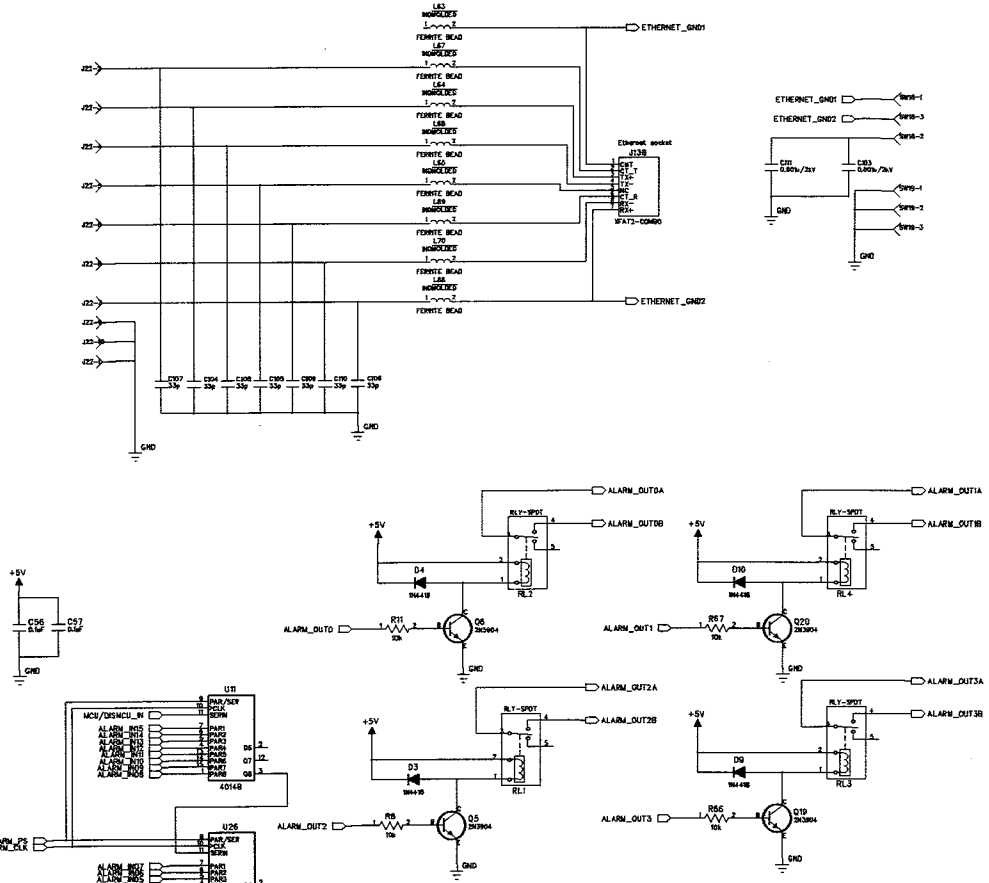
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: OF	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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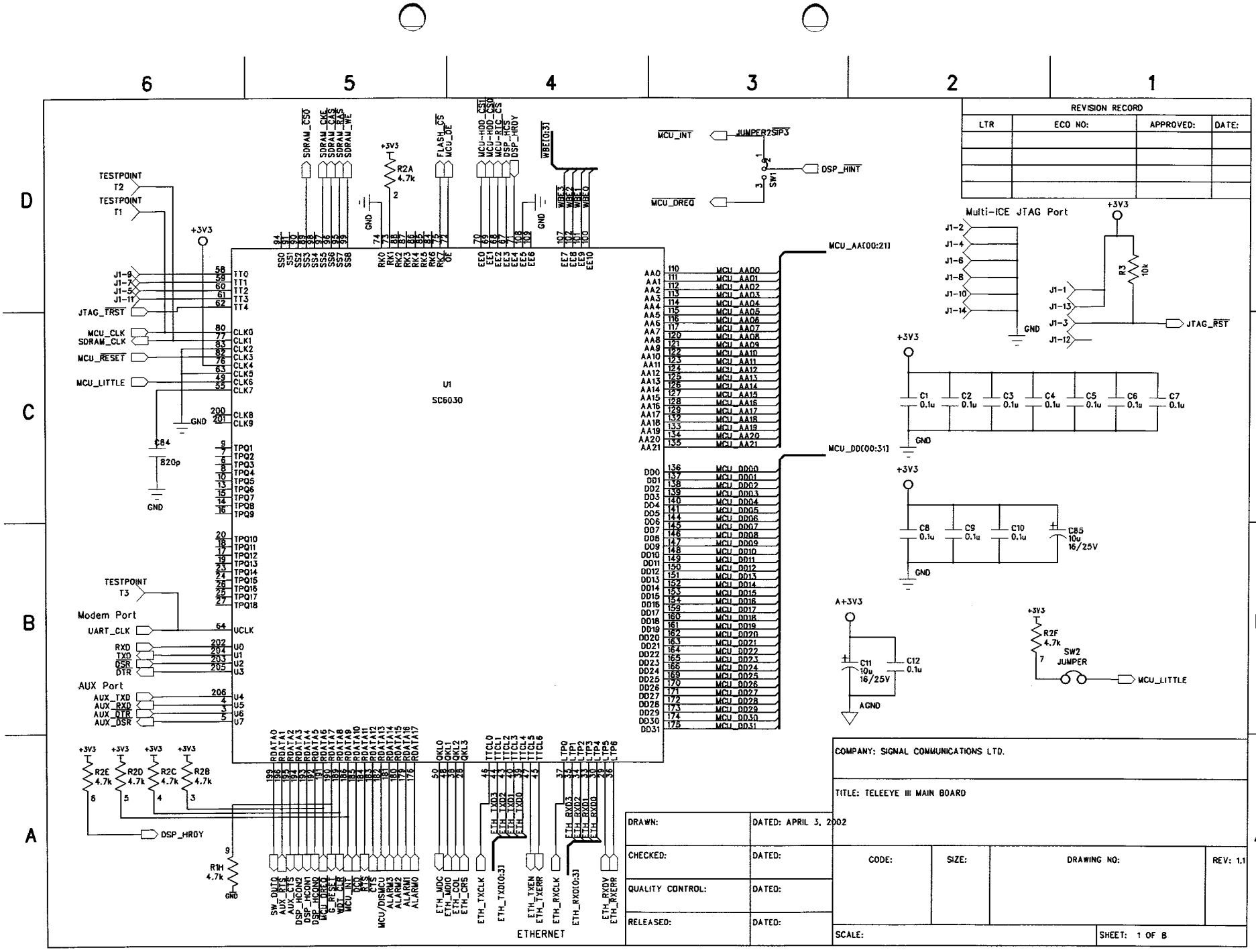
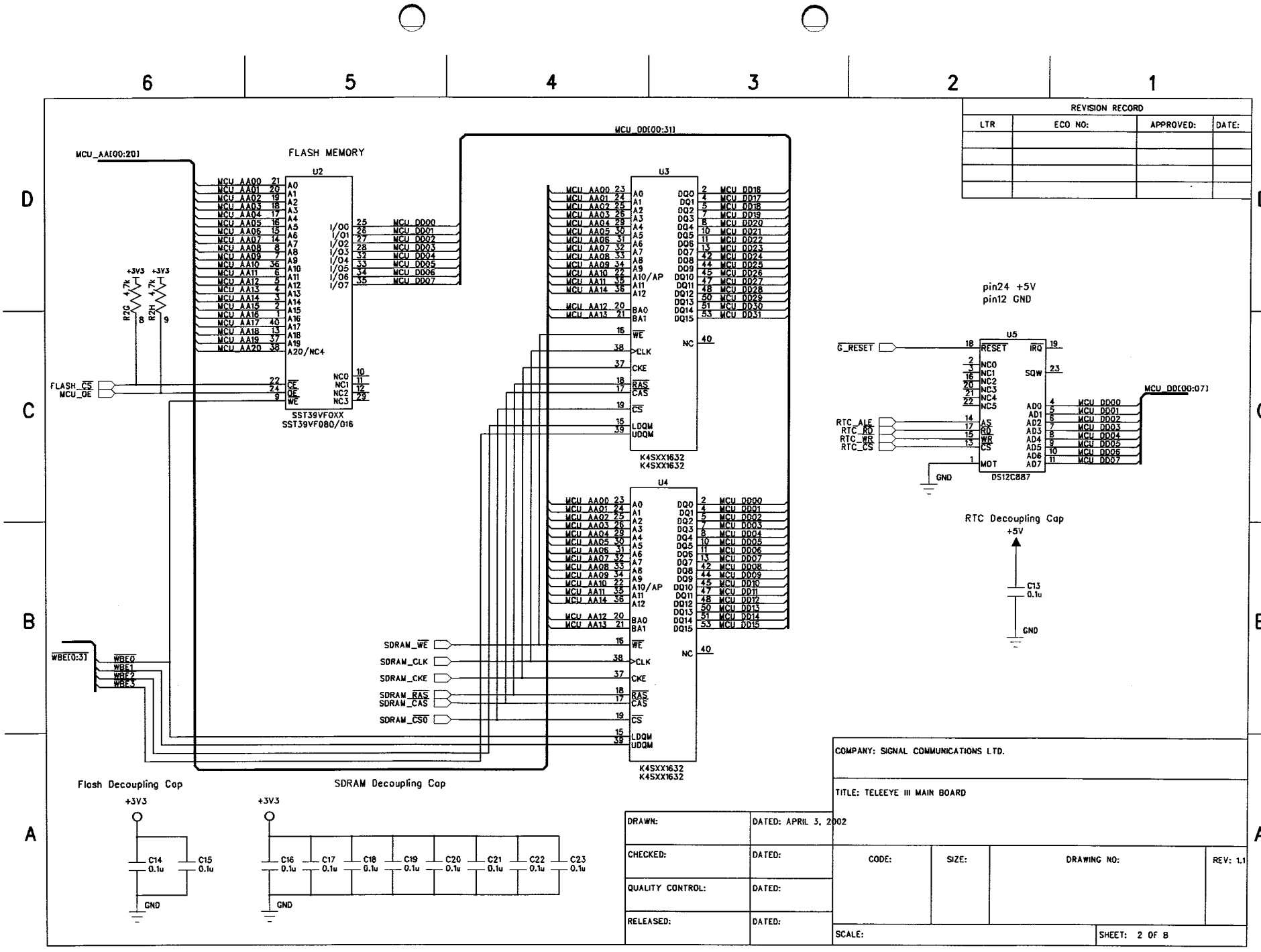


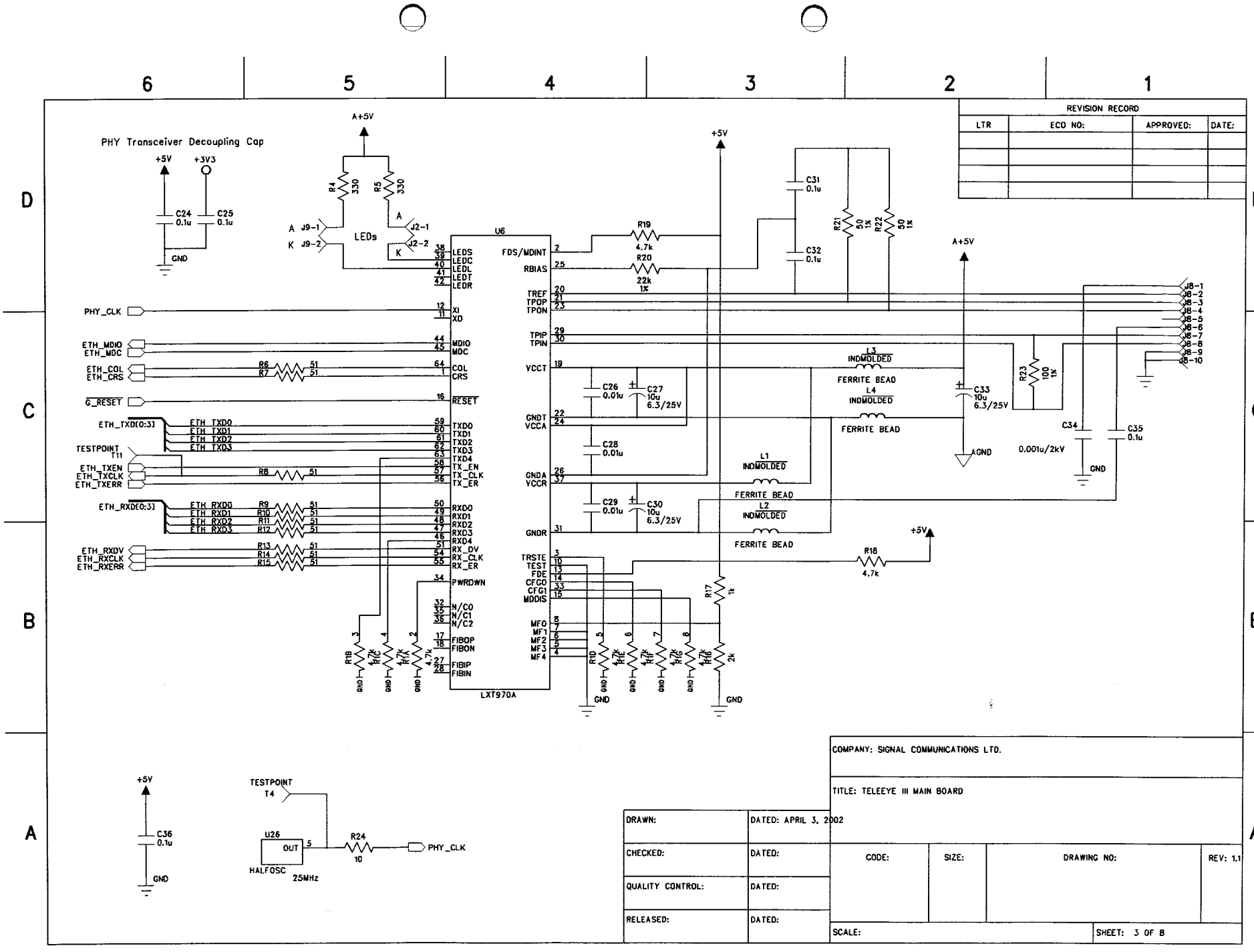
app_mb.sch-1 - Thu Apr 4 16:03:21 2002

Main PCB Circuit Diagram



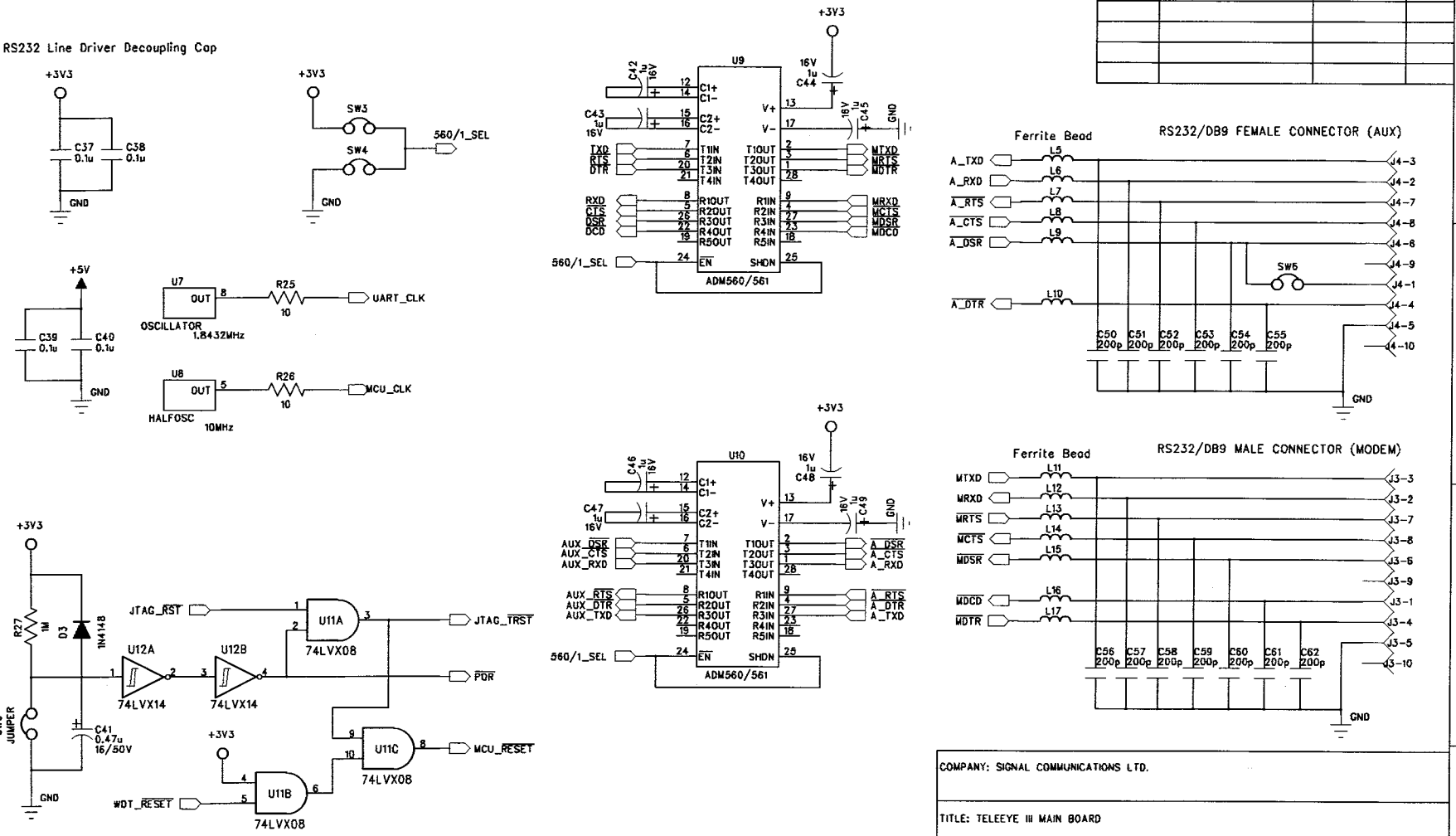
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN:	DATED: APRIL 3, 2002	COMPANY: SIGNAL COMMUNICATIONS LTD.		
CHECKED:	DATED:	TITLE: TELEEYE III MAIN BOARD		
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO: REV: 1.1
RELEASED:	DATED:	SCALE:		SHEET: 2 OF 8



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

RS232 Line Driver Decoupling Cap



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CHECKED:	DATED:	TITLE: TELEEYE III MAIN BOARD			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV: 1.1
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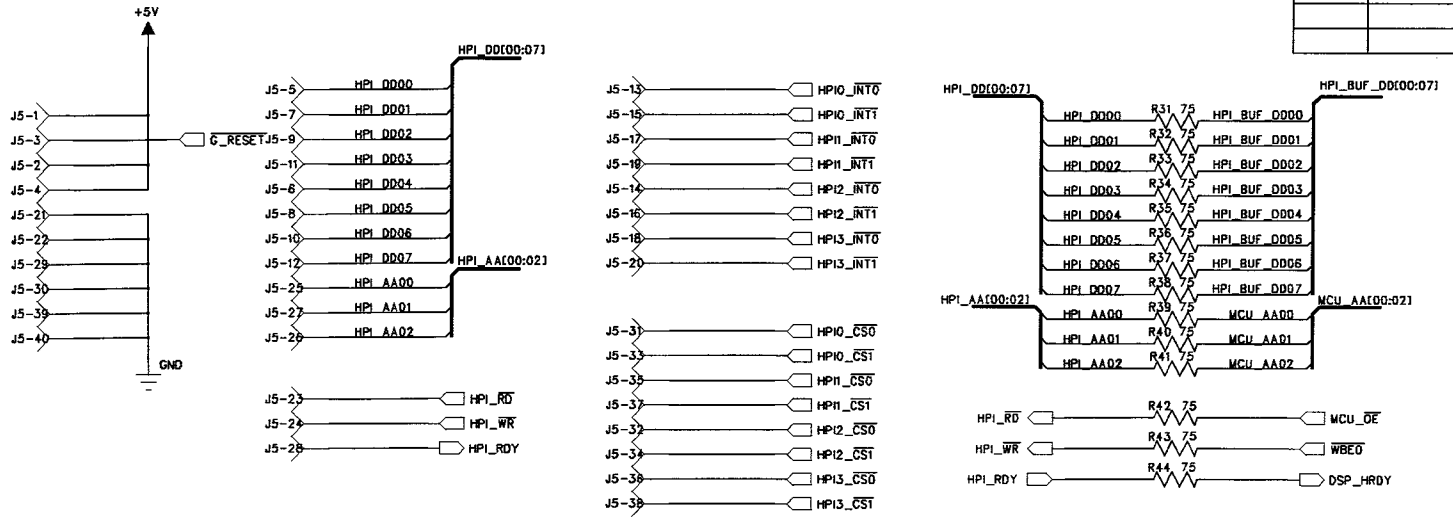
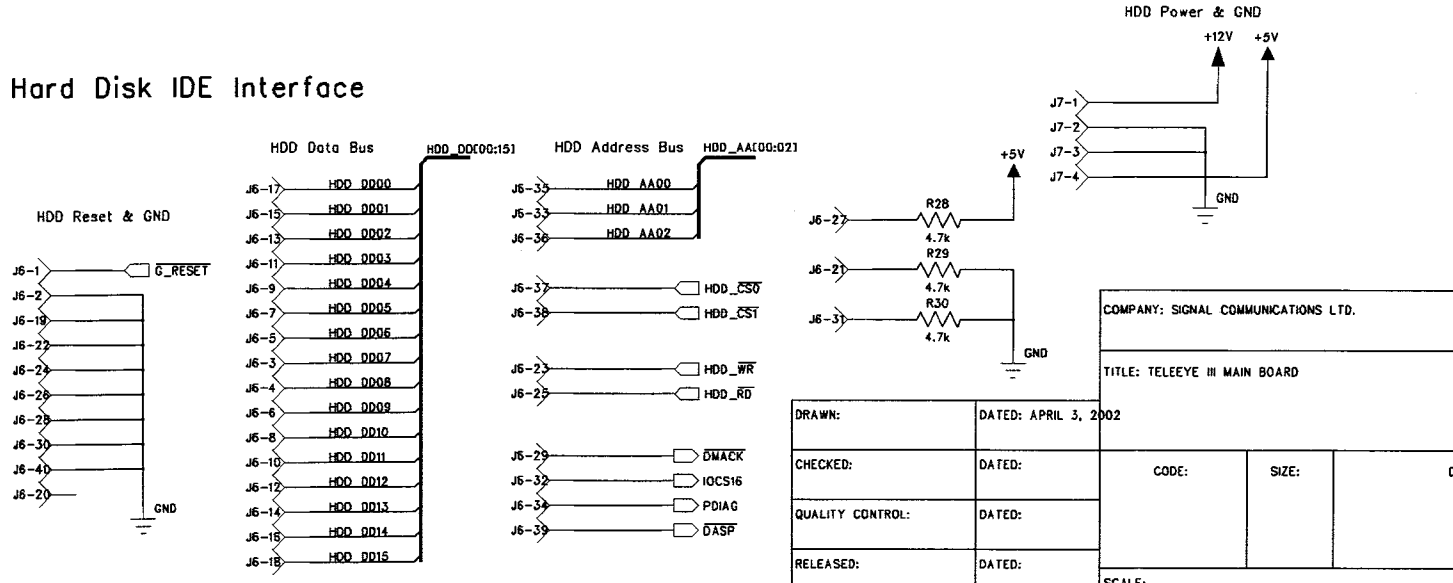
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Host Port Interface



Hard Disk IDE Interface



COMPANY: SIGNAL COMMUNICATIONS LTD.				
TITLE: TELEEYE III MAIN BOARD				
DRAWN:	DATED: APRIL 3, 2002	CODE:	SIZE:	DRAWING NO: REV: 1.1
CHECKED:	DATED:			
QUALITY CONTROL:	DATED:			
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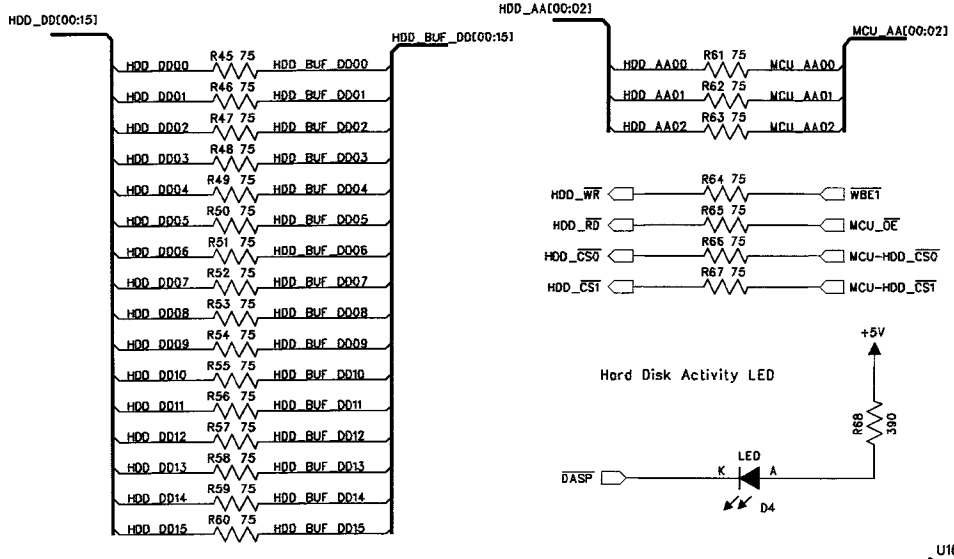
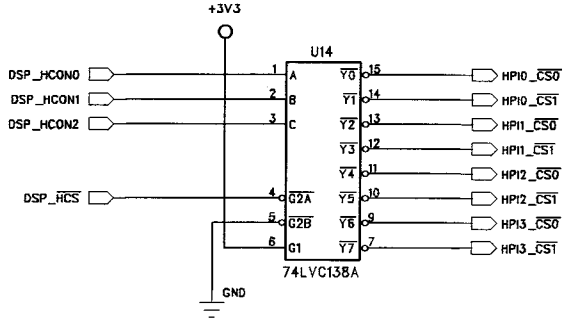
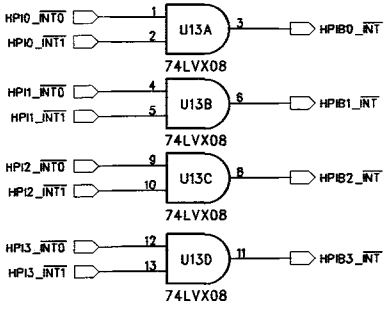
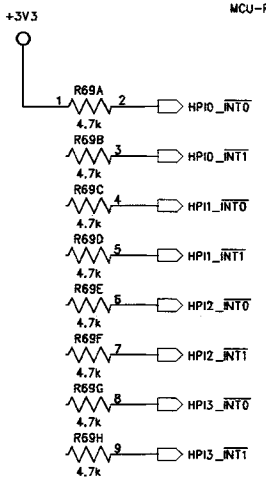
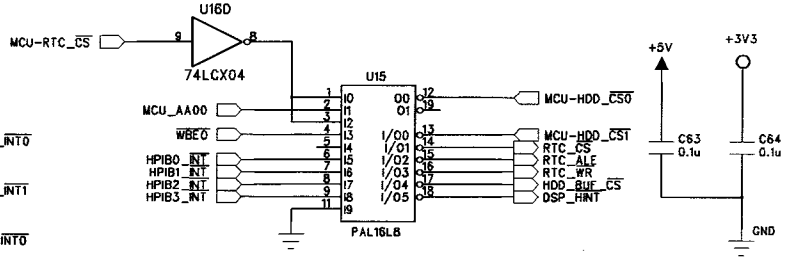
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



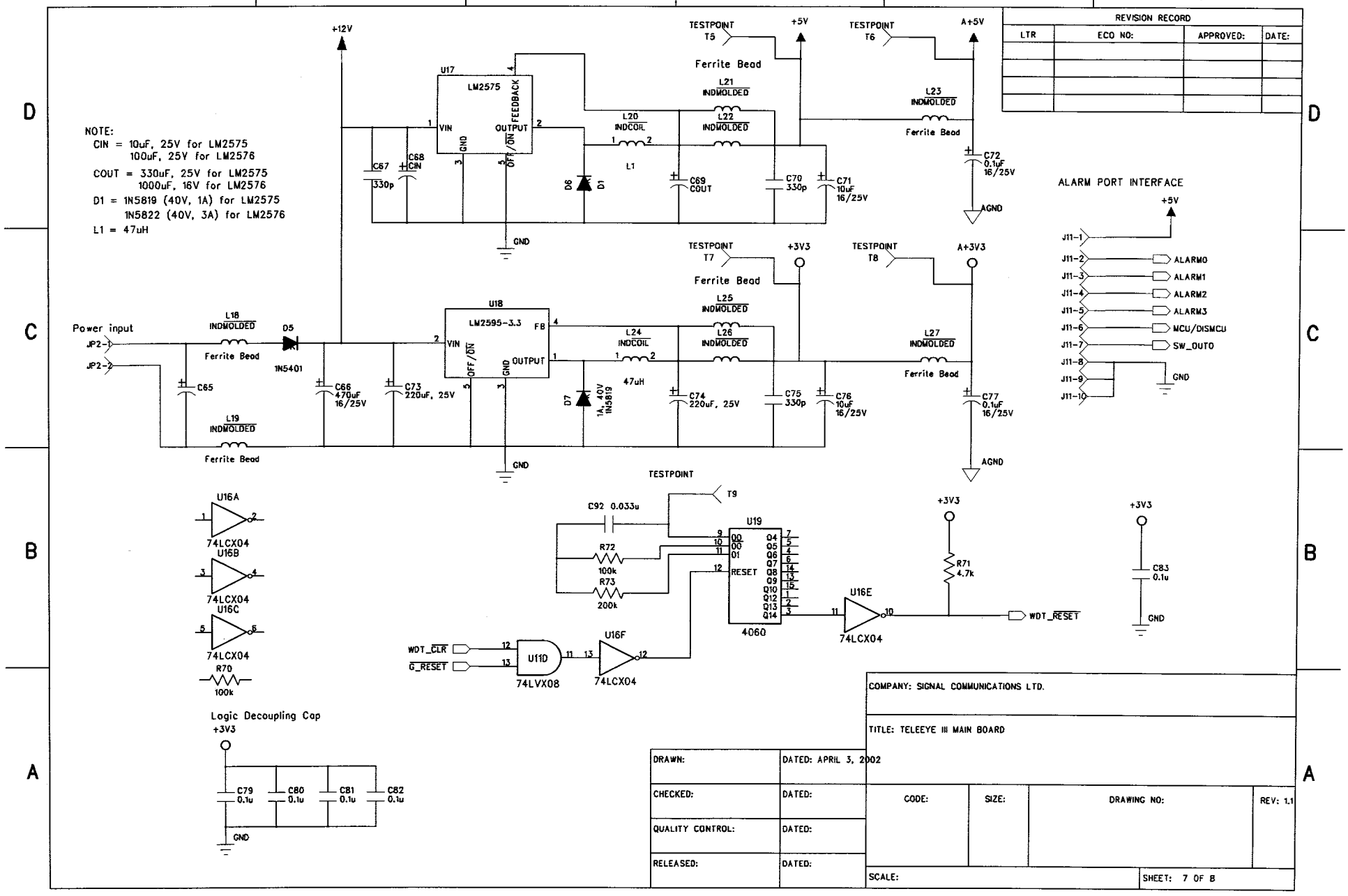








COMPANY: SIGNAL COMMUNICATIONS LTD.					
TITLE: TELEEYE III MAIN BOARD					
DRAWN:	DATED: APRIL 3, 2002	CODE:	SIZE:	DRAWING NO:	REV: 1.1
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: 6 OF 8	


6
5
4
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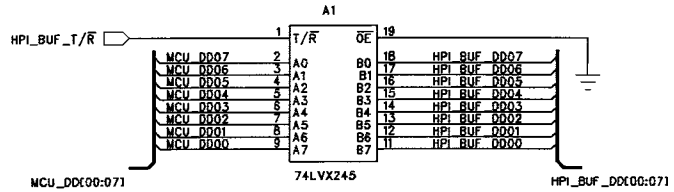
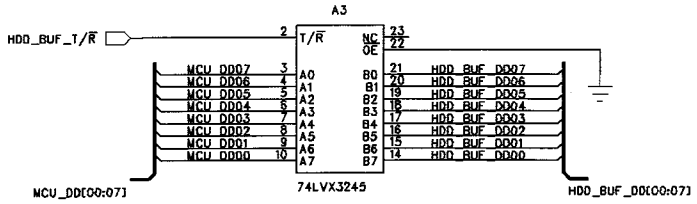
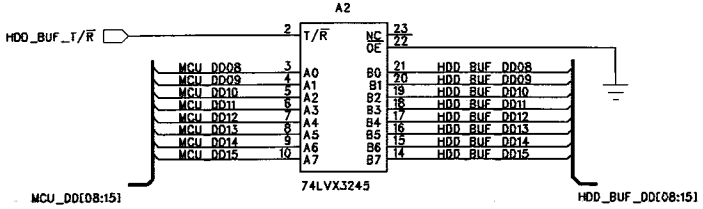
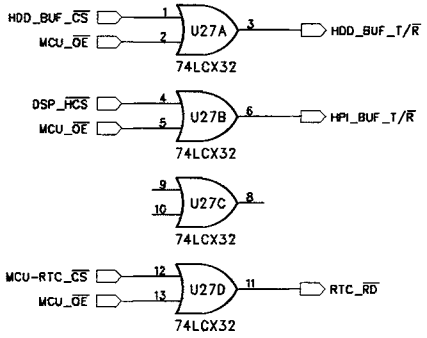
1
D
C
B
A
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
NOTE:
CIN = 10uF, 25V for LM2575
100uF, 25V for LM2576
COUT = 330uF, 25V for LM2575
1000uF, 16V for LM2576
D1 = 1N5819 (40V, 1A) for LM2575
1N5822 (40V, 3A) for LM2576
L1 = 47uH
+12V
U17
LM2575
VIN
OUTPUT
GND
FEEDBACK
ON/OFF
C67 330p
C68 CIN
L1
D6
D1
C69 COUT
C70 330p
C71 10uF 16/25V
GND
TESTPOINT T5
+5V
Ferrite Bead
L21 INDMOLDED
L22 INDMOLDED
L20 INDCOIL
TESTPOINT T6
A+5V
L23 INDMOLDED
Ferrite Bead
C72 0.1uF 16/25V
AGND
ALARM PORT INTERFACE
+5V
J11-1
J11-2 ALARM0
J11-3 ALARM1
J11-4 ALARM2
J11-5 ALARM3
J11-6 MCU/DISMCU
J11-7 SW_OUT0
J11-8
J11-9
J11-10
GND
Power input
JP2-1
JP2-2
L18 INDMOLDED
Ferrite Bead
D5
1N5401
C65
L19 INDMOLDED
Ferrite Bead
C66 470uF 16/25V
C73 220uF, 25V
U18
LM2595-3.3
VIN
OUTPUT
GND
FB
ON/OFF
D7
1A, 40V IN5819
47uH
L24 INDCOIL
L25 INDMOLDED
L26 INDMOLDED
C74 220uF, 25V
C75 330p
C76 10uF 16/25V
GND
TESTPOINT T7
+3V3
Ferrite Bead
TESTPOINT T8
A+3V3
L27 INDMOLDED
Ferrite Bead
C77 0.1uF 16/25V
AGND
U16A
74LCX04
U16B
74LCX04
U16C
74LCX04
R70 100k
TESTPOINT T9
C92 0.033u
R72 100k
R73 200k
U19
RESET
4060
+3V3
R71 4.7k
U16E
74LCX04
WDT_RESET
+3V3
C83 0.1u
GND
WDT_CLR
G_RESET
U11D
74LVX08
U16F
74LCX04
Logic Decoupling Cap
+3V3
C79 0.1u
C80 0.1u
C81 0.1u
C82 0.1u
GND
COMPANY: SIGNAL COMMUNICATIONS LTD.
TITLE: TELEEYE III MAIN BOARD
DRAWN:
DATED: APRIL 3, 2002
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.1
SCALE:
SHEET: 7 OF 8

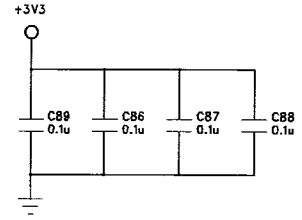
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

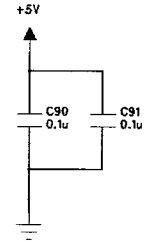












COMPANY: SIGNAL COMMUNICATIONS LTD.					
TITLE: TELEEYE III MAIN BOARD					
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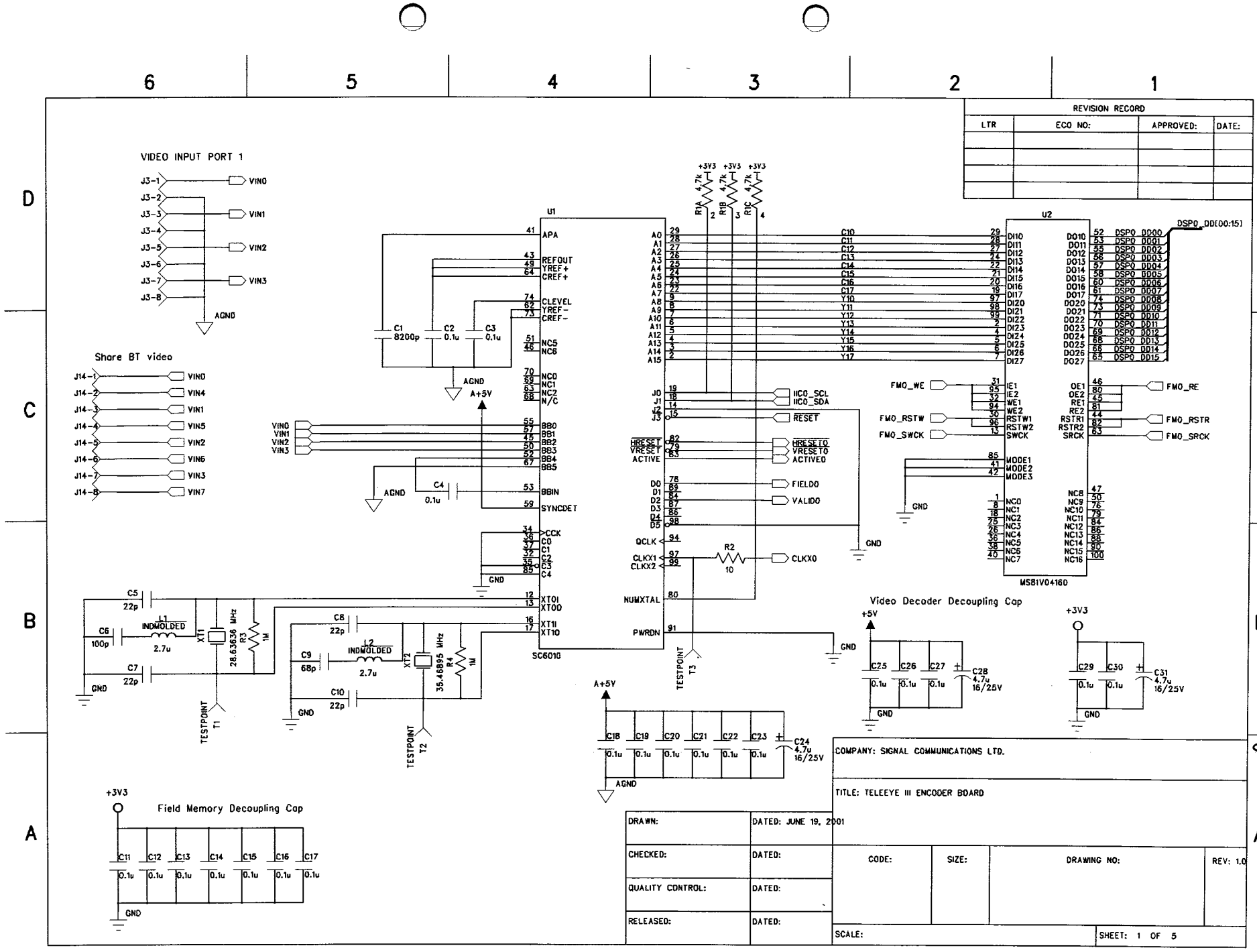
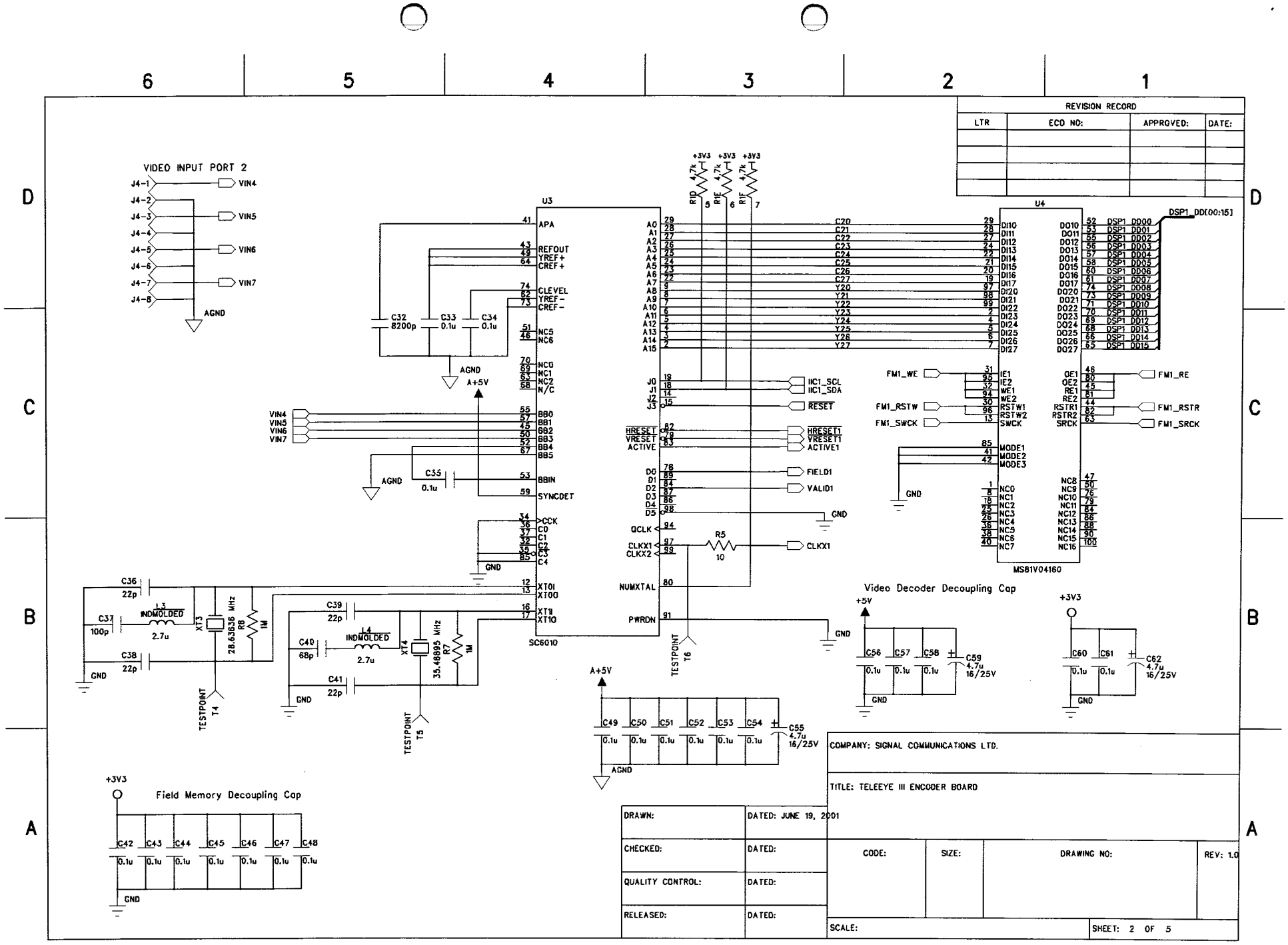
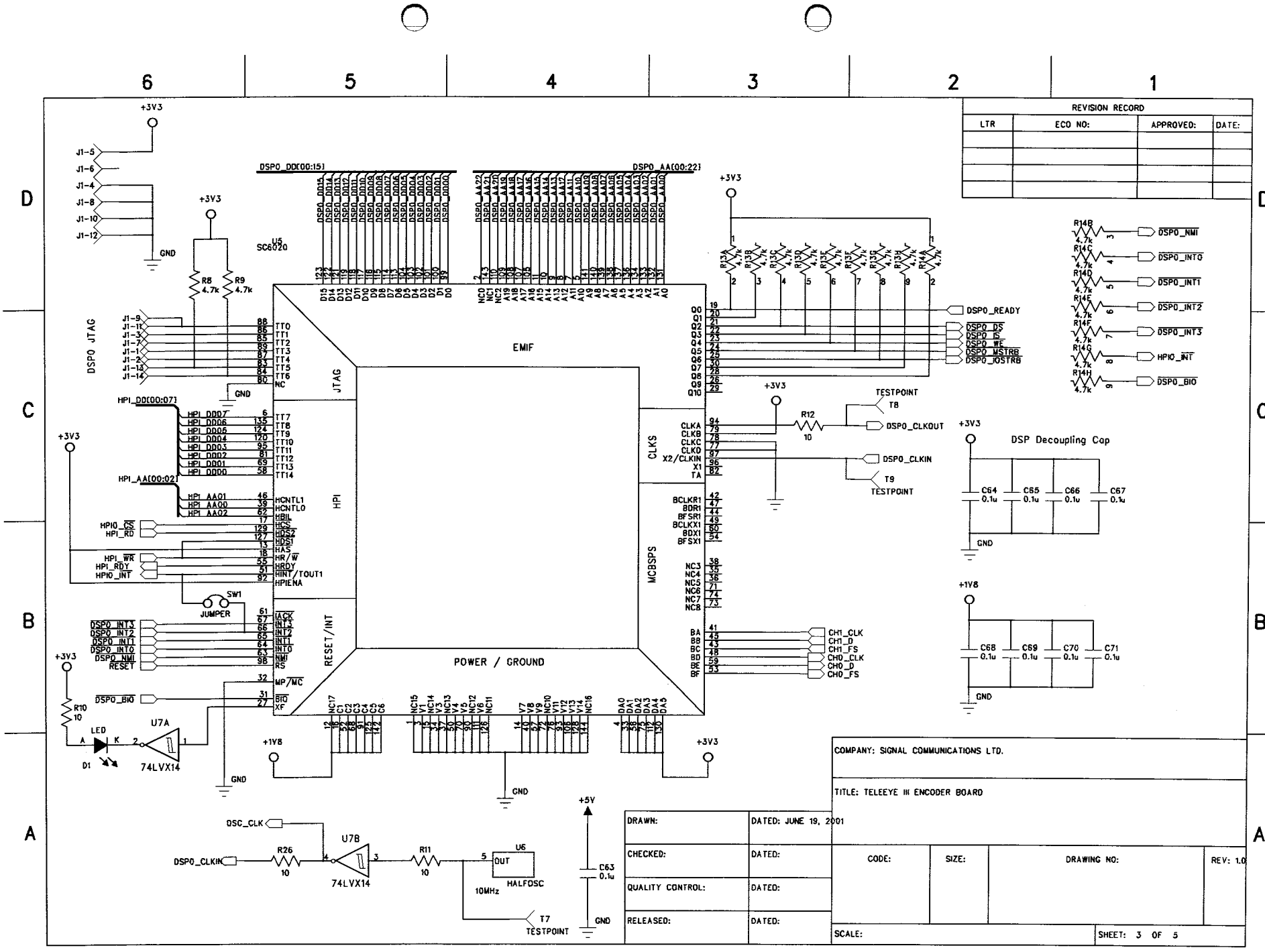
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: 8 OF 8	



app_eb.sch-1 - Sat Apr 6 12:18:49 2002

Encoder PCB Circuit Diagram


6
5
4
3
2
1
D
C
B
A
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
VIDEO INPUT PORT 2
J4-1
J4-2
J4-3
J4-4
J4-5
J4-6
J4-7
J4-8
VIN4
VIN5
VIN6
VIN7
AGND
U3
SC6010
APA
REFOUT
YREF+
CREF+
CLEVEL
YREF-
CREF-
NC5
NC6
NC0
NC1
NC2
N/C
BB0
BB1
BB2
BB3
BB4
BB5
BBIN
SYNCDET
CCK
C0
C1
C2
C3
C4
XTOI
XTOO
XTII
XTIO
NUMXTAL
PWRDN
QCLK
CLKX1
CLKX2
HRESET
VRESET
ACTIVE
D0
D1
D2
D3
D4
D5
IIC1_SCL
IIC1_SDA
RESET
HRESET1
VRESET1
ACTIVE1
FIELD1
VALID1
CLKX1
A+5V
GND
C32 8200p
C33 0.1u
C34 0.1u
C35 0.1u
C36 22p
C37 100p
C38 22p
C39 22p
C40 68p
C41 22p
L3 INDMOLDED 2.7u
L4 INDMOLDED 2.7u
XT3 28.63635 MHz
XT4 35.46895 MHz
R8 1M
R7 1M
R5 10
TESTPOINT T4
TESTPOINT T5
TESTPOINT T6
+3V3
R10 4.7k
R11 4.7k
R12 4.7k
U4
MS81V04160
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
DI10
DI11
DI12
DI13
DI14
DI15
DI16
DI17
DI20
DI21
DI22
DI23
DI24
DI25
DI26
DI27
DO10
DO11
DO12
DO13
DO14
DO15
DO16
DO17
DO20
DO21
DO22
DO23
DO24
DO25
DO26
DO27
DSP1_DD[00:15]
FM1_WE
FM1_RSTW
FM1_SWCK
FM1_RE
FM1_RSTR
FM1_SRCK
MODE1
MODE2
MODE3
Video Decoder Decoupling Cap
C56 0.1u
C57 0.1u
C58 0.1u
C59 4.7u 16/25V
C60 0.1u
C61 0.1u
C62 4.7u 16/25V
C49 0.1u
C50 0.1u
C51 0.1u
C52 0.1u
C53 0.1u
C54 0.1u
C55 4.7u 16/25V
Field Memory Decoupling Cap
C42 0.1u
C43 0.1u
C44 0.1u
C45 0.1u
C46 0.1u
C47 0.1u
C48 0.1u
COMPANY: SIGNAL COMMUNICATIONS LTD.
TITLE: TELEEYE III ENCODER BOARD
DRAWN:
DATED: JUNE 19, 2001
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV: 1.0
SCALE:
SHEET: 2 OF 5



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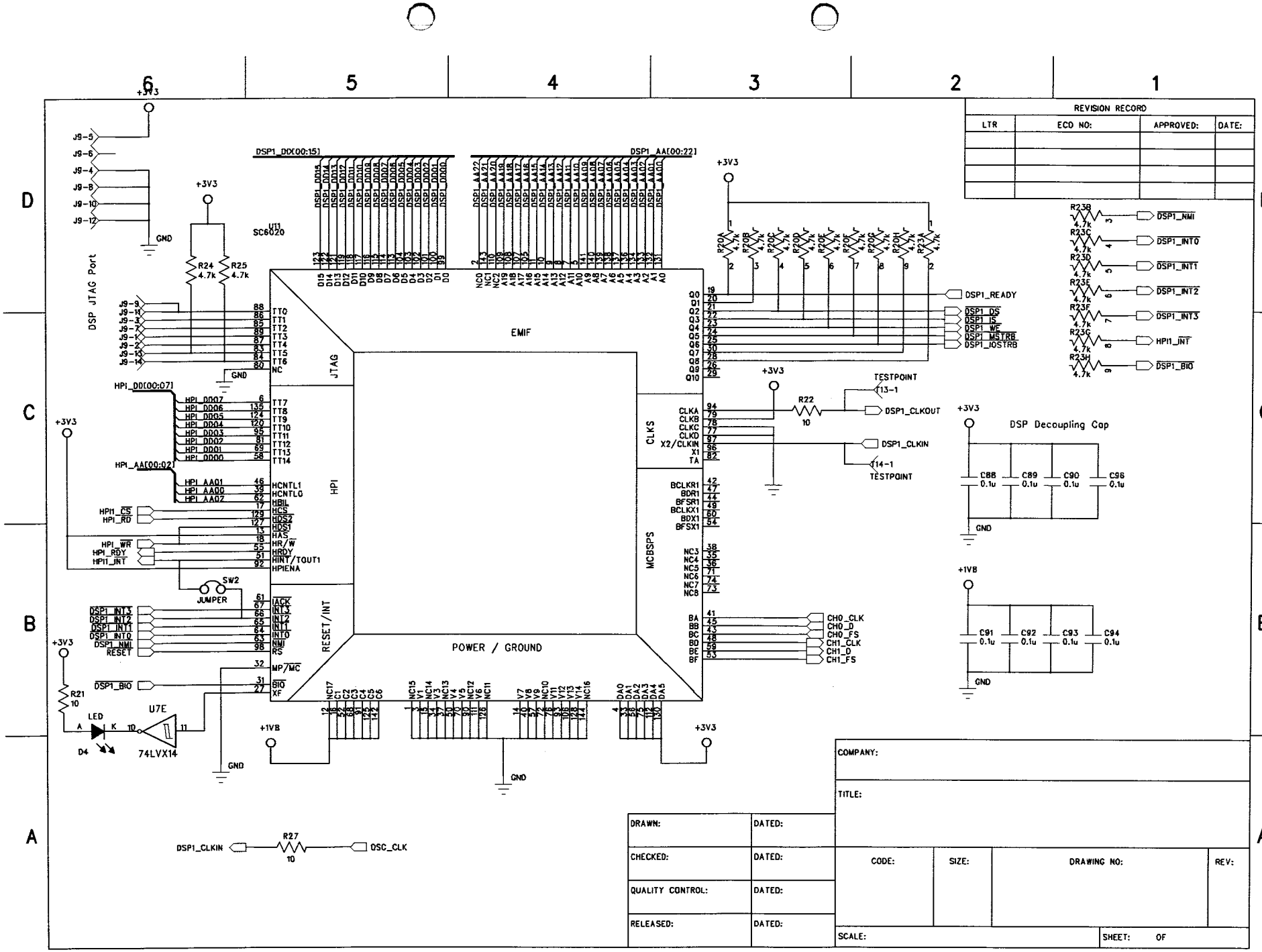

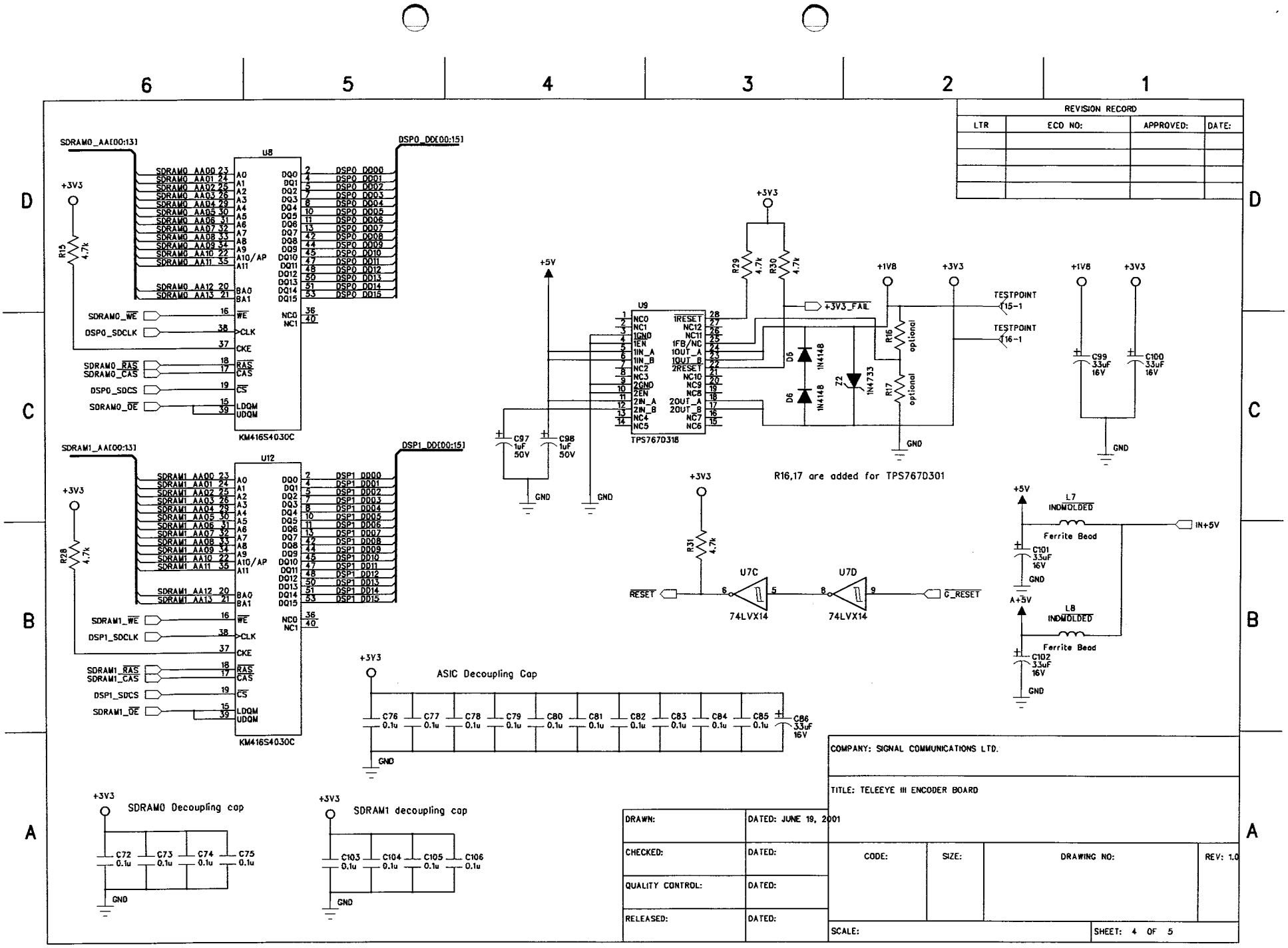

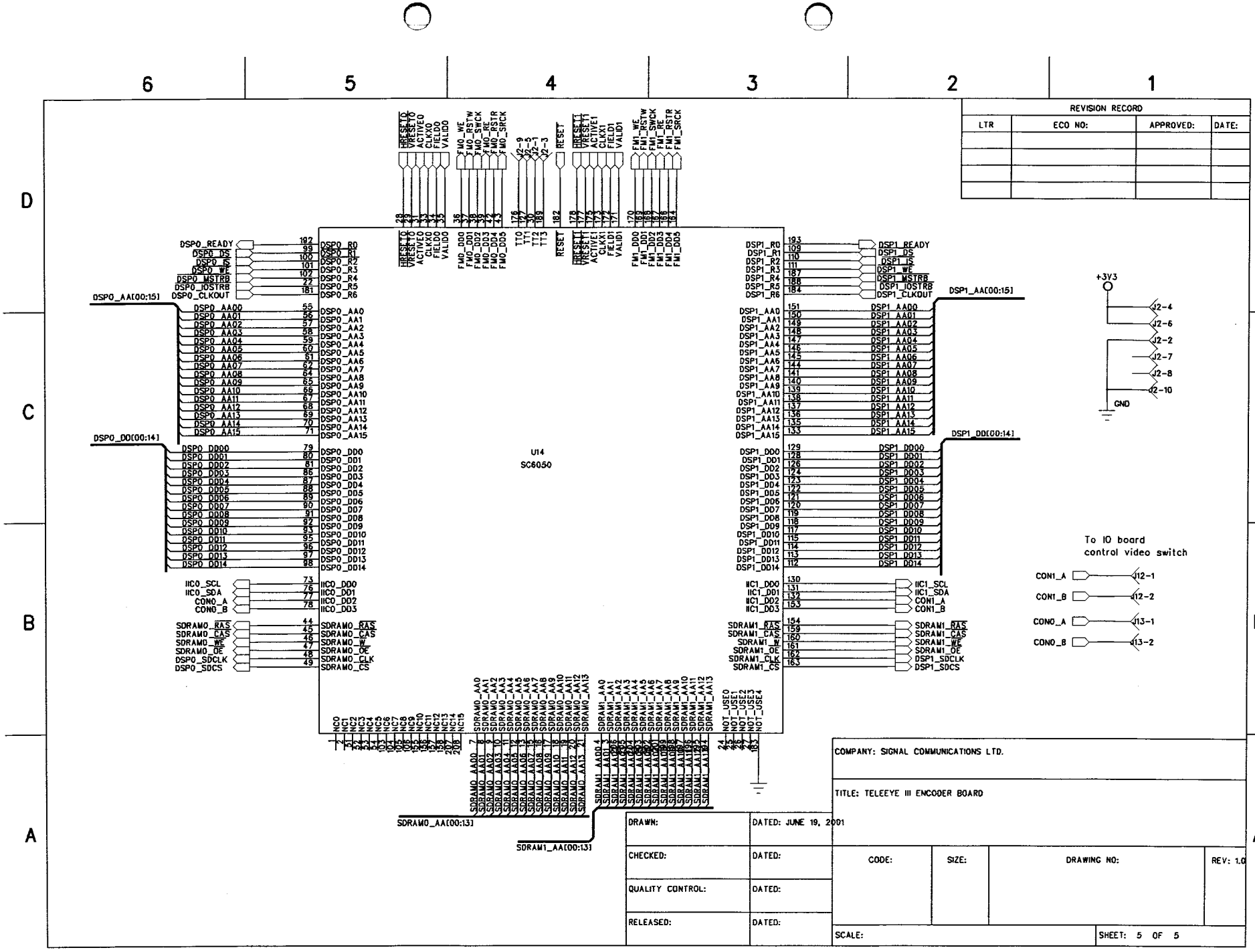

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