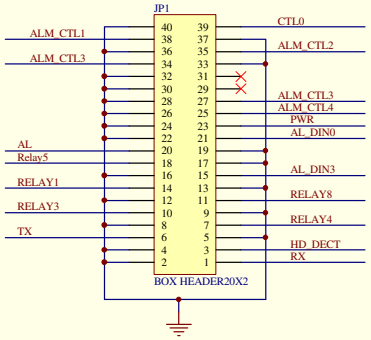
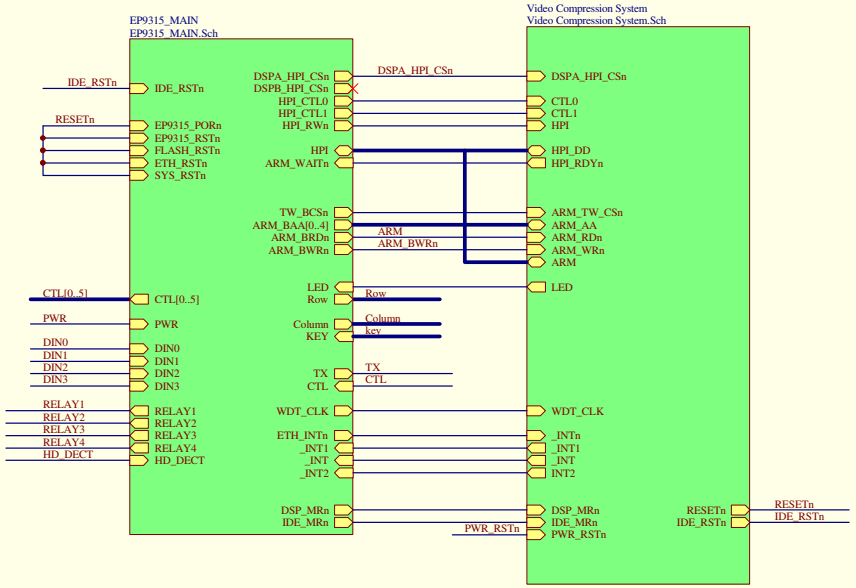
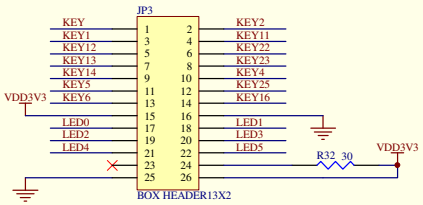
Power board connector



RX 4 channel main board top



Panel board connector



Title	RDVR 8 channel system		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:09	Sheet 1 of 33	
File: RDVR_4ch_TOP.Sch			

Signal Communications Limited
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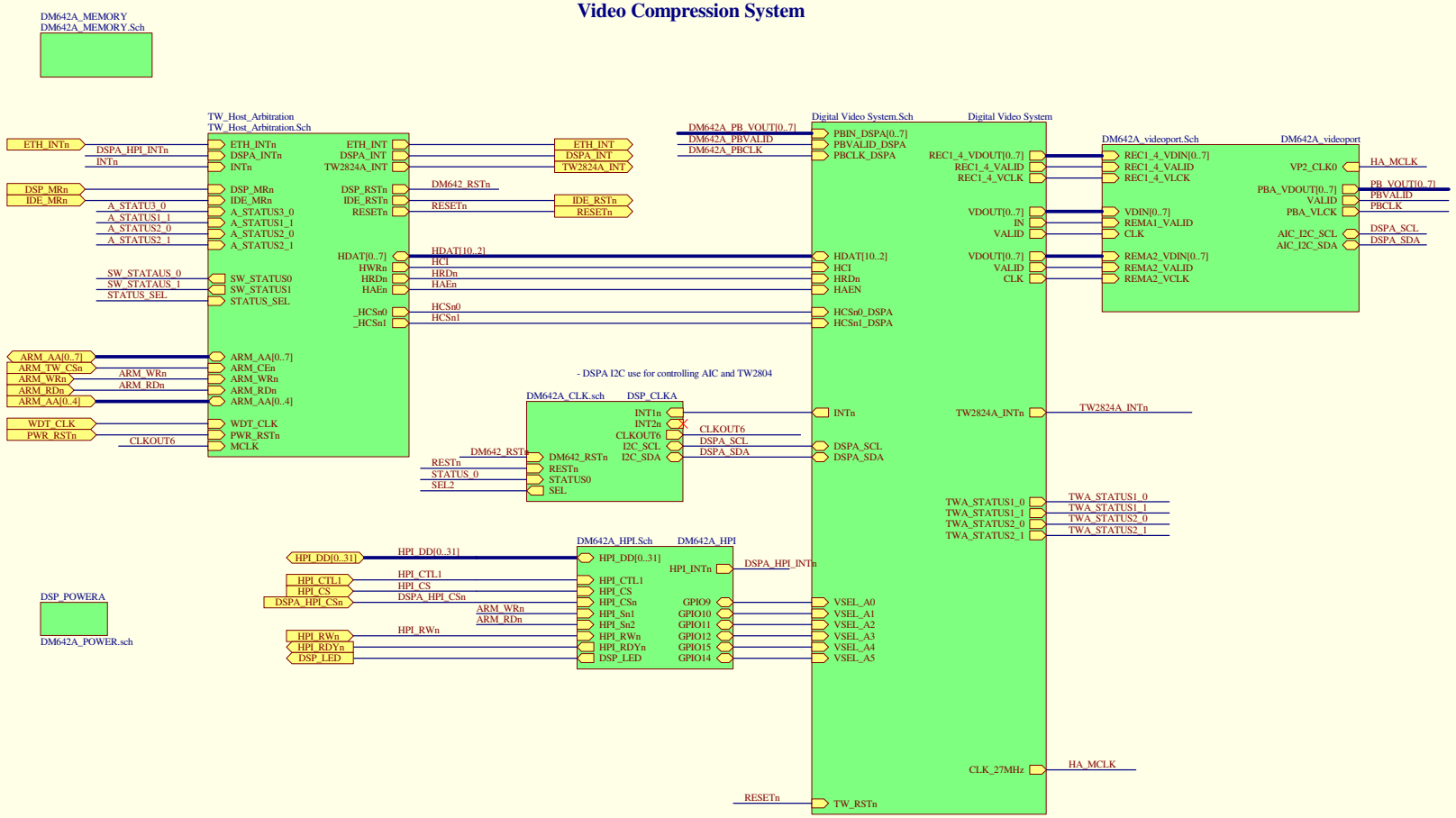
370 Kwun Tong Road,
Kowloon, Hong Kong

Video Compression System



Title	Video Compression System		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:09	Sheet 2 of 33	
File: Video Compression System.Sch			

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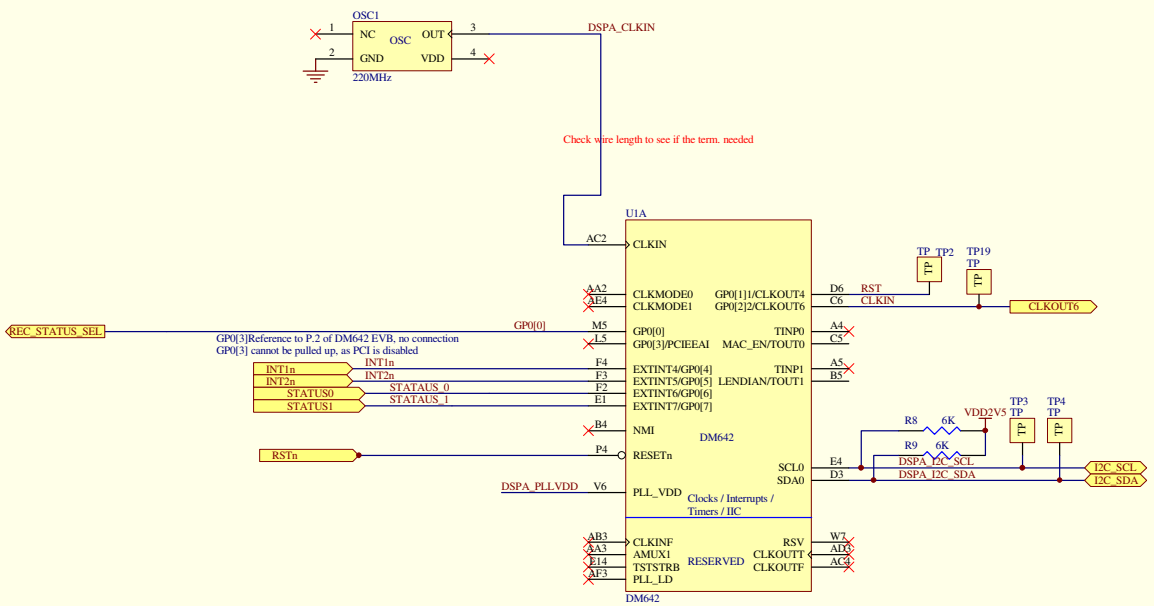
DM642A Clock & Interrupt System



Title	DM642A Clock, Interrupts and Resets		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:09	Sheet 3 of 33	
File: DM642A_CLK.Sch 5			

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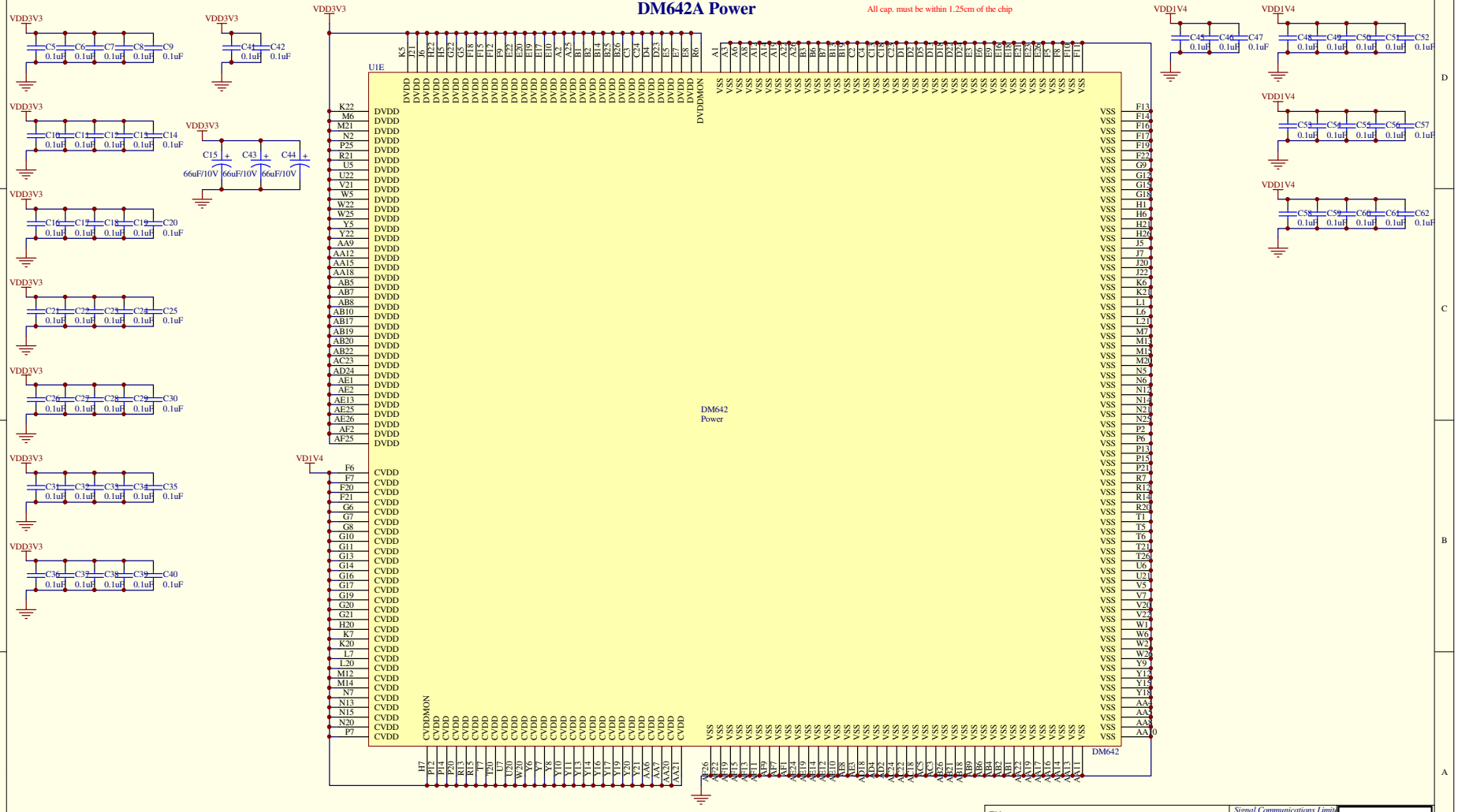
DM642A Power

All cap. must be within 1.25cm of the chip



Title	DM642A Power		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:10	Sheet 4 of 33	
File: DM642A_POWER.sch			

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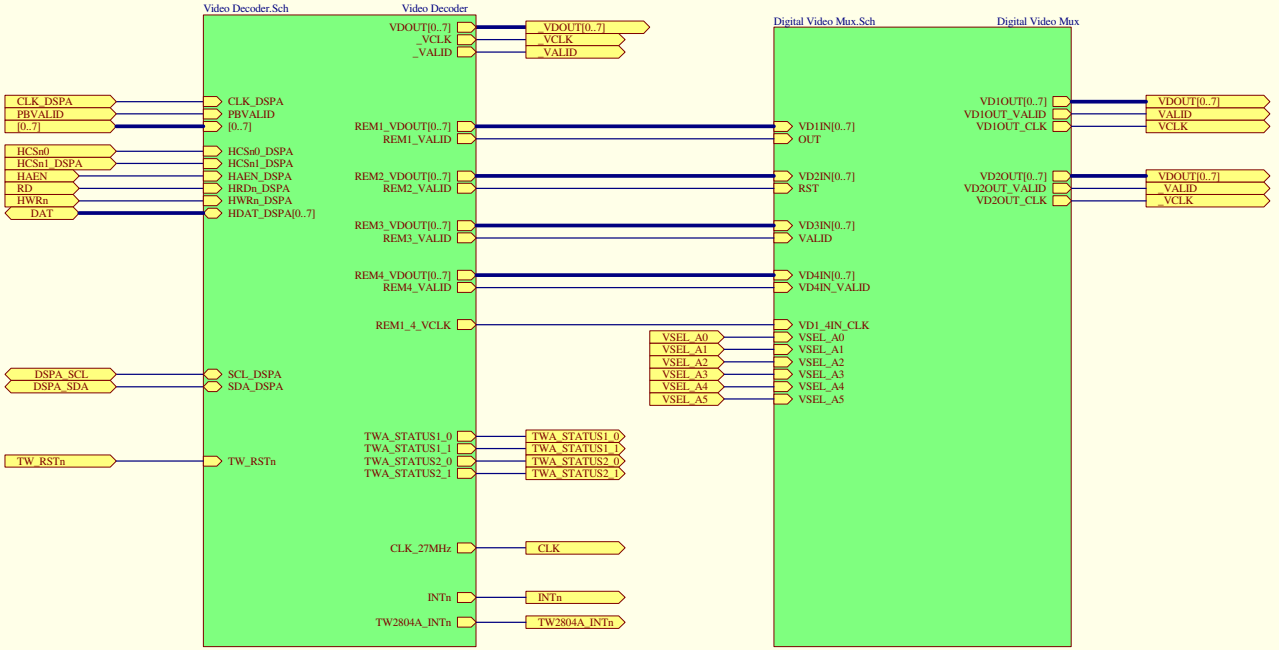
Digital Video System



Title	Digital Video System		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:10	Sheet 5 of 33	
File: Digital Video System5.Sch			

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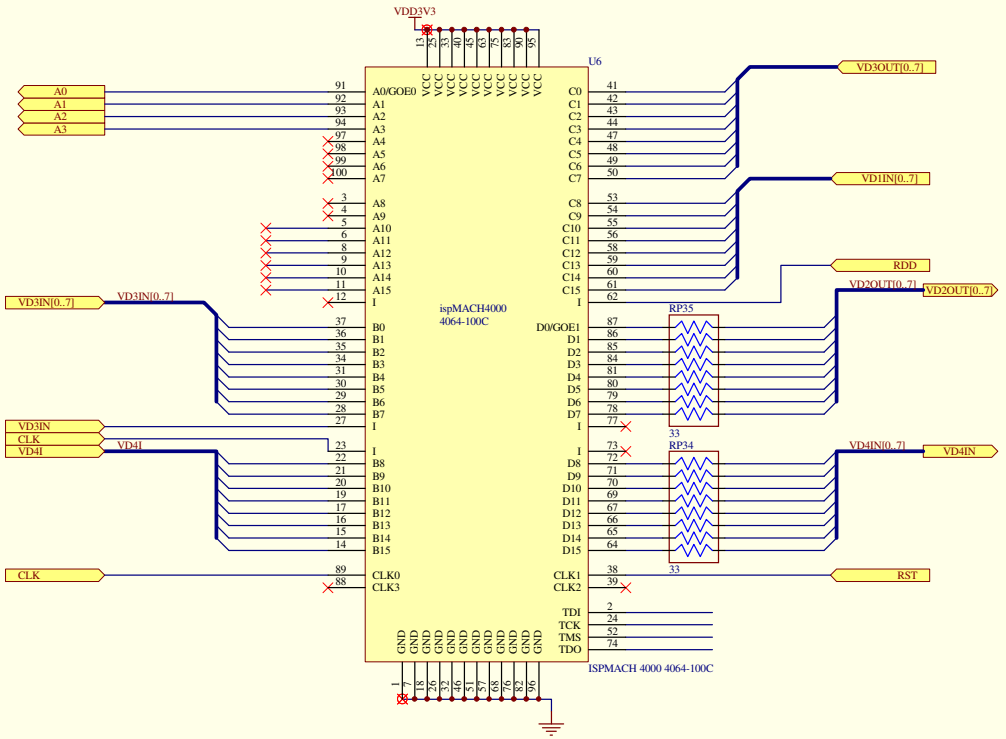
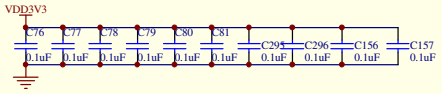
Digital Video MUX CPLD





Title: Digital Video Multiplexer			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005 Time: 09:29:10	Sheet 6 of 33		
File: Digital Video Mux.SCh			

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Video Decoder

- VGND and GND tie together
GND

CONN1
VIDEO_IN_1
VIDEO_IN_2
VIDEO_IN_3
VIDEO_IN_4
CONN_BNC4X2_HF-801-1

Analog Video Input
Analog Video Input.Sch
VIDEO_IN_1 — Video1_In — VideoOut_1A / VideoOut_1B — VideoIn_1A / VideoIn_1B
VIDEO_IN_2 — Video2_In — VideoOut_2A / VideoOut_2B — VideoIn_2A / VideoIn_2B
VIDEO_IN_3 — Video3_In — VideoOut_3A / VideoOut_3B — VideoIn_3A / VideoIn_3B
VIDEO_IN_4 — Video4_In — VideoOut_4A / VideoOut_4B — VideoIn_4A / VideoIn_4B

TW2824A_SDRAM_IF
TW2824A_SDRAM_IF.sch

TW2824A_MAIN.SCH — TW2824_0
HCSn0_DSPA
HCSn1_DSPA
HAEN_DSPA
HRDn_DSPA
HWRn_DSPA
HDAT_DSPA[0..7]
TW2824_HCSn0
TW2824_HCSn1
TW2824_HAEN
TW2824_HRDn
TW2824_HWRn
TW2824_HDAT[0..7]
VAOUTYX
VAOUTCX
TW2824_INTn → TW2824A_INTn
VideoOut_1A
VideoOut_2A
VideoOut_3A
VideoOut_4A
TW2824_VIN1
TW2824_VIN2
TW2824_VIN3
TW2824_VIN4
VDOUTY[0..7] → REC1_4_VDOUT[0..7]
VDOUTY_CLK → REC1_4_VCLK
VDOUTX_CLK → CLK_27MHz
VCLK
Rem_DSPA
VALID_DSPA
A[0..7]
CLK
DATA
ADD
PBCLK
PBVALID
PBIN[0..7]
MPPDEC0_0 — DEBUG00
MPPDEC1_0 — TWA_DEBUG10
MPPDEC2_0 — TWA_DEBUG20
MPPDEC3_0 — TWA_DEBUG30
TW_RSTn
TW2824_RSTn
MPPDEC0_1 — TWA_DEBUG01
MPPDEC1_1 — TWA_DEBUG11
MPPDEC2_1 — TWA_DEBUG21
MPPDEC3_1 — RST

Analog Video Output.sch — Analog Video Output
VAIN_Y — VOUT_CVBS
- analog video is output to the monitor
- the digital output have no use
VOUT_CVBS
VDD3V3
R33 500
CONN2
CONN_BNC1X2_HF-201-1
R36 0 NOP
TWA_STATUS1_2
TWA_STATUS2_3
REC1_4_VALID
TWA_STATUS1_1
TWA_STATUS2_1

JP4
TWA_DEBUG00 — TWA_DEBUG01
TWA_DEBUG10 — TWA_DEBUG11
TWA_DEBUG20 — TWA_DEBUG21
TWA_DEBUG30 — TWA_DEBUG31
HEADER5X2

TW2804A_MAIN.SCH — TW2804_MUX0
TW2804_RSTn
VideoIn_1B
VideoIn_2B
VideoIn_3B
VideoIn_4B
TW2804_VIN1
TW2804_VIN2
TW2804_VIN3
TW2804_VIN4
SCL_DSPA
SDA_DSPA
SCL
SDA
I2C_ADDR1
I2C_ADDR0
VALID1 — VD1OUT[0..7] → REM1_VALID / VD1
VALID2 — VD2OUT[0..7] → REM2_VALID / VD2
VALID3 — VD3OUT[0..7] → REM3_VALID / VD3
VALID4 — VD4OUT[0..7] → REM4_VALID / VD4
VDOUT_CLK → REM1_4_VCLK
TW2804_INTn → VD5

Title: Video Decoder & Encoder			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:10	Sheet 7 of 33	
File: Video Decoder.Sch 5			

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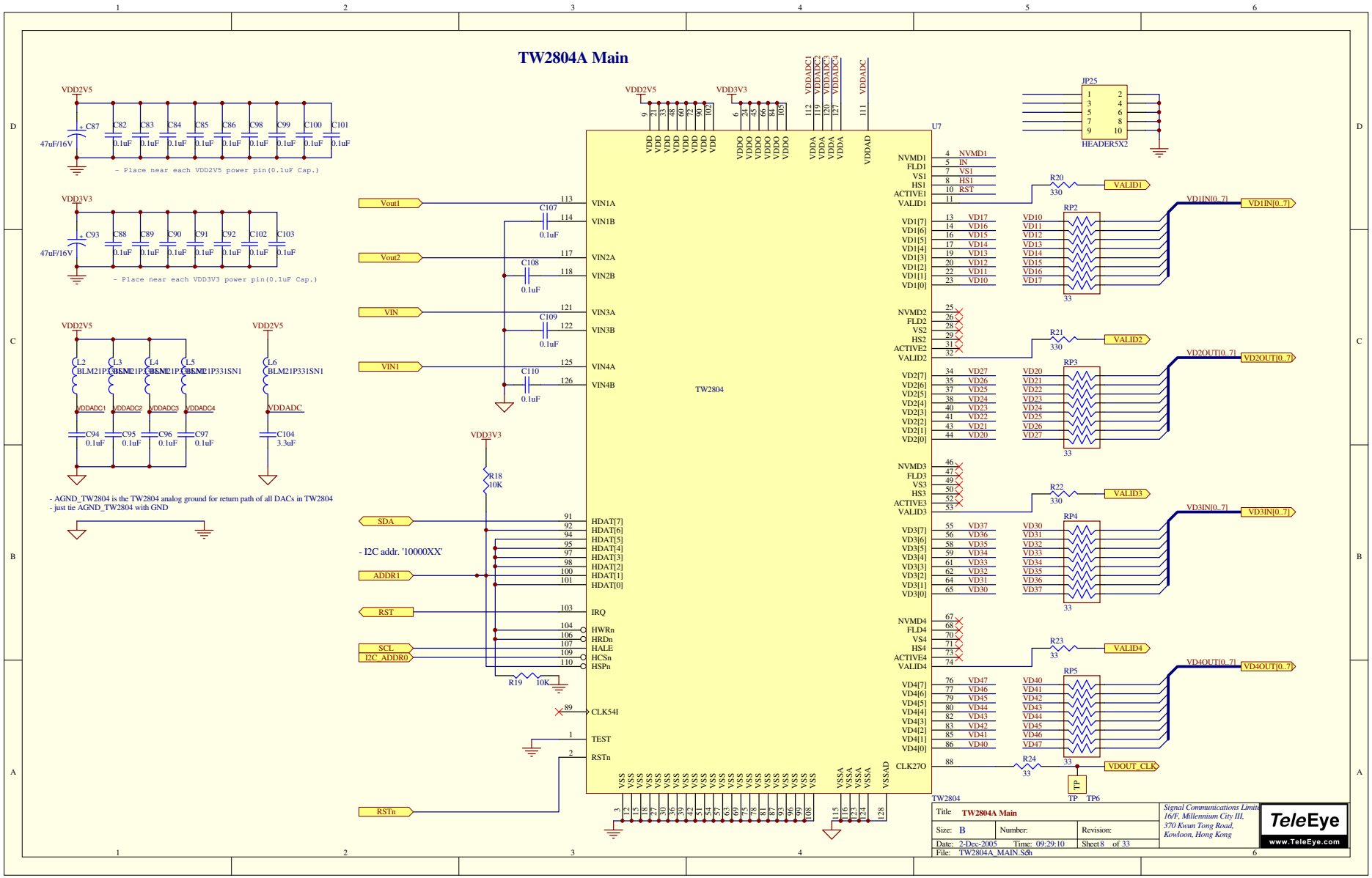
TW2804A Main
VDD2V5
VDD3V3
C87
47uF/16V
C82
C83
C84
C85
C86
C98
C99
C100
C101
0.1uF
- Place near each VDD2V5 power pin(0.1uF Cap.)
C93
C88
C89
C90
C91
C92
C102
C103
- Place near each VDD3V3 power pin(0.1uF Cap.)
L2
L3
L4
L5
L6
BLM21P331SN1
VDDADC1
VDDADC2
VDDADC3
VDDADC4
VDDADC
C94
C95
C96
C97
C104
3.3uF
- AGND_TW2804 is the TW2804 analog ground for return path of all DACs in TW2804
- just tie AGND_TW2804 with GND
TW2804
U7
Vout1
Vout2
VIN
VIN1
VIN1A
VIN1B
VIN2A
VIN2B
VIN3A
VIN3B
VIN4A
VIN4B
C107
C108
C109
C110
R18
10K
SDA
ADDR1
RST
SCL
I2C_ADDR0
- I2C addr. '10000XX'
HDAT[7]
HDAT[6]
HDAT[5]
HDAT[4]
HDAT[3]
HDAT[2]
HDAT[1]
HDAT[0]
IRQ
HWRn
HRDn
HALE
HCSn
HSPn
R19
CLK54I
TEST
RSTn
CLK27O
JP25
HEADER5X2
R20
R21
R22
R23
R24
330
VALID1
VALID2
VALID3
VALID4
VDOUT_CLK
RP2
RP3
RP4
RP5
VD1IN[0..7]
VD2OUT[0..7]
VD3IN[0..7]
VD4OUT[0..7]
TP
TP6
Title TW2804A Main
Size: B
Number:
Revision:
Date: 2-Dec-2005
Time: 09:29:10
Sheet 8 of 33
File: TW2804A_MAIN.SCH
Signal Communications Limited
16/F, Millennium City III,
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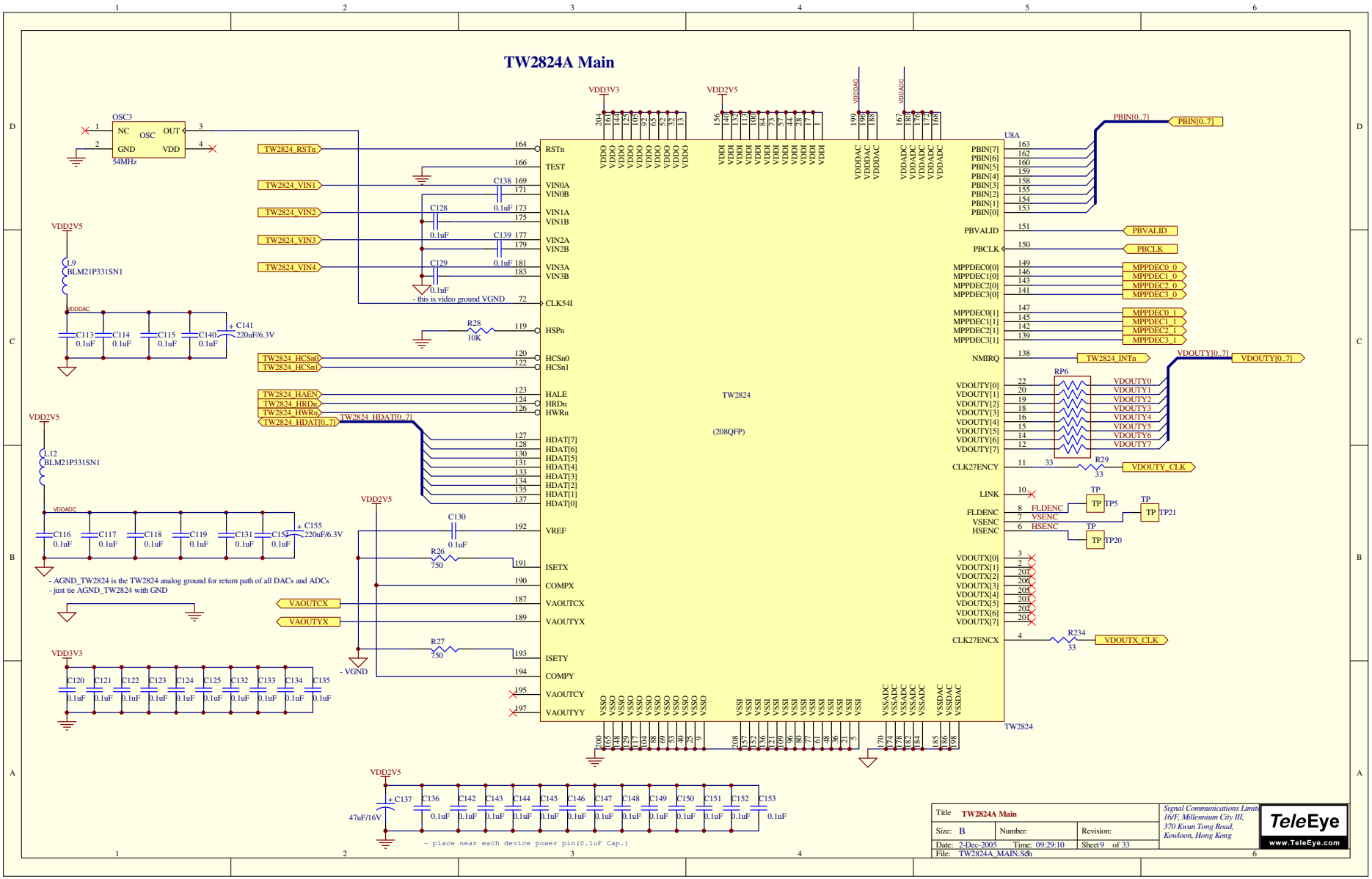
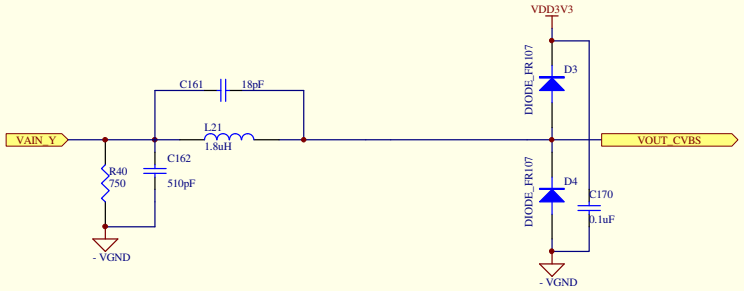
Kowloon, Hong Kong
TeleEye
www.TeleEye.com

TW2824A Main



Analog Video Output



Title: Analog Video Output			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005 Time: 09:29:10	Sheet 10 of 33		
File: Analog Video Output.SchDoc			

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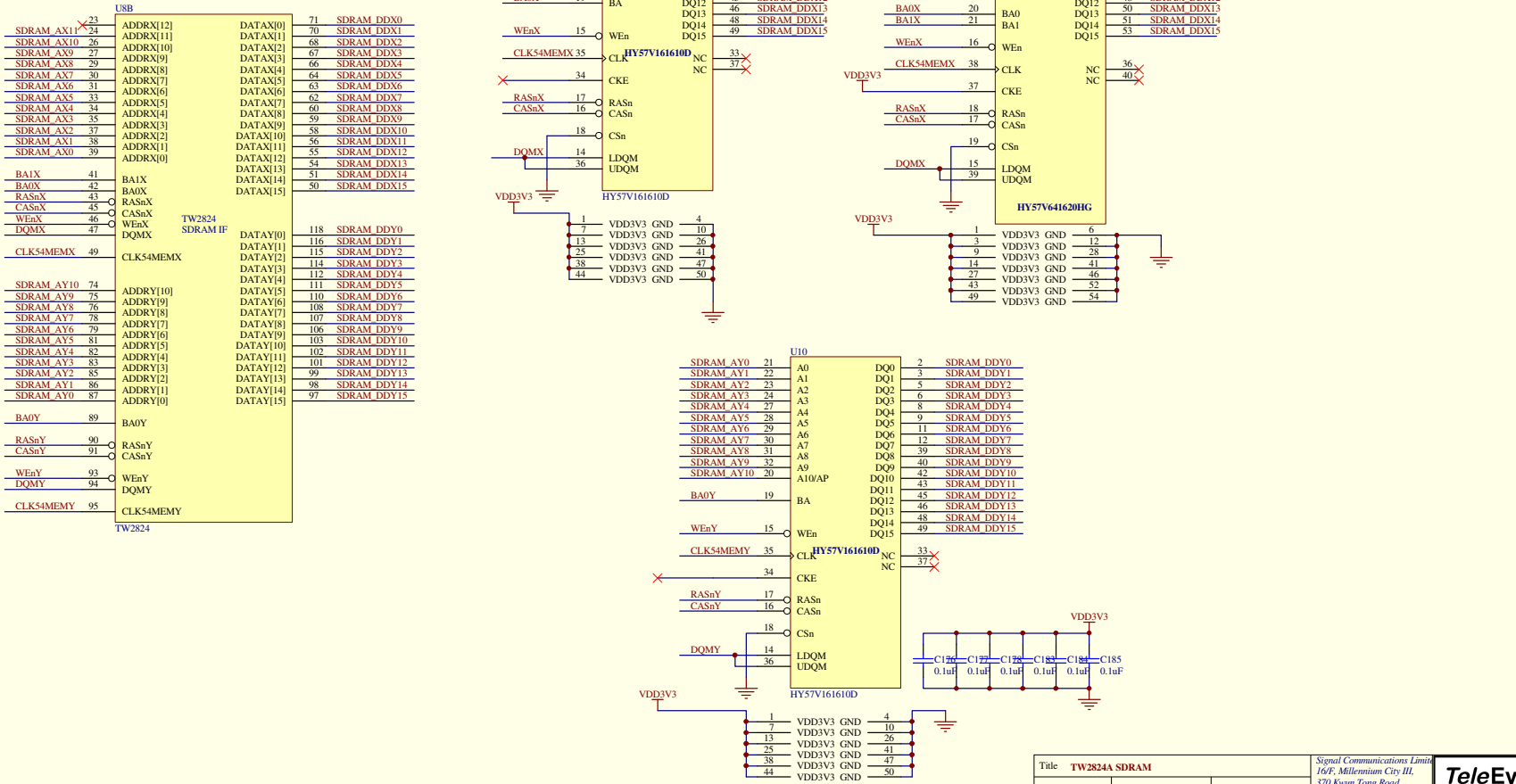
TW2824A SDRam I/F



Title	TW2824A SDRAM		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:10	Sheet 11 of 33	
File: TW2824A_SDRAM5IF.Sch			

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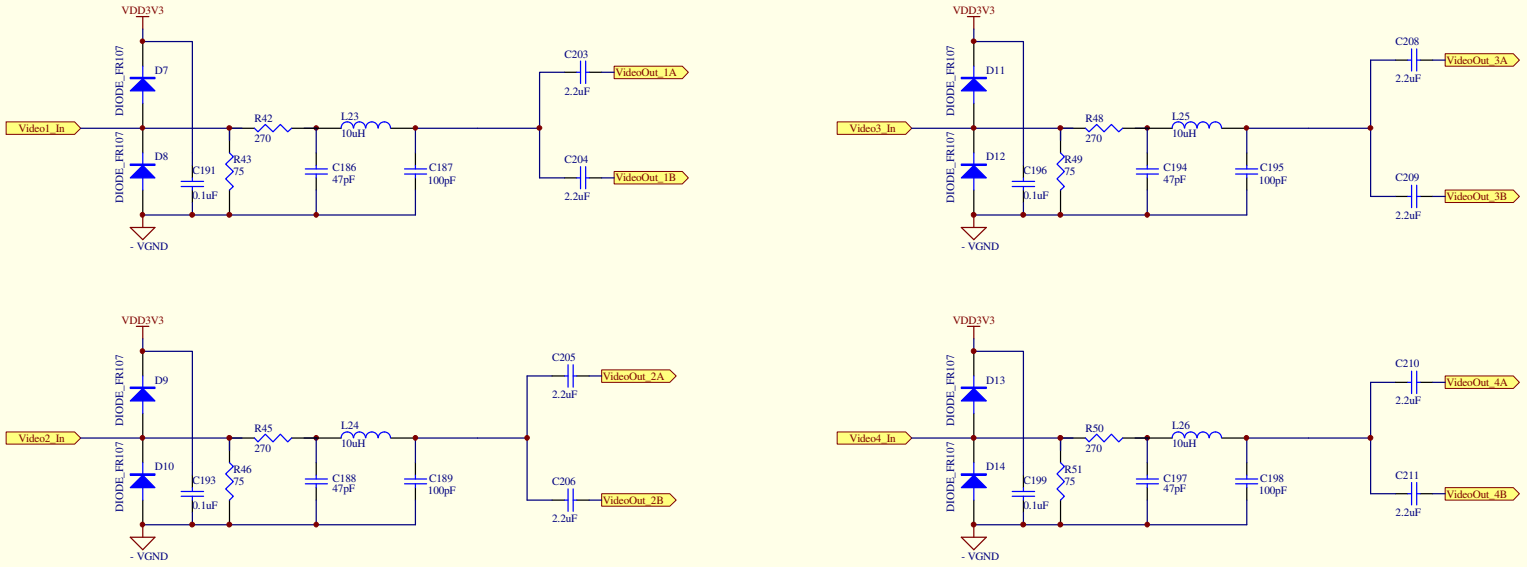
Kowloon, Hong Kong

Analog Video Input



Title	Analog Video Input		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:10	Sheet 12 of 33	
File: Analog Video Input.SchDoc			

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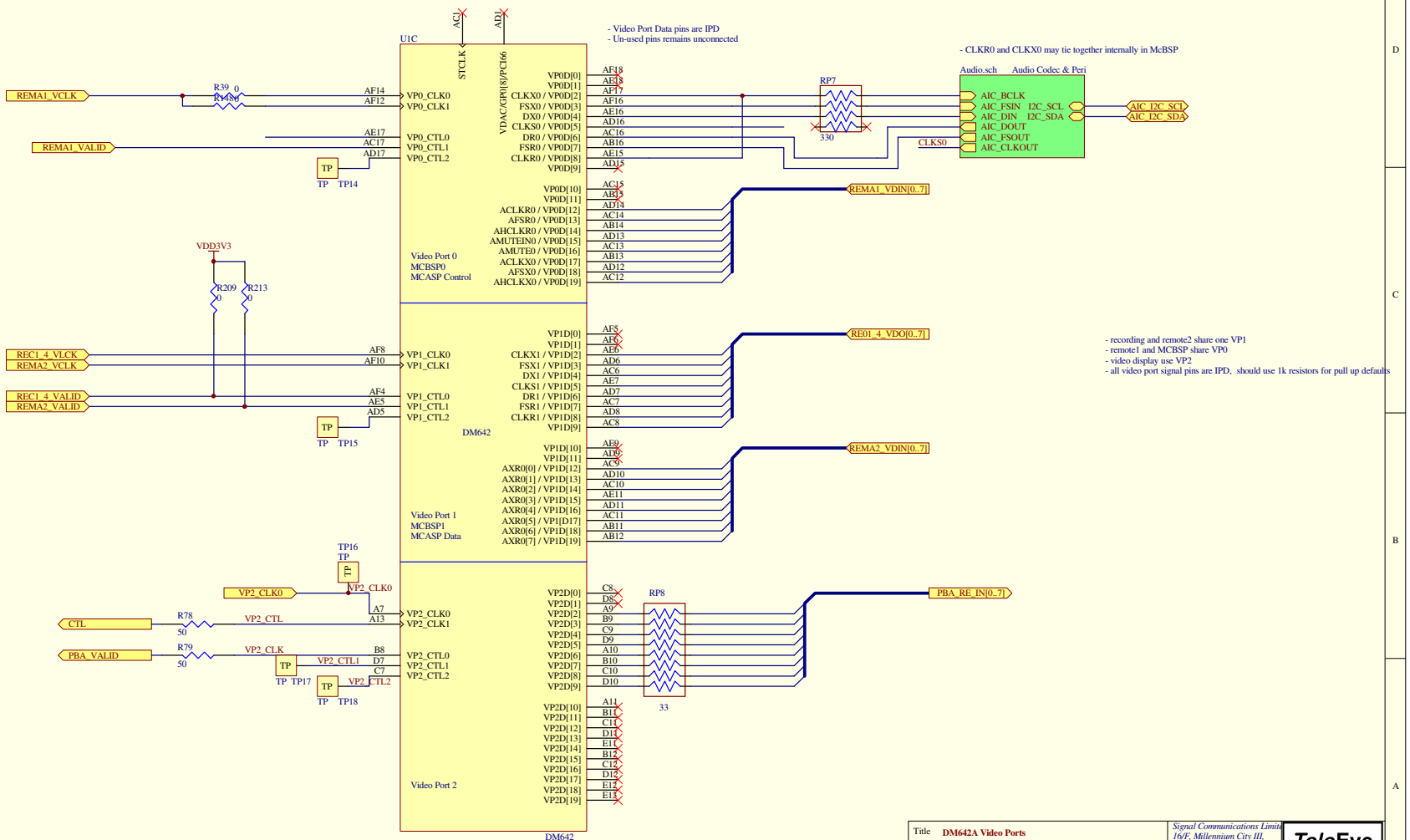
DM642A Video Port



Title	DM642A Video Ports		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:11	Sheet 14 of 33	
File: DM642A_videoport.Sch			

Signal Communications Limited
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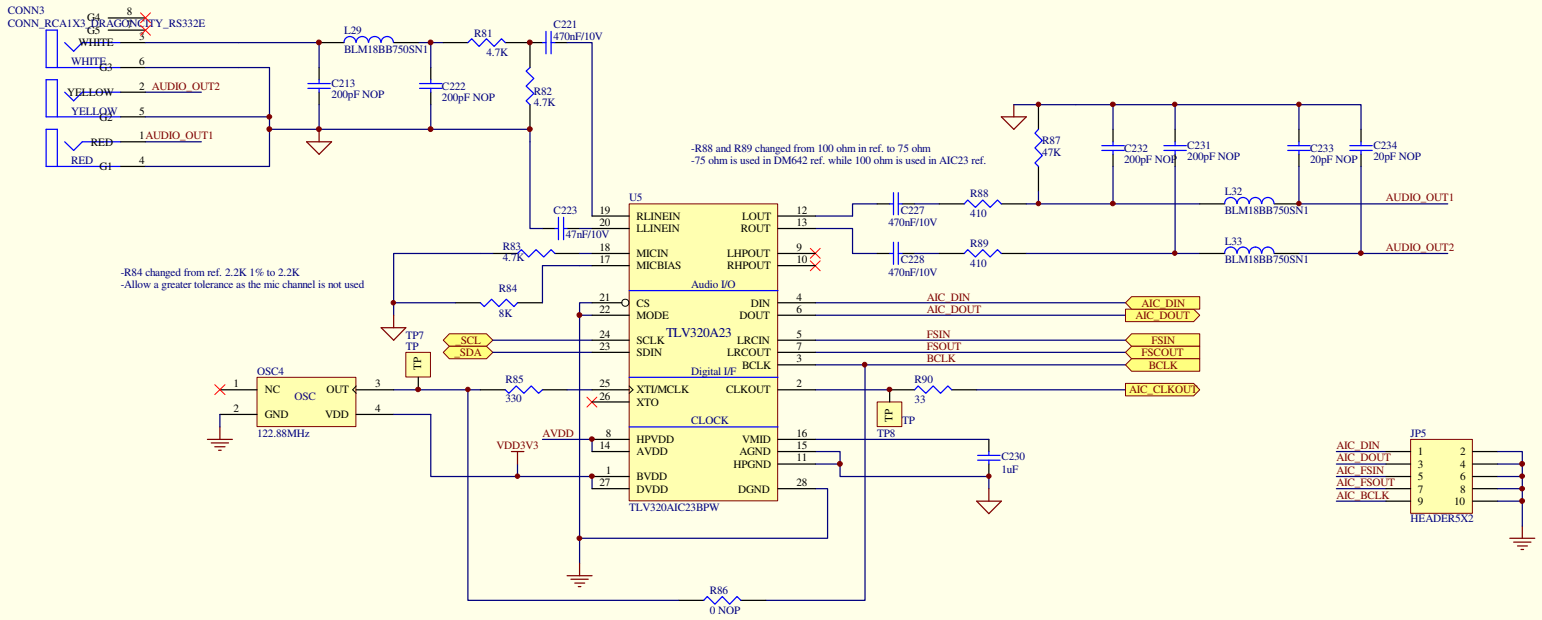
Kowloon, Hong Kong

Audio System



Title: Audio Codec			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:11	Sheet 15 of 33	
File: Audio.Sch			

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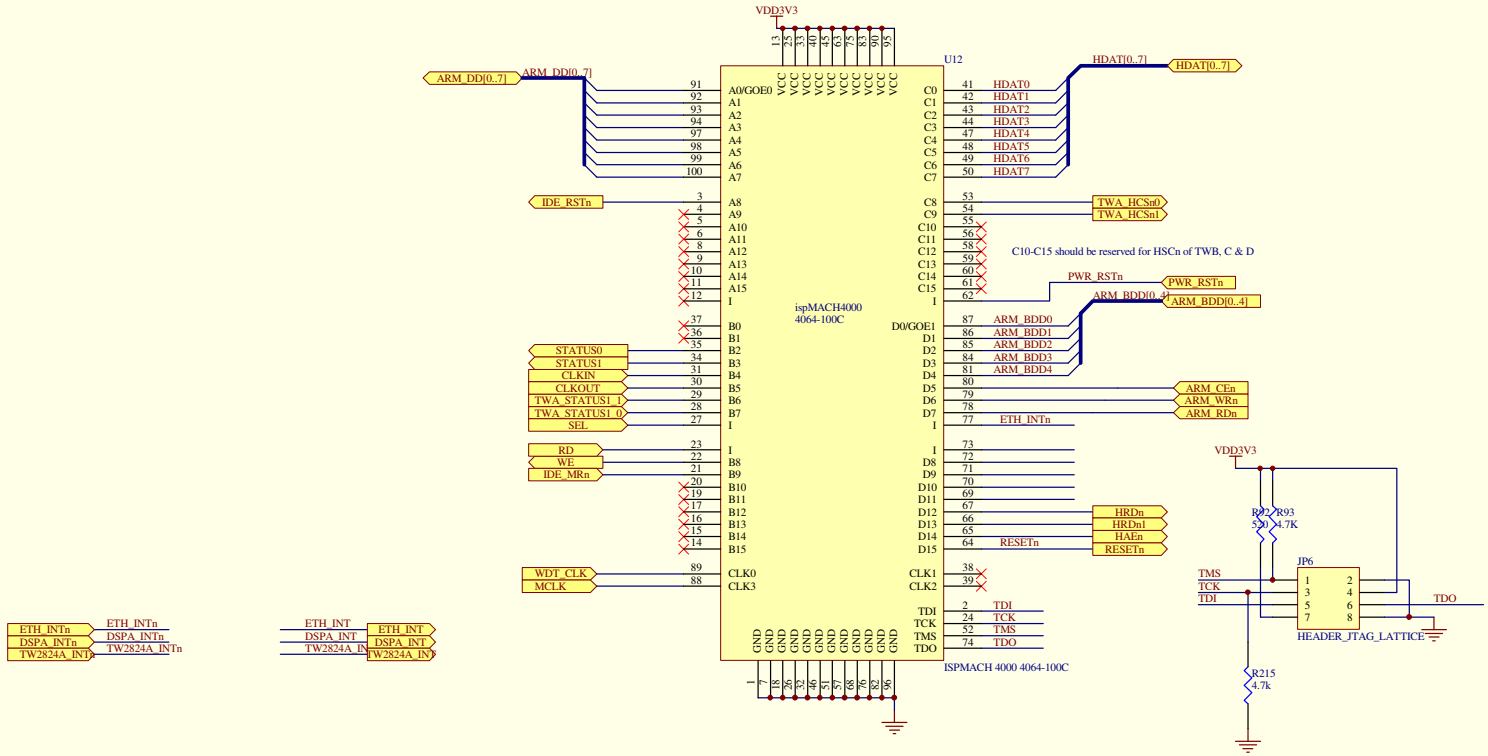
Techwell 2824 host arbitration



Title	**Video Decoder Host Port Controller**		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:11	Sheet 16 of 33	
File: TW_Host_Arbitration.Sch			

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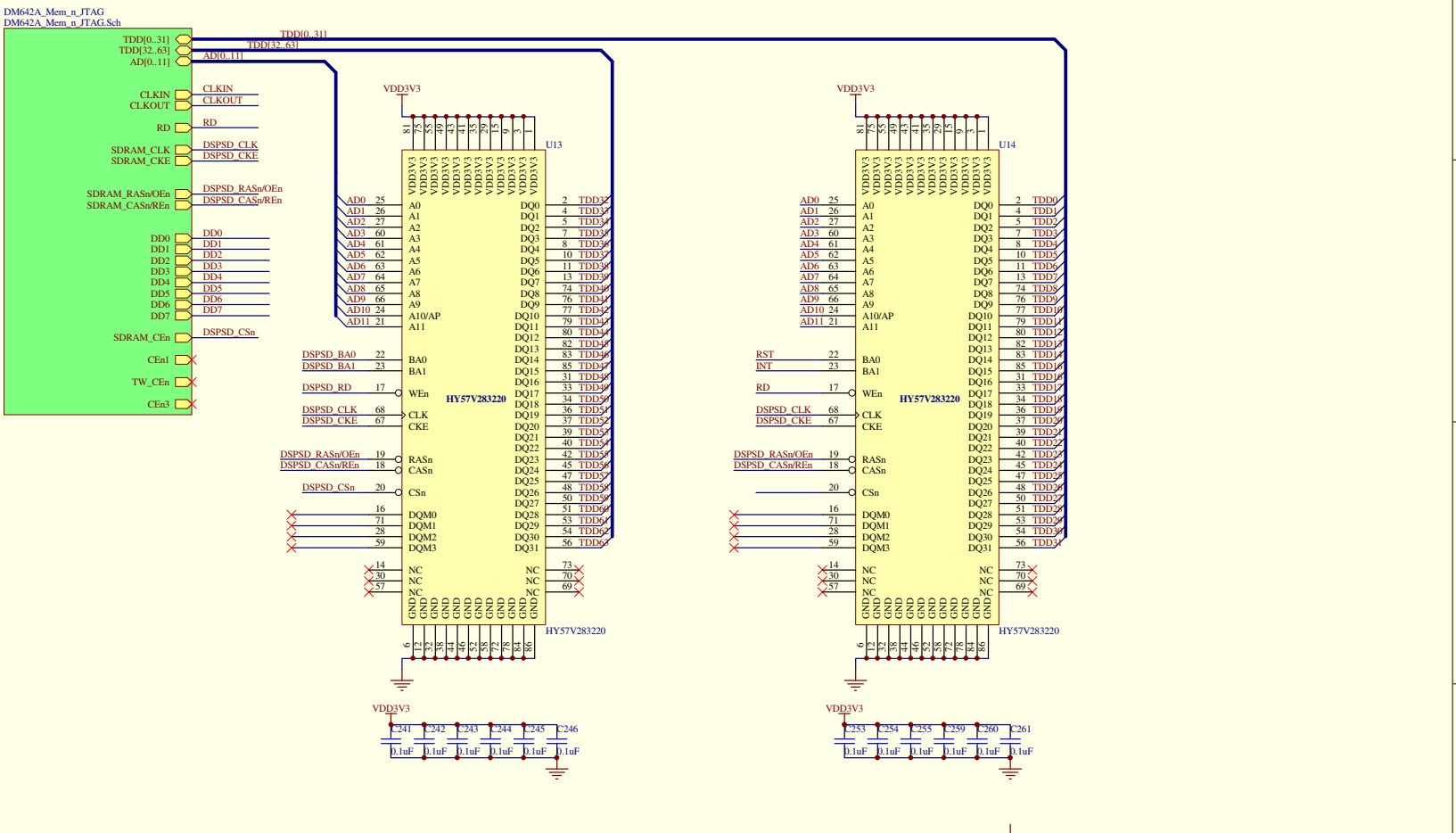
Kowloon, Hong Kong

DM642A SDRam



Title	DM642A Memory		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:11	Sheet 17 of 33	
File: DM642A_MEMORY.Sch			

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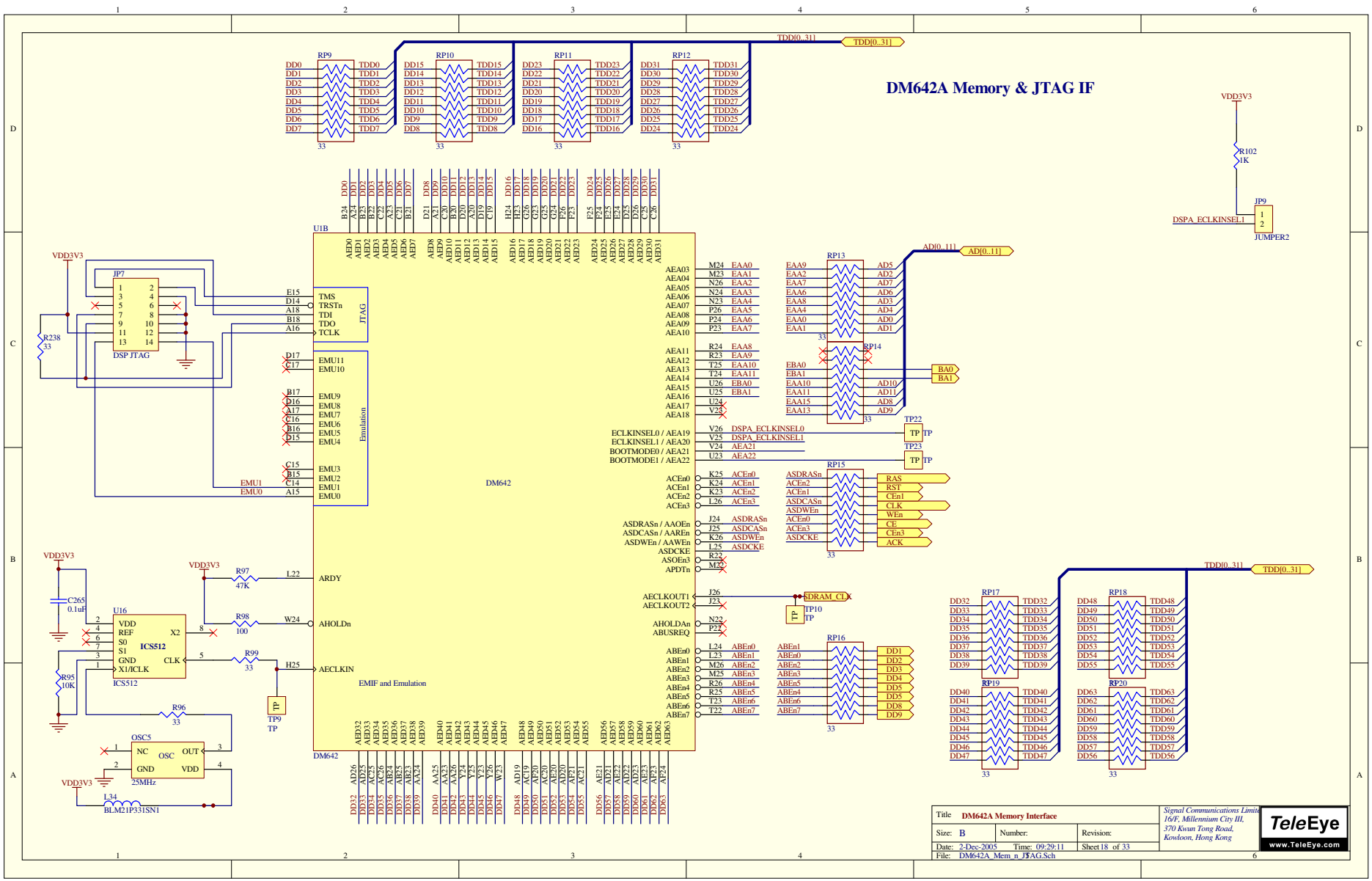
DM642A Memory & JTAG IF
DM642
U1B
JTAG
Emulation
EMIF and Emulation
DSP JTAG
JP7
JP9
JUMPER2
DSPA_ECLKINSEL1
R102
1K
R238
33
U16
ICS512
C265
0.1uF
R95
10K
R96
33
R97
47K
R98
100
R99
33
OSC5
25MHz
L34
BLM21P331SN1
TP9
TP10
TP22
TP23
RP9
RP10
RP11
RP12
RP13
RP14
RP15
RP16
RP17
RP18
RP19
RP20
TDD[0..31]
AD[0..11]
EDRAM_CLK
ARDY
AHOLDn
AECLKIN
RAS
RST
CEn1
CLK
WEn
CE
CEn3
ACK
BA0
BA1
Title DM642A Memory Interface
Size: B
Number:
Revision:
Date: 2-Dec-2005 Time: 09:29:11 Sheet 18 of 33
File: DM642A_Mem_n_JTAG.Sch
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TeleEye
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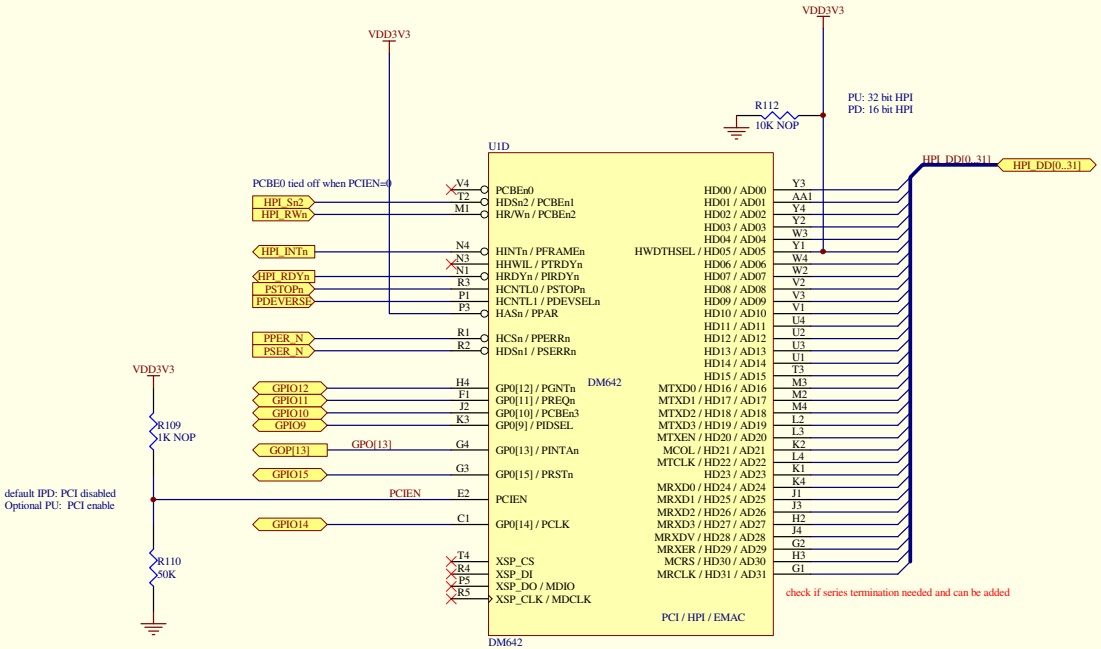
DM642A HPI IF



Title: DM642A HPI			*Signal Communications Limited* *16/F, Millennium City III,* *370 Kwun Tong Road,* *Kowloon, Hong Kong*
Size: B	Number:	Revision:	
Date: 2-Dec-2005 Time: 09:29:11	Sheet 19 of 33		
File: DM642A_HPI.Sch 5			

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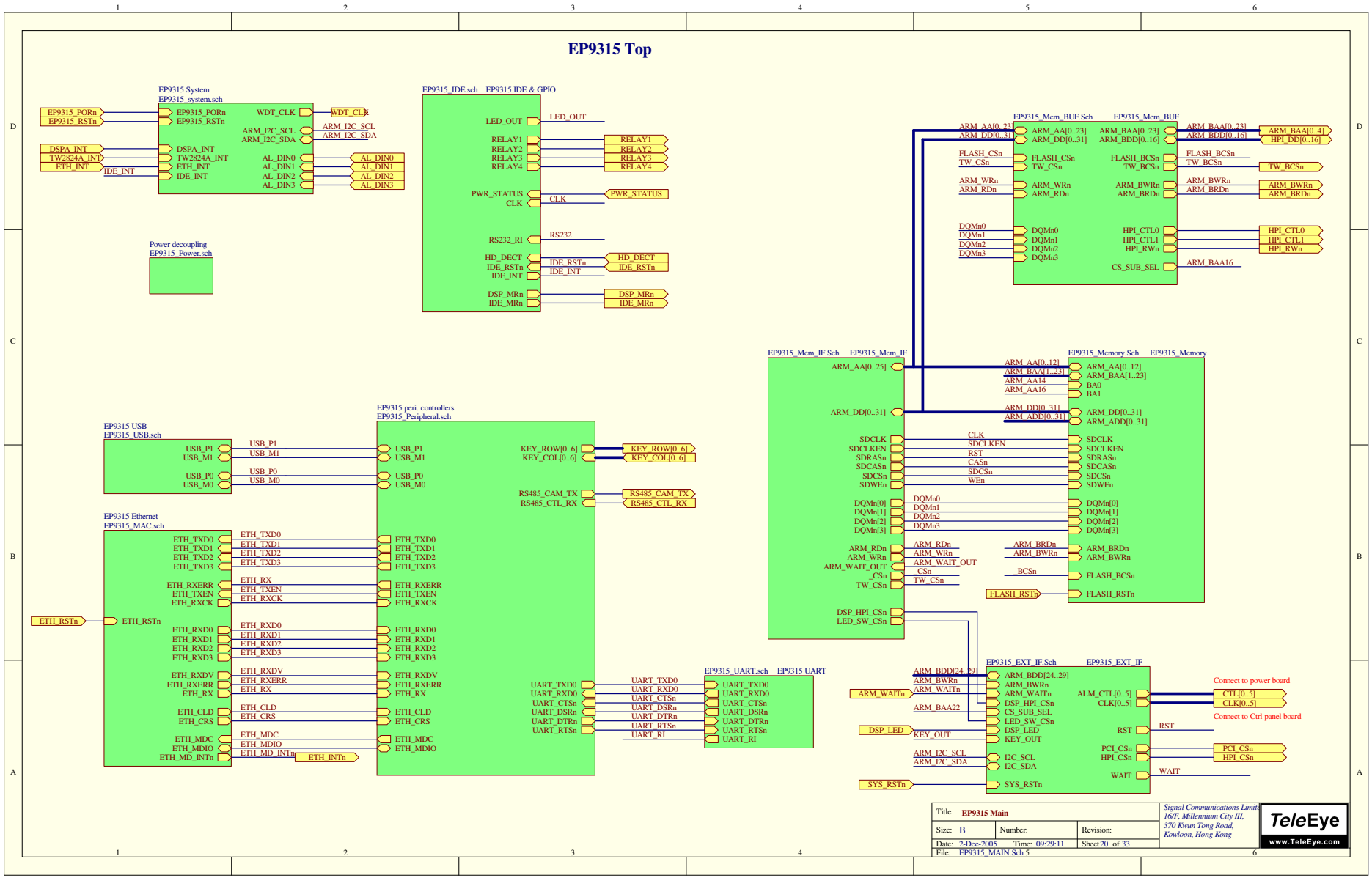
EP9315 Top



Title	EP9315 Main		
Size:	B	Number:	Revision:
Date:	2-Dec-2005	Time: 09:29:11	Sheet 20 of 33
File:	EP9315_MAIN.Sch 5		

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- INT[0:3] interrupts are active high level-sensitive
- EGPIO[0:16] interrupts can be configure as active high/low, rising/falling edge trigger

EP9315 System

U4 DS1339C
ARM_I2C_SCL 15
ARM_I2C_SDA 16
SCL
SDA
DS1339C
SQW → WDT_CLK
VCC → VDD3V3
VBACKUP → VBACKUP
GND
NC

Y3 32.768kHz NOP
U17
X1
X2
DS1339
SQW → WDT_CLK
VCC → VDD3V3
VBACKUP
GND
I2C
SCL
SDA
DS1339, NOP
BAT1 LI_BATTERY
C273 0.1uF

ETH_INT
DSPA_INT
TW2824A_INT

EP9315_PORn
EP9315_RSTn
R145 0 NOP
R224 0
RP21 10K

- EECLK select internal boot mode
- PU: internal boot (default)
- PD: external boot

R118 50K
R119 1K
- PU: EEDAT must pull up (default)
- PD: not allowed

R121 1K NOP

U2A
PRSTn
RSTOn
Reset
EECLK
EEDAT
EEPROM
SLA[1]
SLA[0]
I2C_SCL
I2C_SDA
R227 0
R228 0
AL_DIN3
AL_DIN2

- SLA0, SLA1, GRLED, RDLED are configure as GPIO, input type
- alarm input from Alarm&PWR board

AL_DIN3
AL_DIN2
AL_DIN1
AL_DIN0

LED
GRLED
RDLED
AL_DIN1
AL_DIN0
D15 LED_GREEN
D16 LED_RED
R123 560
R124 560

R113 1M
VDD1V8
L35 BLM21P331SN1
PLL_VDD
PLL_GND
PLL
RTC
RTCXTALI
RTCXTALO
Y4 14.7456MHz
C269 180pF
C270 18pF

IDE_INT
ETH_INT
INT
INT[3]
INT[2]
INT[1]
INT[0]
INT2
JTAG
TCK
TDI
TDO
TMS
TRSTn
R122 1M
Y2 608kHz
C272 47pF
C274 150pF

BOOT[1]
BOOT[0]
BOOT
NC
EP9315

VDD3V3
R115 1K

- Select serial boot mode

BOOT1	BOOT0	Mode
0	1	serial boot
0	0	non serial boot (default)

JP13 JUMPER2
R116 10K
R117 10K

U25
A0
A1
WP
NC
VDD
GND
SDA
SCL
AT24C128 NOP
C164 0.1uF

RP22 10K
R125 10K
JP17 HEADER10X2 ICE JTAG
JP16 JUMPER2
- default open

Title	EP9315 System Setting		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:11	Sheet 21 of 33	
File: EP9315_system.Sch.5			

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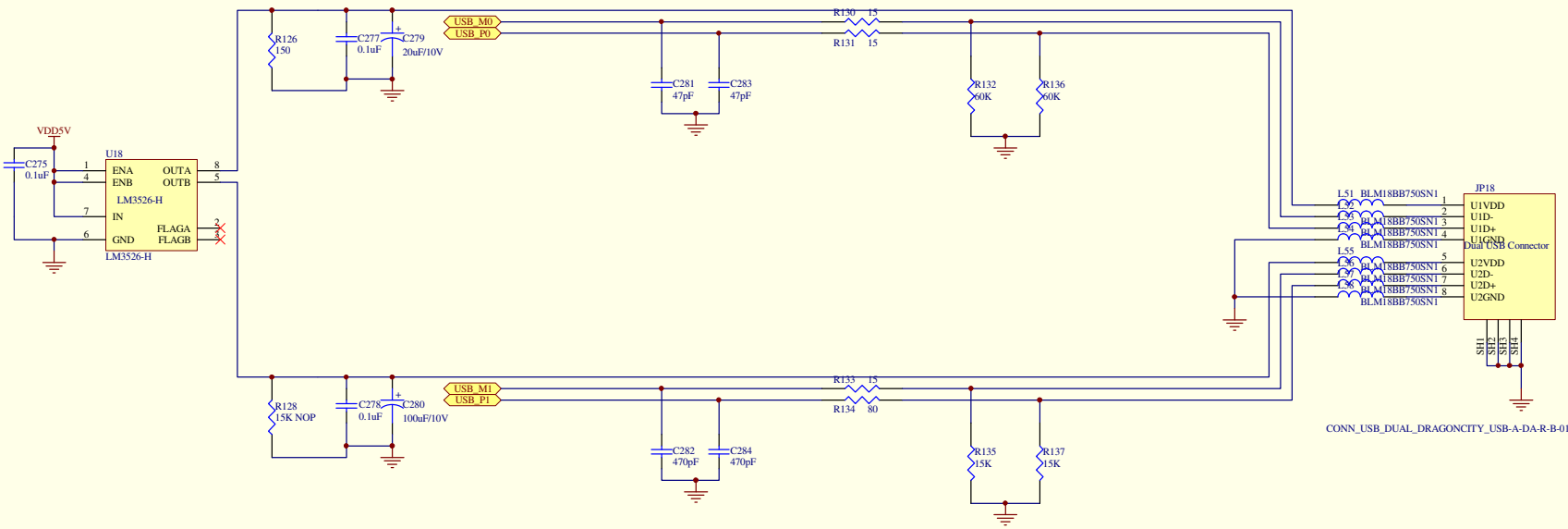
EP9315 USB Interface



Title	EP9315 USB		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:12	Sheet 22 of 33	
File: EP9315_USB.Sch 5			

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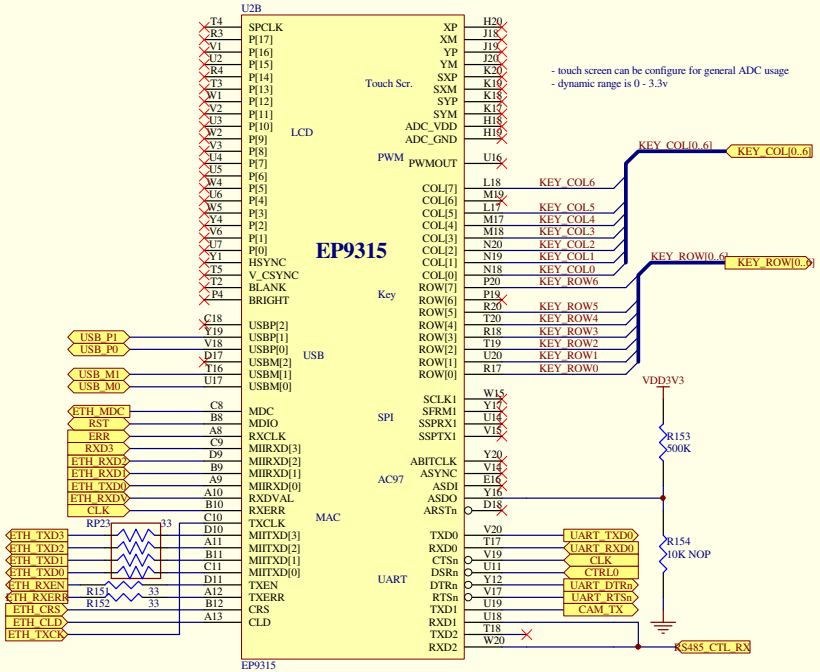
Kowloon, Hong Kong

EP9315 Peripheral



Title: EP9315 Peripherals		
Size: B	Number:	Revision:
Date: 2-Dec-2005 Time: 09:29:12	Sheet 24 of 33	
File: EP9315_Peripheral.Sch		

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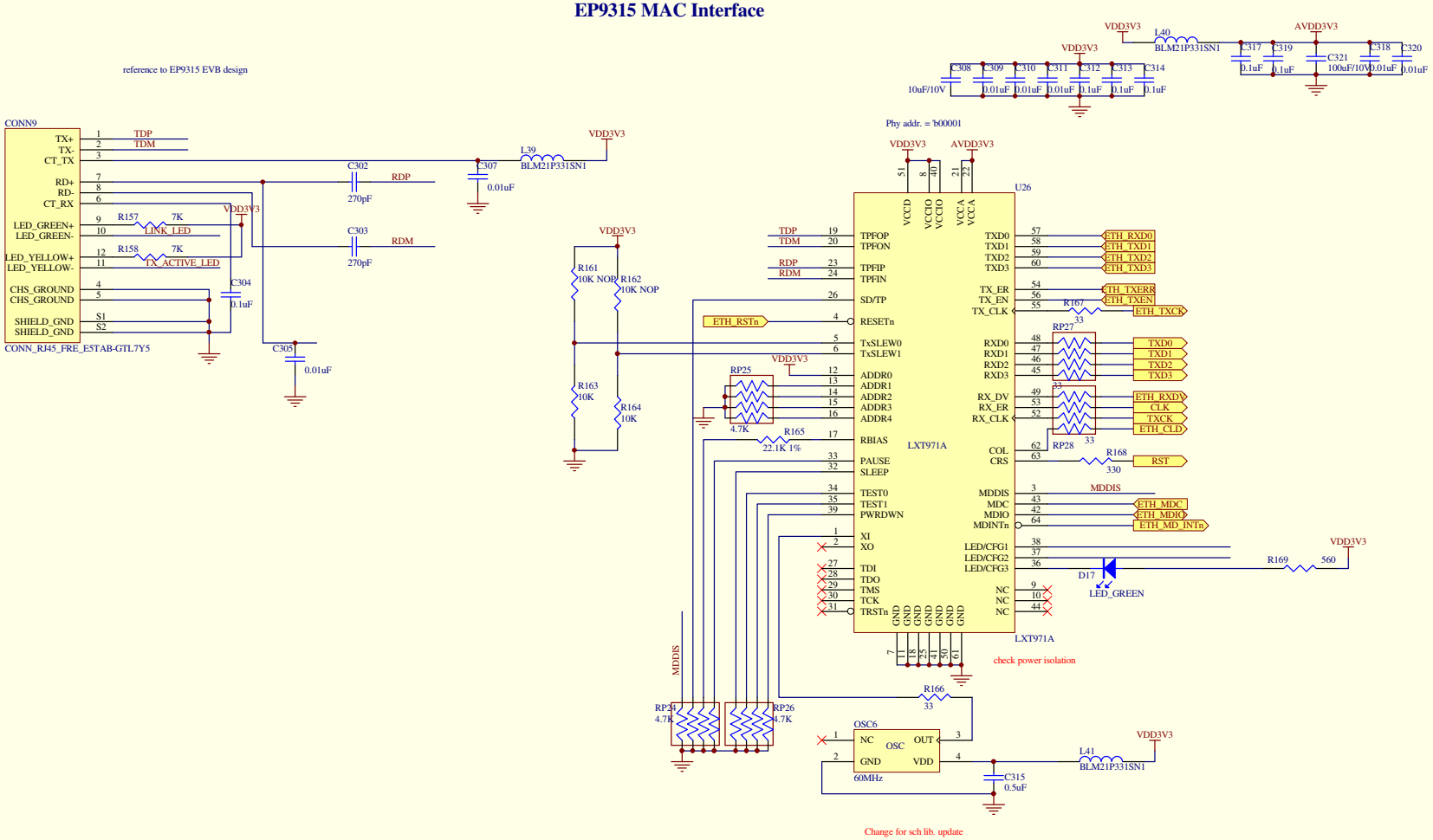
Kowloon, Hong Kong

EP9315 MAC Interface



Title: EP9315 MAC			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:12	Sheet 25 of 33	
File: EP9315_MAC.Sch_5			

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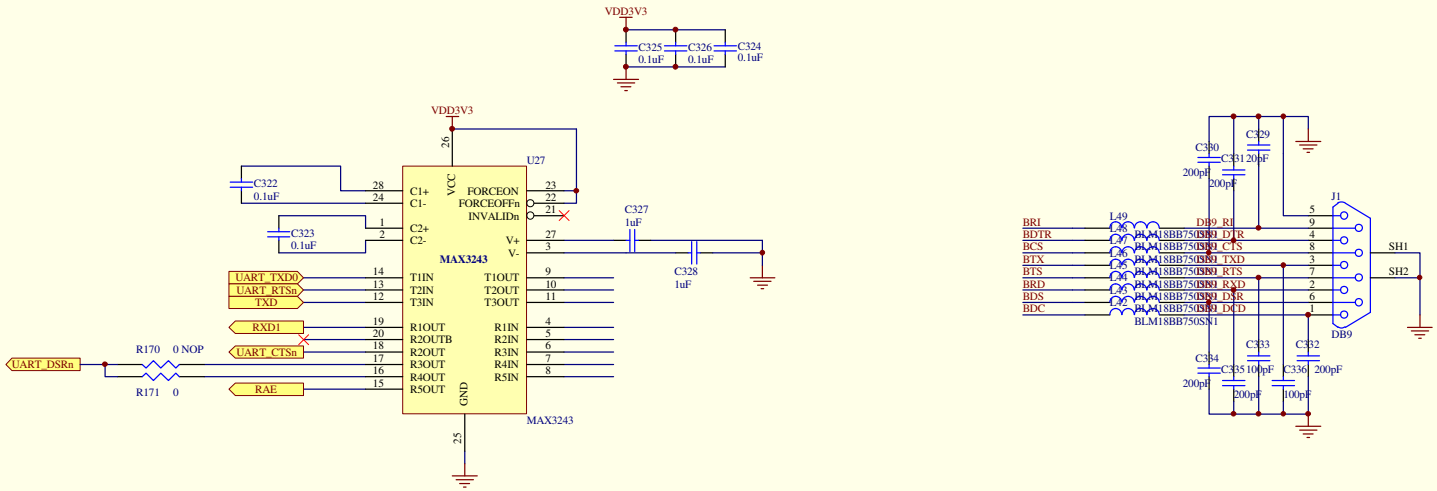
EP9315 UART Interface



Title	EP9315 UART		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:12	Sheet 26 of 33	
File: EP9315_UART.Sch.5			

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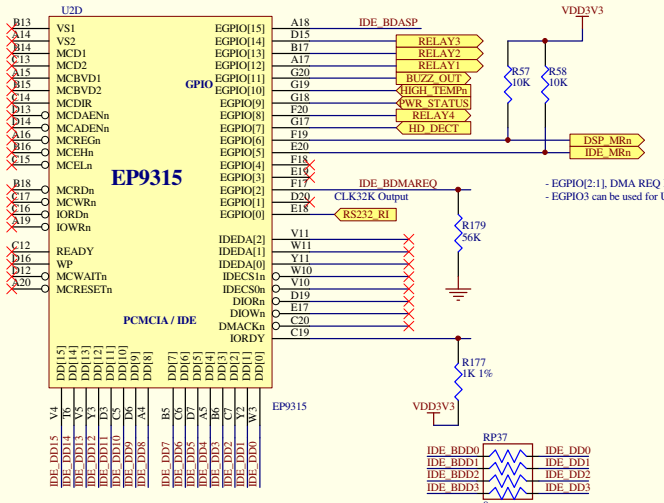
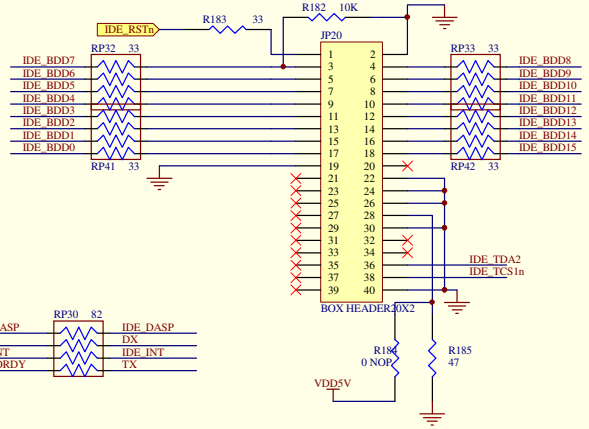
EP9315 IDE Interface & GPIO

- GPIO is configure as default mode which include:
-- EGPIO[7:0] : Port A
-- EGPIO[15:8] : Port B
-- GRLED, RDLED : Port E[0:1]
-- PCMCIA : Port F
-- EECLK, EEDAT : Port G[0:1]
-- Key Scanning : no map, remain key scanning function
-- IDE : no map, remain IDE function
- A, B, F are EGPIO ports, can be configure as interrupt inputs

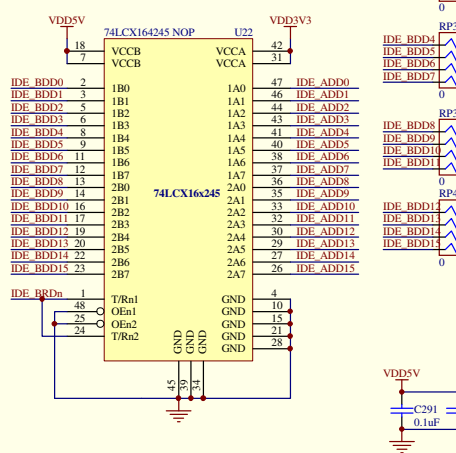
- GPIO[14] should be enabled w/ falling edge type interrupt for connection w/ LM75 O.S.
- The interrupt can be cleared by reading LM75 via I2C

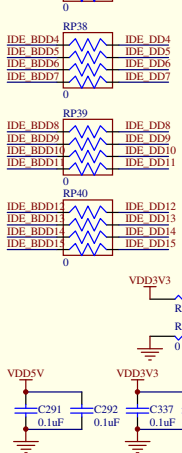


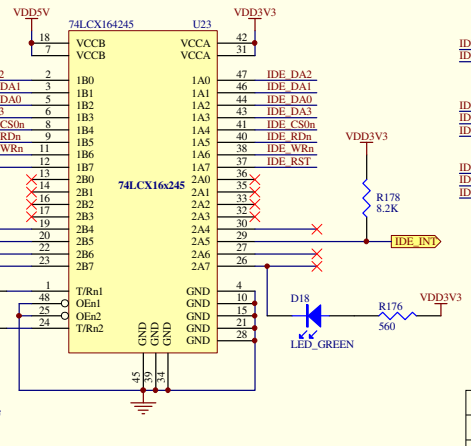
- EGPIO[2:1], DMA REQ Input
- EGPIO3 can be used for UART3 direction pin

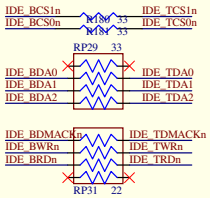


- The CSEL should be ground with according to IDE spec. Currently referenced to ARM EVB
- PDIAG (pin 34) should be open, according to IDE spec.









Title: EP9315 IDE			
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:12	Sheet 27 of 33	
File: EP9315_IDE.Sch 5			

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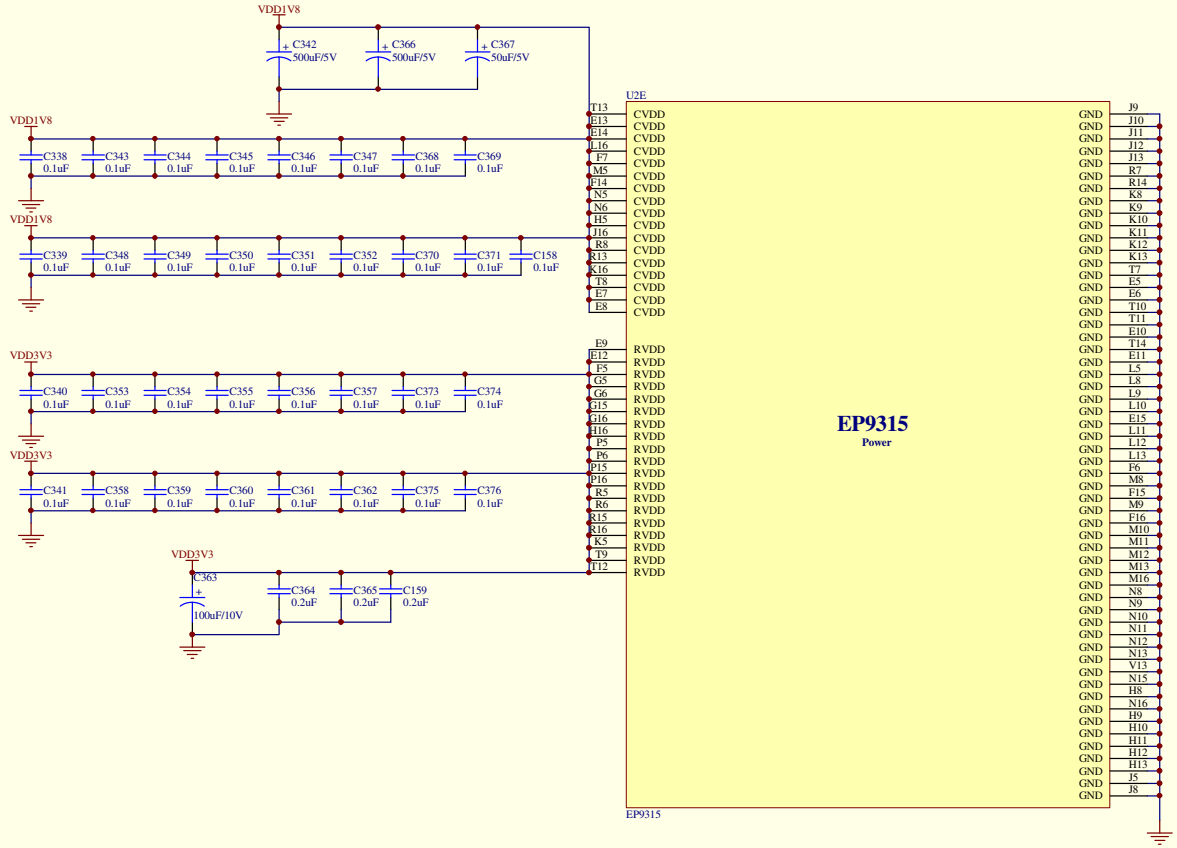
EP9315 Power



Title: EP9315 Power			Signal Communications Limited 16/F, Millennium City III, 370 Kwun Tong Road, Kowloon, Hong Kong
Size: B	Number:	Revision:	
Date: 2-Dec-2005 Time: 09:29:12	Sheet 28 of 33		
File: EP9315_Power.Sch 5			

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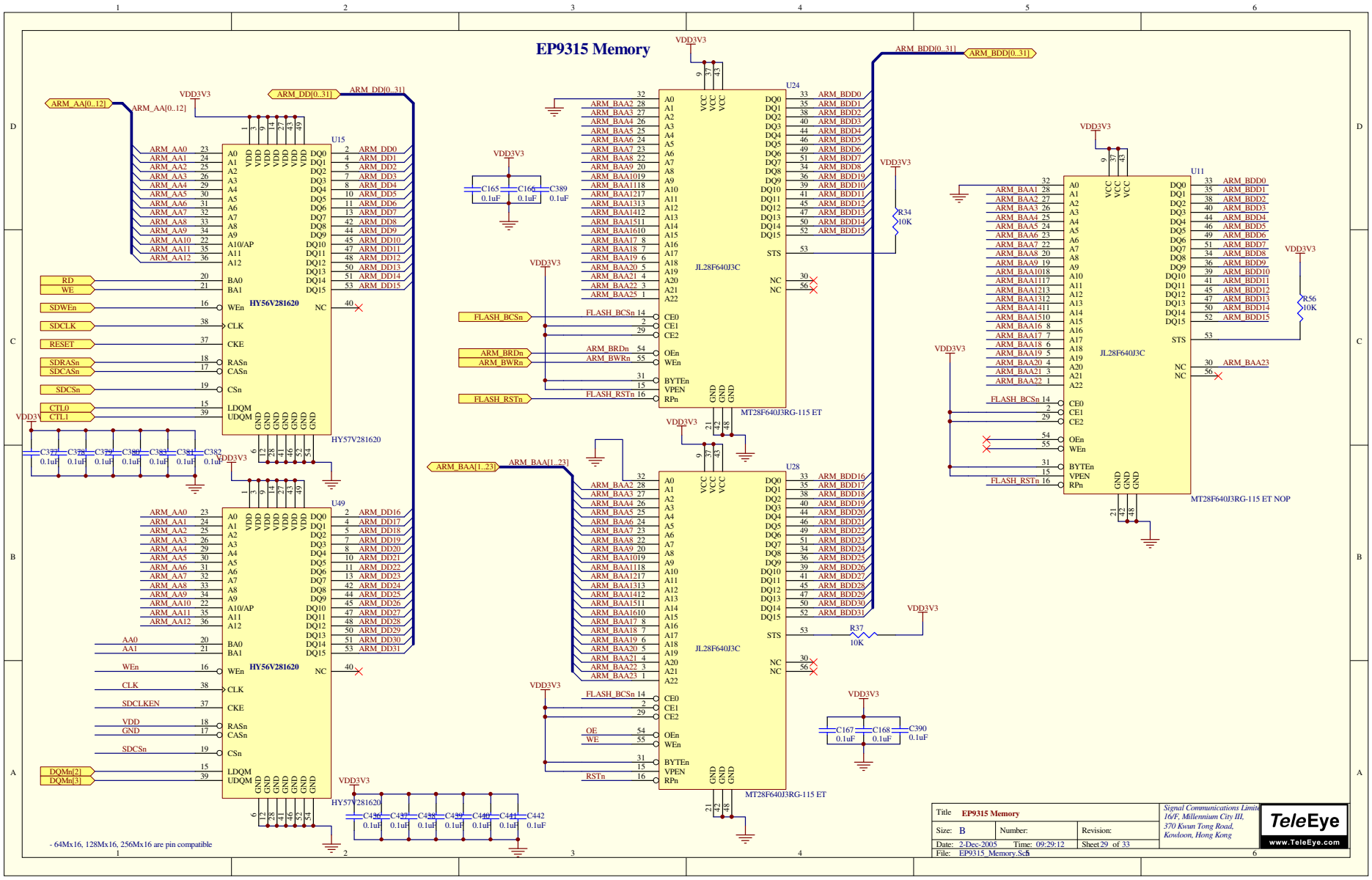
EP9315 Memory
U15
HY56V281620
HY57V281620
U49
U24
U28
JL28F640J3C
MT28F640J3RG-115 ET
U11
MT28F640J3RG-115 ET NOP
ARM_AA[0..12]
ARM_DD[0..31]
ARM_BDD[0..31]
ARM_BAA[1..23]
VDD3V3
RD
WE
SDWEn
SDCLK
RESET
SDRASn
SDCASn
SDCSn
CTL0
CTL1
DQMn[2]
DQMn[3]
FLASH_BCSn
ARM_BRDn
ARM_BWRn
FLASH_RSTn
R34 10K
R37 10K
R56 10K
- 64Mx16, 128Mx16, 256Mx16 are pin compatible
Title EP9315 Memory
Size: B
Number:
Revision:
Date: 2-Dec-2005 Time: 09:29:12
Sheet 29 of 33
File: EP9315_Memory.Sch
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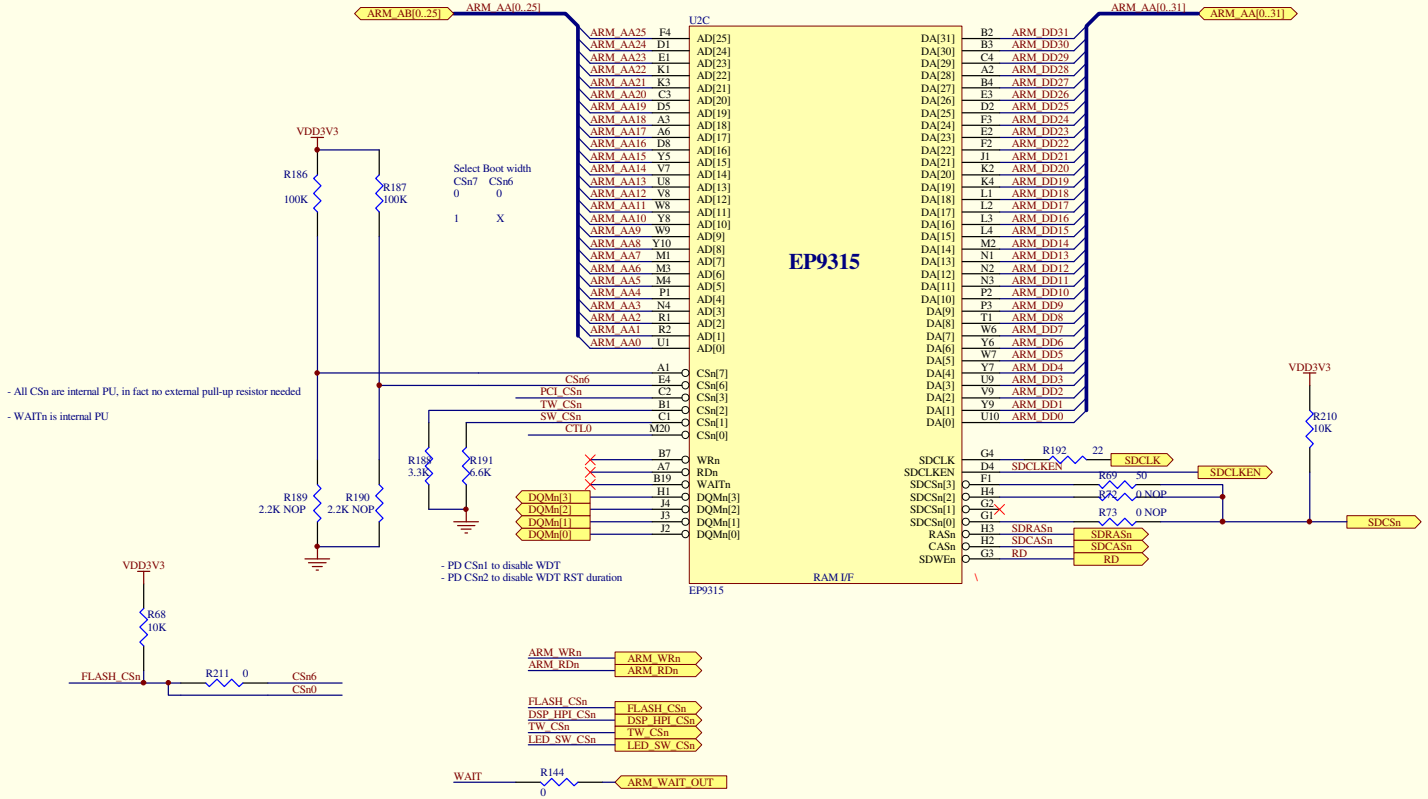
EP9315 Memory Interface



Title: EP9315 Memory Interface		
Size: B	Number:	Revision:
Date: 2-Dec-2005 Time: 09:29:12	Sheet 30 of 33	
File: EP9315_Mem_IF.Sch		

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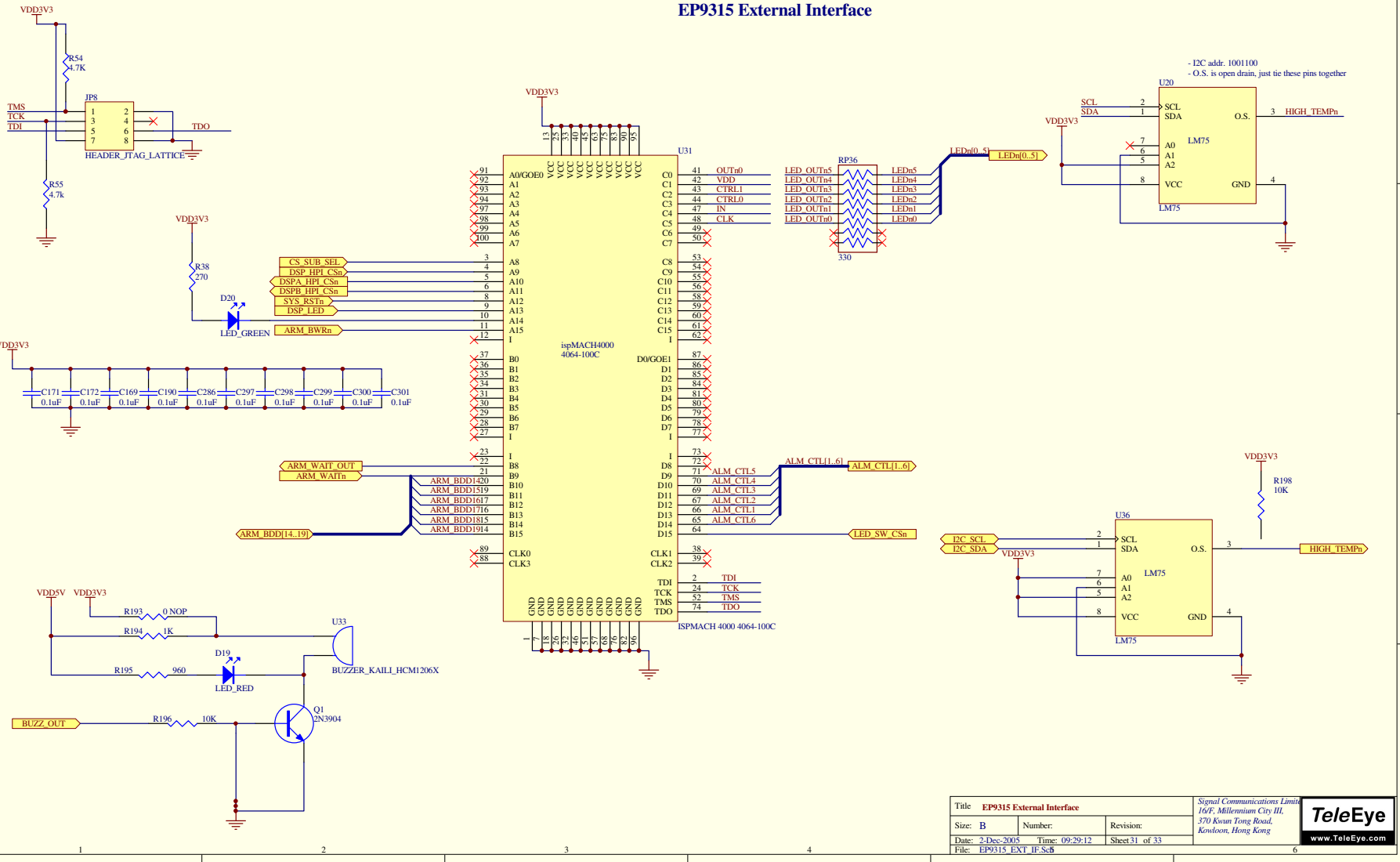
EP9315 External Interface
VDD3V3
R54
4.7K
JP8
TMS
TCK
TDI
TDO
HEADER_JTAG_LATTICE
R55
4.7k
R38
270
D20
LED_GREEN
CS_SUB_SEL
DSP_HPI_CSn
DSPA_HPI_CSn
DSPB_HPI_CSn
SYS_RSTn
DSP_LED
ARM_BWRn
C171 C172 C169 C190 C286 C297 C298 C299 C300 C301
0.1uF
U31
ispMACH4000
4064-100C
ISPMACH 4000 4064-100C
ARM_WAIT_OUT
ARM_WAITn
ARM_BDD[14..19]
ARM_BDD1420
ARM_BDD1519
ARM_BDD1617
ARM_BDD1716
ARM_BDD1815
ARM_BDD1914
ALM_CTL[1..6]
ALM_CTL5
ALM_CTL4
ALM_CTL3
ALM_CTL2
ALM_CTL1
ALM_CTL6
LED_SW_CSn
OUTn0
VDD
CTRL1
CTRL0
IN
CLK
TDI
TCK
TMS
TDO
RP36
330
LED_OUTn5
LED_OUTn4
LED_OUTn3
LED_OUTn2
LED_OUTn1
LED_OUTn0
LEDn5
LEDn4
LEDn3
LEDn2
LEDn1
LEDn0
LEDn[0..5]
- I2C addr. 1001100
- O.S. is open drain, just tie these pins together
U20
SCL
SDA
O.S.
HIGH_TEMPn
LM75
A0
A1
A2
VCC
GND
U36
R198
10K
I2C_SCL
I2C_SDA
VDD5V
R193
0 NOP
R194
1K
R195
960
D19
LED_RED
U33
BUZZER_KAILI_HCM1206X
BUZZ_OUT
R196
10K
Q1
2N3904
Title EP9315 External Interface
Size: B
Number:
Revision:
Date: 2-Dec-2005 Time: 09:29:12
Sheet 31 of 33
File: EP9315_EXT_IF.Sch
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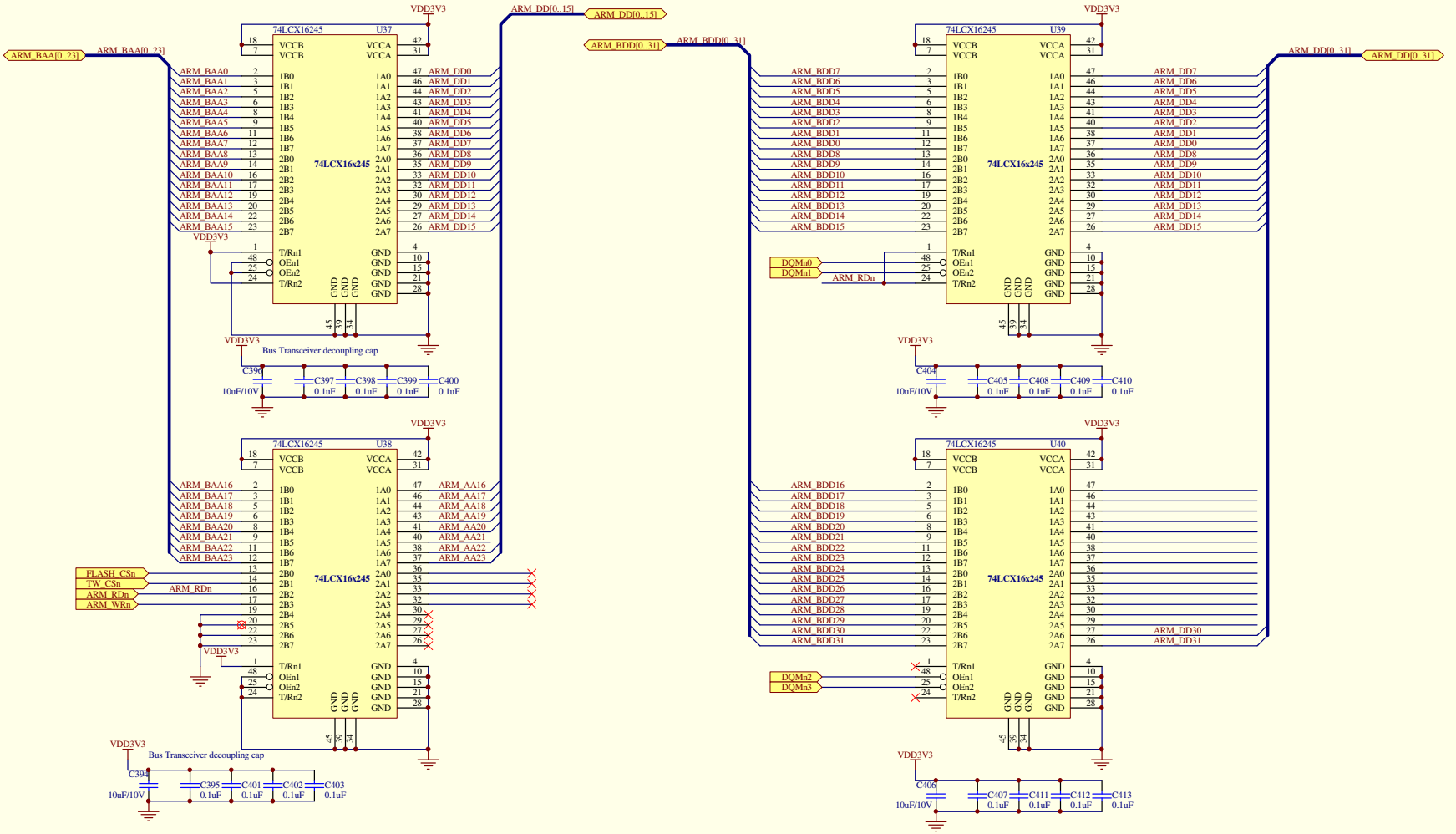
EP9315 Memory Buffer



Title	EP9315 memory buffering		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:13	Sheet 32 of 33	
File: EP9315_Mem_BUF.Sch			

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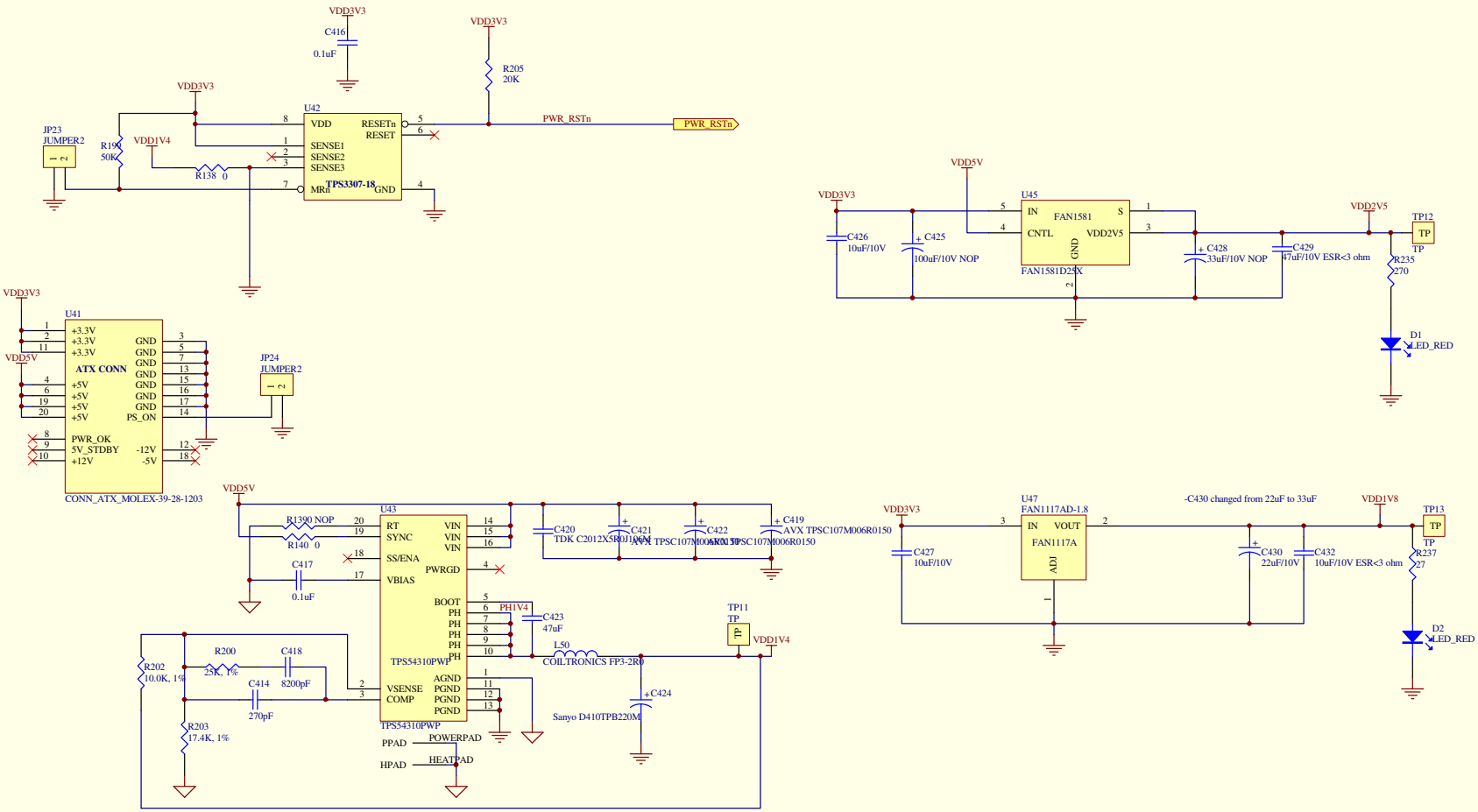
Power Regulation



Title	On-board Power Supply		
Size: B	Number:	Revision:	
Date: 2-Dec-2005	Time: 09:29:13	Sheet 33 of 33	
File: Power Regulation.Sch			

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