Modules

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# Product Technical Specification

## HL781x

January 2025

41114133 Rev. 15

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# Contact Information

| | |
|---|---|
| Sales information and technical support, including warranty and returns | Web: sierrawireless.com/company/contact-us/<br>Global toll-free number: 1-877-687-7795<br>6:00 am to 5:00 pm PST |
| Corporate and product information | Web: sierrawireless.com |

# Revision History

| Revision number | Release date | Changes |
|---|---|---|
| 1 | June 2021 | Creation |
| 2 | May 2022 | Updated:<br>▪ Current consumption values |
| 3 | May 2022 | Added:<br>▪ Taiwan NCC Statement |
| 4 | September 2022 | Updated:<br>▪ Table 3-7, Table 3-8, Table 3-9, Table 4-12 values<br>▪ Table 3-9 changed to Cat-NB<br>▪ For Table 3-14:<br>  ▪ NB1 UL peak throughput value changed from 62.5 to 45.7<br>  ▪ Subcarriers uplink changed from 3 to 12<br>▪ For Table 3-15<br>  ▪ Changed HL7810 to HL7812<br>  ▪ Removed duplicate MCS.TBS:13<br>  ▪ Changed NB2 UL peak throughput from 109 kbps to 159 kbps<br>  ▪ Changed Subcarriers uplink from 3 to 12<br>▪ Table 8-1 and Table 8-2 values<br>Added:<br>▪ Added Standby for Table 3-6, Table 3-7, Table 3-8, Table 3-9<br>▪ Added note for flash wear out feature under Table 3-5 |
| 5 | October 2022 | Updated:<br>▪ Table 8-1 Band 8<br>Added:<br>▪ Added RF Circuit |

| | | |
|---|---|---|
| 6 | December 2022 | Updated:<br>▪ Current Consumption—Added TX power in note<br>▪ Table 3-6, Table 3-7, Table 3-8, Table 3-9—Updated the PSM values, eDRX values, DRX running current value<br>▪ Table 4-21—Modified max wakeup timing for T1 and T2<br>▪ Table 4-22—Modified typ wakeup timing<br>▪ Table 4-23—Modified max wakeup timing for T2<br>▪ Added information under Current Consumption |
| 7 | April 2023 | Updated:<br>▪ Updated pin definition for C21 on Table 2-2<br>▪ Removed BAT_RTC from Figure 1-2<br>▪ Added Japan Radio and Telecom Approval |
| 8 | May 2023 | Updated:<br>▪ Updated Figure 2-1for C21, changed VBAT_BB to NC |
| 9 | August 2023 | Updated:<br>▪ Removed Patents section<br>▪ Updated Software Power Off in Unmanaged Mode steps |
| 10 | April 2024 | Updated:<br>▪ Updated to Semtech template<br>▪ Added GPIO7 Usage<br>▪ Updated C41 in Table 2-2<br>▪ Updated VBAT_BB min voltage for C63 and in Table 3-2 |
| 11 | July 2024 | Updated:<br>▪ Updated VBAT_BB min voltage in Table 1-4, Table 2-2, and Table 3-2 |
| 12 | September 2024 | Updated:<br>▪ Removed values for T1 min, T2 max, T5_eDRX min, and T5_PSM min in Table 4-7 and Table 4-8<br>▪ Added NTN bands in Table 1-1<br>▪ Added Table 4-26 and Table 4-29<br>▪ Updated T3: delay time maximum value in Table 4-21 |
| 13 | October 2024 | Updated:<br>▪ Added note for T4: delay in Table 4-12 |
| 14 | December 2024 | Updated:<br>▪ Added alternate function for C46 under Table 4-6<br>▪ Updated Table 1-4 General Features<br>▪ Updated Software Power Off in Unmanaged Mode<br>▪ Updated Tables 3-6, 3-7, 3-8, 3-9<br>▪ Updated Table 4-7<br>▪ Updated Fig 4-3 |
| 15 | January 2025 | Updated:<br>▪ Added B23 and B255 under Table 8-1 |

# Contents

# 1: Introduction

This document defines the high-level product features and illustrates the interfaces for Semtech HL781x Modules (HL7810, HL7812), designed for M2M and Internet of Things (IoT) markets. It covers the hardware aspects of the product series, including electrical and mechanical. For additional documentation (e.g. Firmware Customer Release Notes, AT Command Reference, etc.), refer to the module page at source.sierrawireless.com.

HL781x collectively identifies HL7810 and HL7812. Variant-specific content is identified where applicable. The HL781x supports a variety of interfaces such as USB FS, UART, ADC, GPIOs, and also supports the low power consumption hibernation modes to provide customers with flexibility in implementing high-end solutions.The key differentiators between HL781x variants are regulatory and industrial approvals/ certifications, and supported radio access technologies (RATs)-HL7810 supports Cat-M1/NB-IoT while HL7812 supports Cat-M1/NB-IoT/2G.

*Note: Semtech modules are shipped factory-programmed with industry or mobile operator approved firmware, according to the specific SKU ordered. Periodically, newer firmware versions become available and can include new features, bug fixes, or critical security updates. Semtech strongly recommends that customers establish their own production capability for updating module firmware on their assembled end platform, in the event that a newer firmware must be installed before deployment. Semtech also recommends customers design their products to support post-deployment FOTA upgrades using the AirVantage cloud platform.*

## 1.1 Supported RF Bands/Connectivity

The HL781x is a Semtech Ready-to-Connect (R2C) module that supports the use of its embedded SIM (eSIM) or an external SIM for global data connectivity on the RF bands detailed in the following module-specific tables.

For details about using the HL781x's eSIM with Sierra Smart Connectivity, refer to ▪ Sierra Wireless Ready-to-Connect Module Integration Guide Reference: 41113385. For additional information on Sierra Smart Connectivity, explore www.sierrawireless.com or contact Semtech.

*Note: The Semtech eSIM is SKU-dependent and not included in all modules. Contact Semtech for details.*

**Table 1-1: HL781x Supported RF Bands/Connectivity**

| Module | RF Band | Transmit (TX) Frequency (MHz) | Receive (Rx) Frequency (MHz) | NB-NTN | Cat-M1 | Cat-NB2 | 2G |
|---|---|---|---|---|---|---|---|
| HL7810<br>HL7812 | LTE B1 | 1920–1980 | 2110–2170 | | Y | Y | |
| | LTE B2 | 1850–1910 | 1930–1990 | | Y | Y[a] | |
| | LTE B3 | 1710–1785 | 1805–1880 | | Y | Y | |
| | LTE B4 | 1710–1755 | 2110–2155 | | Y | Y[a] | |
| | LTE B5 | 824–849 | 869–894 | | Y | Y[a] | |
| | LTE B8 | 880–915 | 925–960 | | Y | Y | |
| | LTE B12 | 699–716 | 729–746 | | Y | Y[a] | |
| | LTE B13 | 777–787 | 746–756 | | Y | Y[a] | |
| | LTE B18 | 815–830 | 860–875 | | Y | Y | |
| | LTE B19 | 830–845 | 875–890 | | Y | Y | |
| | LTE B20 | 832–862 | 791–821 | | Y | Y | |
| | LTE B25 | 1850–1915 | 1930–1995 | | Y | Y[a] | |
| | LTE B26 | 814–849 | 859–894 | | Y | Y[a] | |
| | LTE B28 | 703–748 | 758–803 | | Y | Y | |
| | LTE B66 | 1710–1780 | 2110–2200 | | Y | Y[a] | |
| | LTE B85 | 698–716 | 728-746 | | Y | Y[a] | |
| | NB-NTN B23 | 2000–2019.9 | 2180–2199.9 | Y | | | |
| | NB-NTN B255 | 1626.5–1660.4 | 1525–1558.9 | Y | | | |
| | NB-NTN B256 | 1980–2010 | 2170–2200 | Y | | | |
| HL7812 | GSM 850 | 824–849 | 869–894 | | | | Y |
| | E-GSM 900 | 880–915 | 925–960 | | | | Y |
| | DCS 1800 | 1710–1785 | 1805–1880 | | | | Y |
| | PCS 1900 | 1850–1910 | 1930–1990 | | | | Y |

a. To ensure FCC compliance near NB band edges, Cat-NB2 supported TX channel ranges do not include outer channels. Supported channel ranges are:
- B2: 18602–19198
- B4: 19952–20398
- B5: 20402–20648
- B12: 23012–23178
- B13: 23182–23278
- B25: 26042–26688
- B26: 26692–27038
- B66: 131974 - 132670
- B85: 134004–134179

# 1.2 Common Flexible Form Factor (CF3)

The HL781x belongs to Semtech's Common Flexible Form Factor (CF3) family of WWAN modules. These modules share a compatible footprint. The CF3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from GSM to LTE advanced) and band groupings
- Offers electrical and functional compatibility
- Provides direct mount, as well as socket mount (depending on customer needs,
- e.g. for use in development kits or for prototype development)

# 1.3 Physical Dimensions and Connection Interface

HL781x modules are compact, robust, fully shielded industrial-grade embedded modules with the dimensions noted in Table 1-2

**Table 1-2: Module Dimensions[a]**

| Parameter | Nominal | Tolerance | Units |
|---|---|---|---|
| Length | 18.0 | ±0.10 | mm |
| Width | 15.0 | ±0.10 | mm |
| Thickness | 2.4 | ±0.20 | mm |
| Weight | 1.17 | ±0.24 | g |

a. Typical dimensional values, accurate as of the release date of this document.

All electrical and mechanical connections to the HL781x module are made through the 86 Land Grid Array (LGA) pads on the bottom side of the PCB.

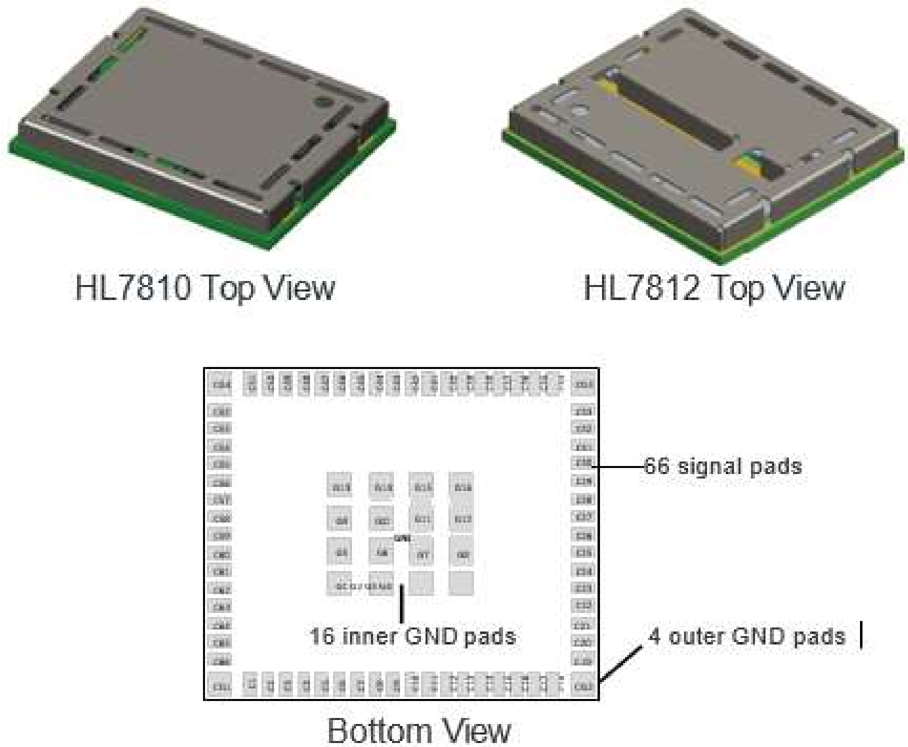


*Figure 1-1: Mechanical Overview*

Table 1-3 describes the LGA pads.

**Table 1-3: LGA Pad Types / Distribution**

| Pad Type | Quantity | Dimensions | Pitch |
|---|---|---|---|
| Signal pads | 66 pads | 1.0×0.5 mm | 0.8 mm |
| Ground pads | 16 inner pads | 1.0×1.0 mm | 1.825 mm/1.475 mm |
| | 4 outer corner pads | 0.85×0.97 mm | - |

# 1.4 General Features

Table 1-4 summarizes the HL781x's features.

**Table 1-4: General Features**

| Feature | Description |
|---|---|
| Physical | Small form factor (86-pad solderable LGA pad). See Physical Dimensions and Connection Interface for details.<br>Metal shield can<br>RF connection pads (RF_MAIN and RF_GNSS)<br>Baseband signals connection |
| Power supply | 2.4V–4.35V support voltage (VBAT_BB)<br>3.2V–4.35V supply voltage (VBAT_RF)<br>▪ Single supply (recommended)—VBAT (VBAT_BB tied to VBAT_RF) or<br>▪ Dual supplies—Single supply each for VBAT_BB and VBAT_RF |
| RF | 2G (HL7812 only)<br>▪ 850/900 Power Class 4 (33 dBm), GPRS Class 10<br>▪ 1800/1900 Power Class 1 (30 dBm), GPRS Class 10<br>Cat-M1<br>▪ Power Class 3 (23 dBm)<br>▪ Cat-NB2<br>▪ Power Class 3 (23 dBm)<br>GNSS<br>▪ GPS—1575.42 MHz<br>▪ GLONASS—1589.0625–1605.375 MHz<br>See GNSS details.<br>*Note: The GNSS receiver and LTE/GSM receiver share the same RF resources, therefore GNSS can only be used when the module is not actively connected on LTE/GSM. An example of a suitable implementation of GNSS in an end product would be the use of GNSS positioning for asset management applications where infrequent and no real-time position updates are required.* |
| SIM interface | 1.8V support<br>SIM extraction / hot plug detection<br>SIM/USIM support<br>Conforms with ETSI UICC Specifications<br>Supports SIM application tool kit with proactive UICC commands |
| Application interface | AT command interface—3GPP 27.007 standard, plus proprietary extended AT commands<br>CMUX multiplexing over UART<br>USB Full Speed (FS) |

**Table 1-4: General Features (Continued)**

| Feature | Description |
| --- | --- |
| Protocol stack | 2G (HL7812 only)<br>▪ GPRS Class 10<br>Cat-M1<br>▪ 3GPP Rel. 14:<br>  ▪ Up to 1100 kbit/s UL, 590 kbit/s DL<br>  ▪ HARQ-ACK bundling in HD-FDD<br>  ▪ 10 DL HARQ processes<br>  ▪ Faster frequency returning<br>  ▪ Release Assistance Indication<br>▪ Half-duplex<br>▪ Channel bandwidth—1.4 MHz<br>▪ LTE carrier bandwidth—1.4/3/5/10 /15/20 MHz<br>▪ Extended Coverage Mode A<br>▪ PSM (Power Save Mode)<br>▪ I-DRX (Idle Mode Discontinuous Reception)<br>▪ C-DRX (Connected Mode Discontinuous Reception)<br>▪ Idle mode mobility<br>▪ Connected mode mobility<br>▪ eDRX (Extended Discontinuous Reception)<br>▪ Control Plane CIoT Optimization (Data over NAS)<br>NB-IoT<br>▪ 3GPP Rel. 14:<br>  ▪ Up to 158 kbit/s UL, 127 kbit/s DL<br>  ▪ 2 HARQ processes<br>  ▪ Release Assistance Indication<br>  ▪ Long DRX values with regular wake-up cycle)<br>  ▪ Cat-NB2<br>▪ Half-duplex<br>▪ Channel bandwidth—180 kHz<br>▪ LTE carrier bandwidth—1.4/3/5/10 /15/20 MHz<br>▪ Operational mode—In-band, Guard band, Standalone<br>▪ Control Plane CIoT Optimization (Data over NAS)<br>▪ NIDD over SGi tunneling<br>▪ NIDD over SCEF<br>▪ Extended coverage<br>▪ PSM (Power Save Mode)<br>▪ I-DRX (Idle Mode Discontinuous Reception)<br>▪ C-DRX (Connected Mode Discontinuous Reception)<br>▪ Idle mode mobility<br>▪ eDRX (Extended Discontinuous Reception)<br>Flexible selection<br>▪ Manual system selection across RATs<br>▪ Dynamic system selection across RATs (preferred RAT) |

**Table 1-4: General Features (Continued)**

| Feature | Description |
|---|---|
| Connectivity | Multiple cellular packet data profiles<br>Sleep mode for minimum idle power draw<br>Mobile-originated PDP context activation / deactivation<br>Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol).<br>PDP context type (IPv4, IPv6, IPv4v6)<br>RFC1144 TCP/IP header compression |
| Environmental | Operating temperature ranges<br>▪ Class A: -30°C to +70°C<br>▪ Class B: -40°C to +85°C |
| RTC | Real Time Clock (RTC) |

# 1.5 Architecture

Figure 1-2 presents an overview of the HL781x's internal architecture and external interfaces.

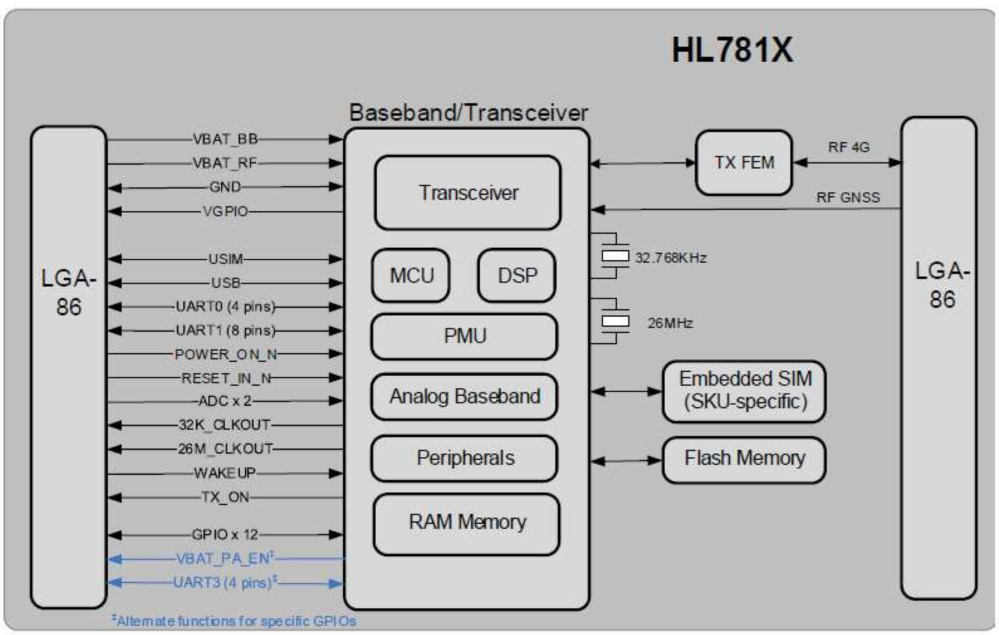


*Figure 1-2: Architecture Overview*

# 1.6 Interfaces

The HL781x provides the following interfaces and peripheral connectivity:

- (1) VGPIO (1.8V)— See VGPIO
- (1) 1.8V USIM— See USIM Interface
- (1) USB 2.0 FS— See USB Interface.
- (12) GPIOs— See General Purpose Input/Output (GPIO).
- (1) 8-wire UART— See Main Serial Link (UART1).
- (1) Active low power on signal (will be available in a future firmware release)— See Power On Signal (POWER_ON_N).
- (1) Active low reset signal— See Reset Signal (RESET_IN_N).
- (2) ADC— See Analog to Digital Converter (ADC).
- (2) System clock out (32.768 kHz and 26 MHz)— See Clock Interface.
- (1) 4-wire UART for debug interface only— See Debug Interfaces.
- (1) Wake up signal— See Wake Up Signal (WAKEUP).
- (1) Main RF Antenna— See RF Interface.
- (1) TX_ON indicator— See TX Burst Indicator (TX_ON).
- (1) GNSS Antenna — See GNSS.
- (1) External PA Voltage Control Indicator— SeeTx/Rx Activity Indicator; External RF Voltage Control.

**Table 1-5: ESD Specifications[a]**

| Category | Connection | Specification |
|---|---|---|
| Operational | ▪ Power supply (C61, C62, C63)<br>▪ RF ports (C38, C49) | IEC-61000-4-2 (Electrostatic Discharge Immunity Test)<br>▪ ±6 kV Contact<br>▪ ±8 kV Air |
| Non-operational | All pins | Unless otherwise specified:<br>▪ JESD22-A114 ± 250 V Human Body Model<br>▪ JESD22-C101C ± 250V Charged Device Model |

a. ESD protection is highly recommended on customer platform. For details, see ESD Protection for I/Os

# 1.7 Environmental Specifications

The environmental specifications for operation and storage of the HL781x are defined in Table 1-6.

**Table 1-6: Environmental Specifications**

| Parameter | Range | Operating Class |
|---|---|---|
| Ambient Operating Temperature | -30°C to +70°C | Class A |
| | -40°C to +85°C | Class B |
| Ambient Storage Temperature | -40°C to +85°C | - |

Class A is defined as the operating temperature range within which the device:
- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature range within which the device:
- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish any of the device's supported call modes (SMS, Data, and emergency calls) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

# 2: Pad Definition

The HL781x pins are divided into three categories.

- Core functions and associated pins— Cover all the mandatory features for M2M connectivity and will be available by default across the CF3 module family. These Core functions are always available and always at the same physical pad locations. A customer platform using only these functions and associated pads is guaranteed to be forward and/or backward compatible with the next generation of CF3 modules.
- Extension functions and associated pins— Bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pad location.
- Custom functions and associated pins— Module-specific functionality. If a custom function is available on another module, there is no guarantee that it will be at the same pad location.

For example:

- UART1 interface is a "Core" function on pins C2–C9 that is available on all CF3 modules (including HL781x).
- USB interface is an "Extension" function on pins C12–C13 that is available on HL781x modules, but may not be available on certain other CF3 modules.
- UART0 signals are "Custom" functions on pins C57 and C58. These signals may or may not be available on other CF3 modules and, if available, may be on different pins.

Pins marked as "Not connected" should not be used.

## 2.1 Pin Types

Table 2-1 lists a series of codes used to identify pin characteristics throughout this document.

**Table 2-1: Pin Type Codes**

| Code | Definition |
|---|---|
| AI | Analog Input |
| ANT | Antenna |
| GND | Ground |
| I | Digital Input |
| I/O | Digital Input/Output |
| N/A | Not applicable |

| Code | Definition |
|---|---|
| O | Digital Output |
| PD | Pull-down enabled |
| PI | Power In |
| PO | Power Out |
| PU | Pull-up enabled |
| | |

**Table 2-2: Pin Definitions**

| Pin | Signal Name | Group | I/O | Voltage Supply Domain | Function | Recommendation for unused pads | Isolate required[a] | CF3 |
|---|---|---|---|---|---|---|---|---|
| C1 | GPIO1 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| C2 | UART1_RI[c] | UART1[b] | O | 1.8V (VGPIO) | UART1 Ring Indicator | Leave open | Yes | Core |
| C3 | UART1_RTS | UART1[b] | I | 1.8V (VGPIO) | UART1 Request To Send | Mandatory connection | Yes | Core |
| C4 | UART1_CTS | UART1[b] | O | 1.8V (VGPIO) | UART1 Clear To Send | Mandatory connection | Yes | Core |
| C5 | UART1_TX | UART1[b] | I | 1.8V (VGPIO) | UART1 Transmit Data | Mandatory connection | Yes | Core |
| C6 | UART1_RX | UART1[b] | O | 1.8V (VGPIO) | UART1 Receive Data | Mandatory connection | Yes | Core |
| C7 | UART1_DTR | UART1[b] | I | 1.8V (VGPIO) | UART1 Data Terminal Ready | Leave open | Yes | Core |
| C8 | UART1_DCD | UART1[b] | O | 1.8V (VGPIO) | UART1 Data Carrier Detect | Leave open | Yes | Core |
| C9 | UART1_DSR | UART1[b] | O | 1.8V (VGPIO) | UART1 Data Set Ready | Leave open | Yes | Core |
| C10 | GPIO2 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Core |
| C11 | RESET_IN_N | H/W Control[d] | I | Internal Bias | Input reset signal | Leave open | No | Core |
| C12 | USB_D- | USB | I/O | 3.3V | USB Data Negative (Full Speed) | Leave open | No | Extension |
| C13 | USB_D+ | USB | I/O | 3.3V | USB Data Positive (Full Speed) | Leave open | No | Extension |
| C14 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C15 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C16 | USB_VBUS | USB | PI | 5V | USB VBUS | If USB is:<br>▪ Not used—Leave open<br>▪ Used—Mandatory connection | No | Extension |

**Table 2-2: Pin Definitions (Continued)**

| Pin | Signal Name | Group | I/O | Voltage Supply Domain | Function | Recommendation for unused pads | Isolate required[a] | CF3 |
|---|---|---|---|---|---|---|---|---|
| C17 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C18 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C19 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C20 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C21 | NC | Not connected | | | Not Connected | Leave open | No | Not connected |
| C22 | 26M_CLKOUT | Clock[b] | O | 1.8V (VGPIO) | 26 MHz System Clock Output | Leave open | Yes | Extension |
| C23 | 32K_CLKOUT | Clock[b] | O | 1.8V (VGPIO) | 32.768 kHz System Clock Output | Leave open | Yes | Extension |
| C24 | ADC1 | ADC[b] | AI | 1.8V (VGPIO) | Analog to digital converter | Leave open | Yes | Extension |
| C25 | ADC0 | ADC[b] | AI | 1.8V (VGPIO) | Analog to digital converter | Leave open | Yes | Extension |
| C26 | UIM1_VCC | UIM[b] | PO | 1.8V | USIM1 Power supply | Leave open | No | Core |
| C27 | UIM1_CLK | UIM[b] | O | 1.8V (VGPIO) | USIM1 Clock | Leave open | No | Core |
| C28 | UIM1_DATA | UIM[b] | I/O | 1.8V (VGPIO) | USIM1 Data | Leave open | No | Core |
| C29 | UIM1_RESET | UIM[b] | O | 1.8V (VGPIO) | USIM1 Reset | Leave open | No | Core |
| C30 | RF_DIV_GND_1 | Ground | GND | Ground | Ground | Mandatory connection | No | Extension |
| C31 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C32 | RF_DIV_GND_2 | Ground | GND | Ground | Ground | Mandatory connection | No | Extension |
| C33 | Reserved | Reserved | | | Reserved | Leave open[f] | No | Extension |
| C34 | Reserved | Reserved | | | Reserved | Leave open[f] | No | Extension |

**Table 2-2: Pin Definitions (Continued)**

| Pin | Signal Name | Group | I/O | Voltage Supply Domain | Function | Recommendation for unused pads | Isolate required[a] | CF3 |
|---|---|---|---|---|---|---|---|---|
| C35 | Reserved | Reserved | | | Reserved | Leave open[f] | No | Extension |
| C36 | Reserved | Reserved | | | Reserved | Leave open[f] | No | Extension |
| C37 | RF_GNSS_GND_1 | Ground | GND | Ground | Ground (RF_GNSS) | Mandatory connection | No | Core |
| C38 | RF_GNSS | Antenna | ANT | | GNSS antenna input | Leave open | No | Extension |
| C39 | RF_GNSS_GND_2 | Ground | GND | Ground | Ground (RF_GNSS) | Mandatory connection | No | Core |
| C40 | GPIO7 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Core |
| | | | O | | Module activity indication | | | |
| C41[g] | GPIO8 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Core |
| | VBAT_PA_EN | | O | | Tx/Rx activity indicator/External RF voltage control | | | Custom |
| C42 | NC | Not connected | | | Not Connected | See footnote[e] | No | Not connected |
| C43 | Reserved | Reserved | | | Reserved | Leave open[f] | No | Extension |
| C44 | WAKEUP | H/W Control[d] | I | 1.8V | Wake up signal | Mandatory connection | No | Extension |
| C45 | VGPIO | Power | PO | 1.8V (VGPIO) | GPIO voltage output (reference voltage) | Leave open | No | Core |
| C46 | GPIO6 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Core |
| C47 | NC | Not connected | | | Not Connected | Leave open[e] | No | Not connected |
| C48 | RF_MAIN_GND_1 | Ground | GND | Ground | Ground (RF_MAIN) | Mandatory connection | No | Core |
| C49 | RF_MAIN | Antenna | ANT | | Main RF antenna input/output (Rx/Tx) | Mandatory connection | No | Core |
| C50 | RF_MAIN_GND_2 | Ground | GND | Ground | Ground (RF_MAIN) | Mandatory connection | No | Core |

**Table 2-2: Pin Definitions (Continued)**

| Pin | Signal Name | Group | I/O | Voltage Supply Domain | Function | Recommendation for unused pads | Isolate required[a] | CF3 |
|---|---|---|---|---|---|---|---|---|
| C51 | GPIO14 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| | UART3_CTS | UART3[b] | O | | (MLI debug) UART3 Clear To Send | | | Custom |
| C52 | GPIO10 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| | UART3_TX | UART3[b] | I | | (MLI debug) UART3 Transmit data | | | Custom |
| C53 | GPIO11 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| | UART3_RTS | UART3[b] | I | | (MLI debug) UART3 Request To Send | | | Custom |
| C54 | GPIO15 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| | UART3_RX | UART3[b] | O | | (MLI debug) UART3 Receive data | | | Custom |
| C55 | UART0_RX | UART0[b] | O | 1.8V (VGPIO) | Debug Receive data | Leave open | Yes | Extension |
| C56 | UART0_TX | UART0[b] | I | 1.8V (VGPIO) | Debug Transmit data | Leave open | Yes | Extension |
| C57 | UART0_CTS | UART0[b] | O | 1.8V (VGPIO) | Debug Clear To Send | Leave open | Yes | Custom |
| C58 | UART0_RTS | UART0[b] | I | 1.8V (VGPIO) | Debug Request To Send | Leave open | Yes | Custom |
| C59 | POWER_ON_N | H/W Control[d] | I | Internal Bias | Active-low Power On control signal | Leave open | No | Core |
| C60 | TX_ON | Indication[b] | O | 1.8V (VGPIO) | TX transmission indication | Leave open | Yes | Extension |
| C61 | VBAT_RF | Power | PI | 3.2V (min)<br>3.7V (typ) 4.35V (max) | Power supply | Mandatory connection | No | Core |
| C62 | VBAT_RF | Power | PI | 3.2V (min)<br>3.7V (typ) 4.35V (max) | Power supply | Mandatory connection | No | Core |

**Table 2-2: Pin Definitions (Continued)**

| Pin | Signal Name | Group | I/O | Voltage Supply Domain | Function | Recommendation for unused pads | Isolate required[a] | CF3 |
|---|---|---|---|---|---|---|---|---|
| C63 | VBAT_BB | Power | PI | 2.4V (min)<br>3.7V (typ) 4.35V (max) | Power supply | Mandatory connection | No | Core |
| C64 | UIM1_DET | UIM1[b] | I | 1.8V (VGPIO) | UIM1 Detection | Leave open | Yes | Core |
| | GPIO3 | GPIO[b] | I/O | | General purpose input/output | | | Extension |
| C65 | GPIO4 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| C66 | GPIO5 | GPIO[b] | I/O | 1.8V (VGPIO) | General purpose input/output | Leave open | Yes | Extension |
| CG1-CG4 | GND | Ground | GND | Ground | Ground | Mandatory connection | No | Core |
| G1-G16 | GND | Ground | GND | Ground | Ground | Mandatory connection | No | Core |

a. The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate—Isolation Requirements.
b. By default, signals in group (GPIO, UART, UIM1, ADC, Clock, Indication) are hardware-configured as inputs and are in an undefined state during OFF, reset, and Hibernate modes. The host should ignore all activity on these signals until the module has initialized and reached AT-READY (UART1_CTS transitions from high to low (and stays low) and VGPIO is high, indicating the UART and USB interfaces are ready). For timing details, see Unmanaged POWER_ON_N (Default) and Wakeup from OFF Mode. For further information regarding pre- and post-AT-READY signal states, contact Semtech.
c. UART1_RI cannot be used in Hibernate mode. A GPIO (GPIO2 by default) can be configured as an alternate ring indicator. For details, see Ring Indicator (UART1_RI or Alternative).
d. Hardware Control signals are available in all module operational modes and determine module behavior. For recommendations on managing these signals, see associated signal topics in Detailed Interface Specifications.
e. Pin is not connected internally, but is reserved for future use. Leave unconnected to ensure compatibility with other Semtech CF3 modules.
f. Pin is connected internally, leave open.
g. Default function is VBAT_PA_EN. Contact Semtech to enable GPIO function.

## 2.2 Pad Configuration

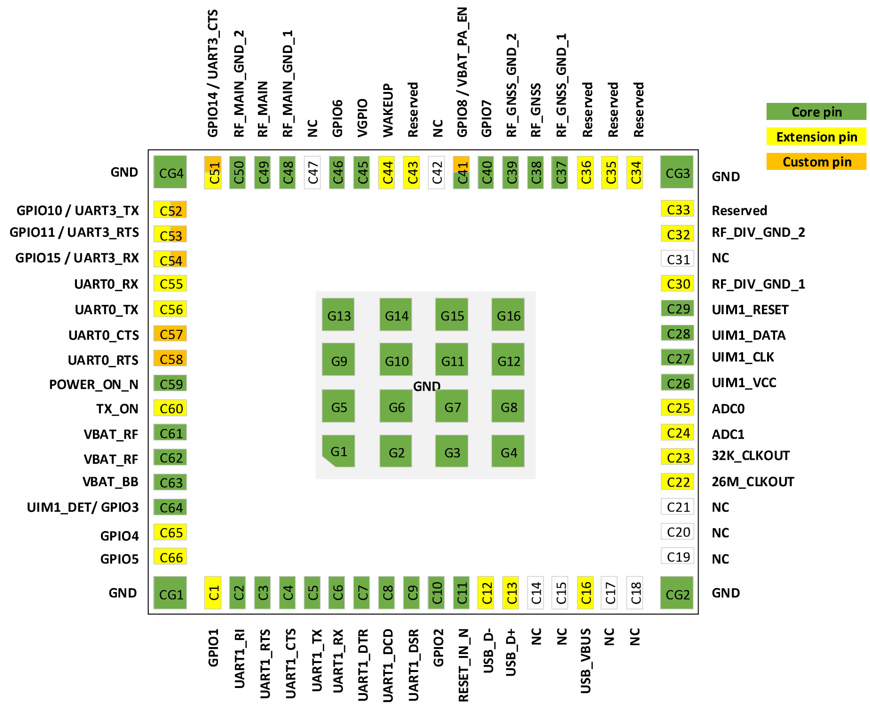


*Figure 2-1: Pad Configuration (Top View through Module)*

# 3: Power Specifications

*Note: If not specified, all electrical values are given for VBAT_BB and VBAT_RF = 3.7V, operating temperature of 25 °C. and with conducted 50Ω load on RF port(s).*

## 3.1 Power Supply

The module is supplied through the VBAT_BB and VBAT_RF signals.

For standard applications, VBAT_BB and VBAT_RF must be tied externally to the same power supply. For some specific applications (e.g. applications requiring a lower VBAT_RF), the module supports separate VBAT_BB and VBAT_RF connection as per Table 3-1.

Table 3-1 and Table 3-2 describe the Power Supply interface.

**Table 3-1: Power Supply Pin Description**

| Pad # | Signal Name | I/O | Description |
|---|---|---|---|
| C63 | VBAT_BB | PI | Power supply (baseband) |
| C61, C62 | VBAT_RF | PI | Power supply (radio frequency) |
| C30, C32, C37, C39, C48, C50, CG1– CG4, G1–G16 | | GND | Ground |

**Caution:** *Operation outside the minimum/maximum specified operating voltage (Table 3-2) is not recommended, and functional operation of the device and specified typical performance are neither implied nor guaranteed.*

**Table 3-2: Power Supply Current Requirements**

| Parameter | | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| VBAT_BB voltage | | 2.4[a] | 3.7 | 4.35 | V | Must be within min/max values overall operating conditions (including voltage ripple, droop, and transient) |
| VBAT_RF voltage Full Specification | | 3.2 | 3.7 | 4.35 | V | |
| VBAT_RF voltage Extended Range | | 2.8[b] | 3.7 | 4.35 | V | |
| Power Supply Ripple | | - | - | 100[c] | mVpp | |
| Max Supply Current | VBAT_BB | - | - | 180 | mA | |
| | VBAT_RF (LTE) | - | - | (HL7810) 300<br>(HL7812) 400 | mA | |
| | (HL7812 only)<br>VBAT_RF (2G)<br>Peak Current | - | 1.9 | 2.5 | A | |

a. VBAT_BB from 2.4-3.2V is functional but the power source must be sufficient, and the impedance of power source or power path should be as low as possible to reduce the voltage drop. Note that operation in this range requires a separate VBAT_BB supply.
b. 3GPP performance is not guaranteed for VBAT_RF from 2.8-3.2V. Note that operation in this range requires a separate VBAT_RF supply.
c. Measured at nominal supply voltage (3.7V), nominal ambient temperature (25°C), and with conducted 50Ω load on RF port(s).

*Note: The host power supply should be capable of supplying* $VBAT\_BB_{max}$ + $VBAT\_RF_{max}$.

# 3.2 Electrical Specifications

## 3.2.1 Digital I/O Characteristics

The I/O characteristics for supported digital interfaces/signals are described in Table 3-3. These interfaces/signals include:

- UARTs
- GPIOs
- Clock output signals
- UIM1
- TX_ON
- External PA voltage control indicator

These signals are not available in Hibernate mode since VGPIO is OFF.

*Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate—Isolation Requirements.*

**Table 3-3: Digital I/O Electrical Characteristics (1.80V)[a]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Logic High Input Voltage | 0.7 × VGPIO | VGPIO | V |
| $V_{IL}$ | Logic High Input Voltage | 0 | 0.3 × VGPIO | V |
| $V_{OH}$ | Logic High Input Voltage | 0.8 × VGPIO | | V |
| $V_{OL}$ | Logic High Input Voltage | | 0.2 × VGPIO | V |
| $I_O$ | Output Current | 2 | 4 | mA |
| $IR_{PD}$ | Internal Pull-Down Resistor current | 11 | 43 | µA |
| $IR_{PU}$ | Internal Pull-Up Resistor current | 11 | 44 | µA |
| $R_{PU}$ | Internal Pull-Up Resistor | 13 | 45 | kΩ |
| $R_{PD}$ | Internal Pull-Down Resistor | 13.6 | 45 | kΩ |

a. VGPIO=1.8V (See VGPIO.)

# 3.3 3GPP Power Saving Features

This section describes 3GPP power saving features (PSM, eDRX) that are supported by the HL781x module. Per 3GPP specifications, these features pertain to the module's cellular communication.

The HL781x also features low power modes that contribute to power savings by selectively limiting or turning off other elements of the module, such as memory states, I/O states, etc. (For details, see HL781x Low Power Modes.)

## 3.3.1 Power Saving Mode (PSM)

Power Saving Mode (PSM) is a 3GPP feature that allows the HL781x to minimize power consumption by registering on a PSM-supporting LTE network and then entering PSM state for a configured duration.

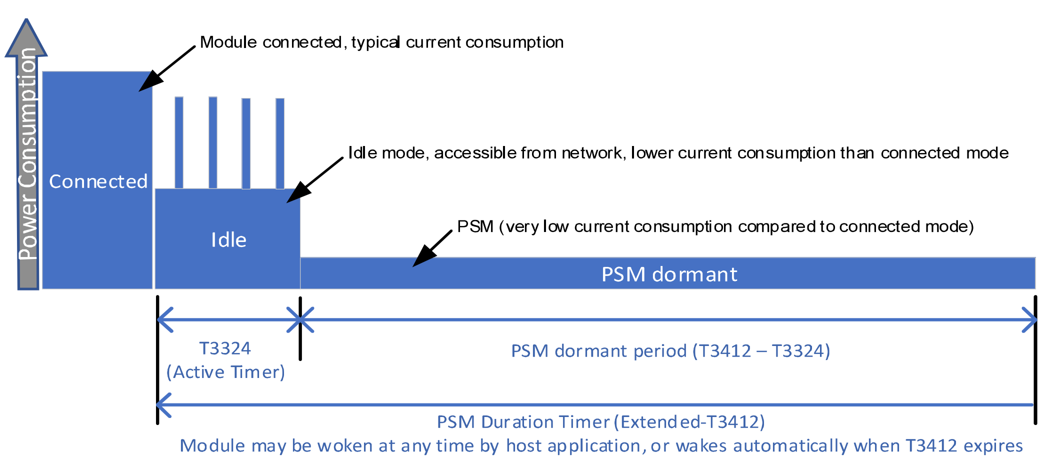


*Figure 3-1: PSM—Timers*

When the module enters the PSM state:

1. The module remains active (accessible from the network) in a lower-power idle state for a short period (T3324 Active Timer).
2. The module then drops to a very-low power 'dormant' state for the remainder of the PSM duration or until the host platform wakes the module to initiate a network contact. During this dormant period, the module is not accessible from the network.
3. After the module contacts the network (for either reason), the process repeats.

Using PSM, an HL781x-based host platform can reduce power consumption significantly because:

- It can enter a very low power state (~1.8 µA) during a very long PSM dormant period.
- The platform can wake the HL781x at any time to initiate data transaction immediately with minimal overhead (signaling/procedure) since the network keeps the module registered during the entire PSM period.

Typical candidates for PSM are systems (such as monitors and sensors) that:

- Require long battery life (low power consumption)
- Infrequently send mobile originated data (every few hours, days, weeks, etc.), with optional reply data from the network
- Tolerate modules being inaccessible for long periods of time
- Do not use mobile-terminated voice/data/SMS. If the host platform needs the module to be able to receive mobile-terminated data, eDRX is a more suitable option.

Figure 3-2 describes an example of a module operating in PSM. In a typical application, the module will always be woken from the dormant state to transmit data (illustrated in the 'Typical MO Use Case' portion of the figure). This is accomplished by setting the T3412 timer much longer than anticipated transmission frequency.

However, if the module is not woken by the host, a TAU will be sent when T3412 expires (illustrated in the 'Default PSM Use Case' portion of the figure). By setting the T3412 longer, unnecessary TAU transmissions can be avoided.

For a more detailed explanation of PSM, refer to ▪ HL78xx Low Power Modes Application Note Reference: 2174229.

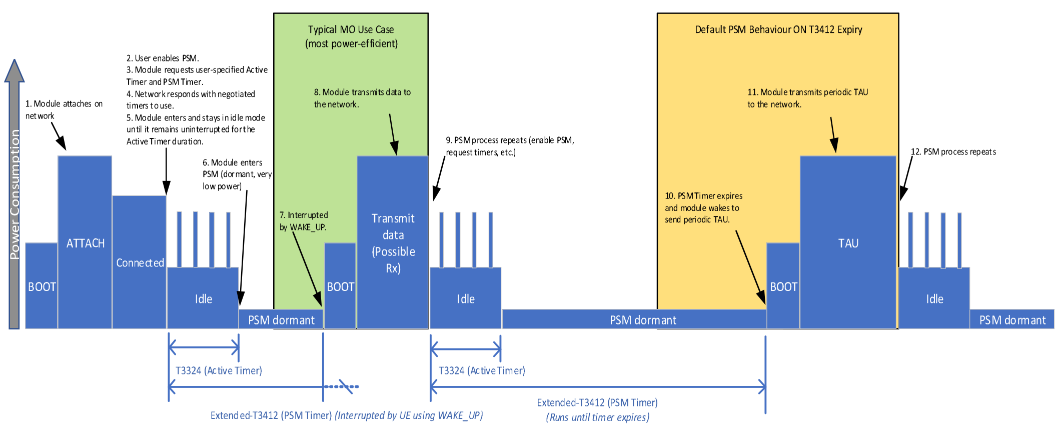


*Figure 3-2: Power Saving Mode—Use Cases Example*

## 3.3.2 Extended DRX (eDRX)

### 3.3.2.1 eDRX Overview

Extended Idle DRX (I-eDRX) is a 3GPP-specified extension of the Discontinuous Reception (DRX) low power consumption feature. This extension reduces the number of paging opportunities (PO) the module must monitor while in idle state, resulting in a corresponding decrease in power consumption.

Many data module applications are tolerant to delays in downlink data packets so extending the period between paging opportunities would allow for current consumption savings for these applications.

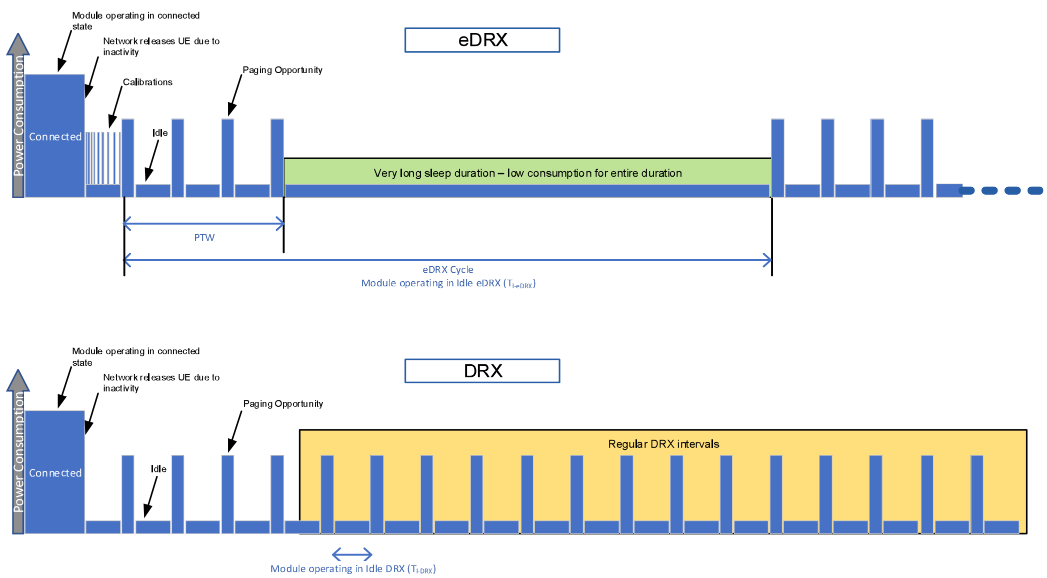


*Figure 3-3: eDRX vs DRX*

As shown in Figure 3-3, the HL7812 supports eDRX, taking advantage of the feature by monitoring a set number of paging opportunities in a Paging Time Window (PTW) and then entering a low power state between PTWs. This sequence (PTW followed by low power state) comprises a single eDRX cycle. The size of the PTW and the length of the eDRX cycle (TI-eDRX) are negotiated between the module (which submits desired values when enabling eDRX) and the network (which indicates the values that will actually be used).

The module remains in I-eDRX until it detects a page from the network during a PO or needs to access the network (e.g. to make a data connection, send a mobility TAU or periodic TAU, etc.), at which time it returns to the connected state.

Note that for a short period of time immediately after the module is released from connected state by the network and enters idle state, it has a few extra short wake ups for clock calibration (shorter than a single PO). Figure 3-4 shows an eDRX power consumption profile with a periodic TAU event. Notice that after the TAU, the eDRX 81.92s cycle is restored slowly by several iterations from 10s to 20s then to 40s before reaching the 81.92s wake. This behavior is an HL781x design feature and cannot be modified.

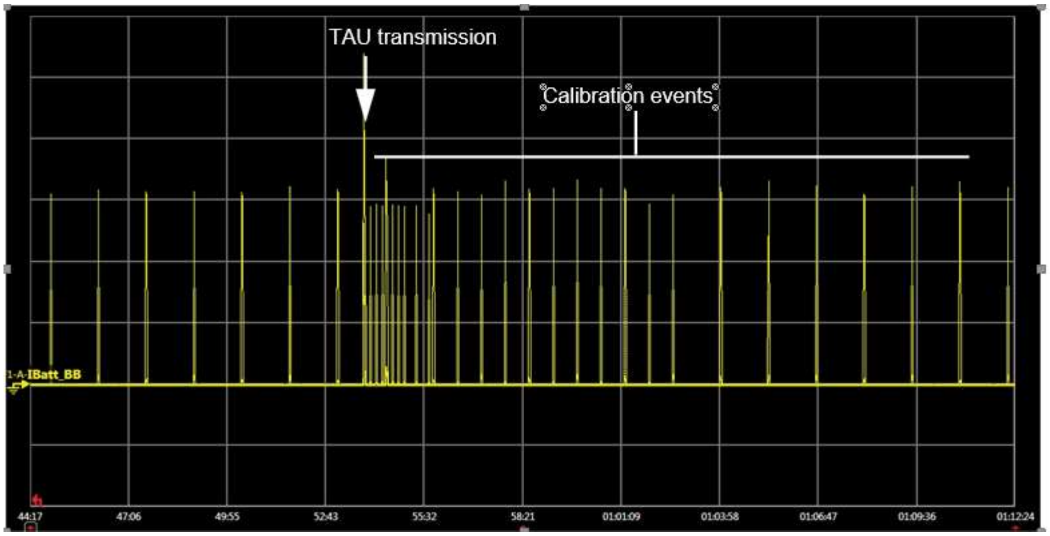


*Figure 3-4: eDRX Power Consumption Profile Interruption*

For a more detailed explanation of eDRX, refer to HL78xx Low Power Modes Application Note.

## 3.3.2.2 Configuring eDRX

Table 3-4 describes available methods for configuring eDRX.

**Table 3-4: eDRX-Related Commands**

| AT Command | Description |
|---|---|
| AT+CEDRXS AT+KEDRXCFG | Enable/disable eDRX and configure related settings |
| AT+CEDRXRDP | Display current eDRX settings |

For example:

- Use AT+CEDRXS to configure the desired TI-eDRX value.
- During the network attach or TAU process:
  - Module sends eDRX request with the settings (as specified in AT+CEDRXS) to the network.
  - Network response indicates if the module may use eDRX and the eDRX parameters that should be used. The network may adjust the eDRX parameters from those requested by the module.
- If eDRX is accepted by the network, the module only needs to monitor during the eDRX paging opportunities. The module may enter low power mode state between the eDRX paging opportunities (depending on the module configuration).

Note that:

- eDRX parameters must be carefully selected to match the intended use case(s) for the module.
  - Given that the module can only be paged at an eDRX paging opportunity:
  - Longer eDRX cycles will delay (increase the latency of) mobile terminated data reception.
  - Shorter eDRX cycles will reduce the latency but will also reduce the eDRX power savings.
  - Setting a cycle longer than 81.92s may not improve power saving significantly, since the module will wake every 81.92s to do a clock calibration.

  The duration of the eDRX cycle should be appropriately selected for the specific use case.

- Network-side store and forward is supported— Packets will be stored until the module's next eDRX paging opportunity or, if the network has a storage time limit, until that limit is reached.

### 3.3.2.3 Concurrent PSM and eDRX

eDRX may be performed during the Active Timer (T3324) window of PSM. For example, if PSM and eDRX are configured with the following settings:

- PSM:
  - T3412 (PSM Timer)— 86400s (24 hours)
  - T3324 (Active Timer)— 327.68s (~5.5 minutes)
- eDRX:
  - eDRX cycle time— 81.92s

Assuming the network does not attempt to contact the module after the module leaves the connected state and enters PSM idle state, the module will stay in the idle state for

327.68 seconds (the Active Timer).

While in the idle state, the module will be in eDRX power saving mode for 4 cycles of

81.92 seconds each, and then go to PSM dormant state for ~23h55m until the T3412 timer expires. At that point the module wakes, sends a periodic TAU, and then the PSM process repeats.

## 3.4 HL781x Low Power Modes

In addition to the 3GPP power saving features Power Saving Mode (PSM) and Extended DRX (eDRX), the HL781x supports the low power modes in Table 3-5.

**Table 3-5: Low Power Modes**

| Power Mode | Possible Modem State | Impact on Module | Hardware Wake-Up Signal Sources |
|---|---|---|---|
| Sleep | Stack OFF, DRX, eDRX, PSM, No service | ▪ 26 MHz system clock is OFF<br>▪ Application processor is idle<br>▪ Modem is out-of-coverage, sleeping, or off<br>▪ I/Os are retained | WAKEUP<br>UART1_DTR[a]<br>RTC alarm event |
| Lite Hibernate | Stack OFF, eDRX, PSM, No service | ▪ 26 MHz system clock is OFF<br>▪ Application processor is OFF<br>▪ Modem is out-of-coverage, sleeping, or off<br>▪ Flash memory and most RAM is off (some retention memory remains on)<br>▪ I/Os are retained | WAKEUP<br>UART1_DTR[a]<br>RTC timeout interrupt |

**Table 3-5: Low Power Modes (Continued)**

| Power Mode | Possible Modem State | Impact on Module | Hardware Wake-Up Signal Sources |
|---|---|---|---|
| Hibernate | Stack OFF, eDRX, PSM, No service | ▪ 26 MHz system clock is OFF<br>▪ Application processor is OFF<br>▪ Modem is OFF<br>▪ Flash memory and most RAM is off (some retention memory may remain on, PSM/eDRX-dependent)<br>▪ I/Os are not retained (e.g. in an undefined state) | WAKEUP<br>RTC timeout interrupt |
| OFF | Stack OFF | ▪ 26 MHz system clock is OFF & RTC clock is OFF<br>▪ Application processor is OFF<br>▪ Modem is OFF<br>▪ Flash memory and RAM off<br>▪ I/Os are not retained (e.g. in an undefined state) | WAKEUP |

a. Only if configured with +KSLEEP <mngt> parameter set to 0

An end product uses the AT+KSLEEP command to specify the preferred lowest power mode. Then when the module sleeps, its power management algorithm determines the appropriate mode based on the module's current operating requirements.

*Note: When a module that is configured for PSM enters Hibernate mode, its non-persistent configurations are lost (just like when it power cycles). Refer to HL78xx AT Commands Interface Guide (Doc# 41111821), Command Timeout and Other Information to identify commands that manage persistent configurations.*

**Warning:** *If USB_VBUS is powered and the USB interface is enabled, it will not be possible to enter Lite Hibernate or Hibernate mode.*

For additional low power mode details (including the relationship between 3GPP power saving features and HL781x power modes), refer to HL78xx Low Power Modes Application Note. For band selection details (which impact power consumption), refer to HL78xx Customization Guide Application Note.

*Note: To prevent flash wear out, the module includes a feature for flash wear out protection. This feature prevents entering Hibernate mode if less than 30 minutes passed since the last Hibernate mode, or less than 30 minutes of Hibernate sleep is expected.*

# 3.5 Current Consumption

This section describes the HL781x module's current consumption under various power states/modes.

- Low Power Current Consumption Modes— Table 3-6 to Table 3-9
- Connected Mode— Table 3-12 to Table 3-16

**Important:** *The module's current consumption will depend on the actual operating / environmental conditions of the customer platform. The current consumption measurements presented in this section (Table 3-6 to Table 3-16) are typical values obtained under the following test conditions:*

- *Nominal supply voltage — 3.7V, TX power — 0 dBm*
- *Nominal ambient temperature — 25 °C*
- *PSM connect type (call box equipment setting) — test mode*
- *eDRX test conditions:*
  - *Cat-M1 eDRX paging cycle — 1.28 sec*
  - *Cat-NB eDRX paging cycle — 2.56 sec*
- *Conducted 50Ω load on RF port(s)*
- *External UICC / USIM that can be activated*

- *In addition, the following conditions apply to Hibernate and OFF mode measurements:*
  - *VGPIO is OFF*
  - *Customer platform ensures module I/Os are **not** driven > 0.2V*
  - *External UICC / USIM that is pre-configured to allow the module to automatically disable the USIM power.*
  
    *(See [4] HL78xx Low Power Modes Application Note (Doc# 2174229) for details.)*
  - *WAKEUP signal Low*

*For detailed low power current consumption information, refer to the HL78xx Low Power Modes Application Note.*

*Note: To be able to enter PSM mode when the module's lowest attainable power state is Lite Hibernate or Hibernate (i.e., +KSLEEP <level> is 1 or 2) and LwM2M is enabled (AutoConnect is enabled by default), the host must not de-assert the WAKEUP pin until it receives a CEREG:4 unsolicited result code.*

### Table 3-6: HL7810 LPM Current Consumption - Cat-M1[a]

| Modem Radio State | Lowest Power Mode | Details | Typ | Unit |
|---|---|---|---|---|
| OFF | OFF | ▪ Module is switched off by AT command (+CPWROFF)<br>▪ Power supplies (VBAT_BB, VBAT_RF) are connected | 2.8 | µA |
| PSM | | TAU—Occurrence is network dependent | 41 | µAh |
| | Hibernate | Floor current during PSM dormant | 2.8 | µA |
| | Lite Hibernate | | 31[b] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 24h<br>▪ T3324 = 20s | 10 | µA |
| | Lite Hibernate Cycle[c] | | 36[d] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 1h<br>▪ T3324 = 20s | 95 | µA |
| | Lite Hibernate Cycle[c] | | 90[d] | µA |
| eDRX[e] | | Calibration—Applies to eDRX 81.92s and longer | 3 | µAh |
| | Hibernate | Floor current during eDRX | 27[b] | µA |
| | Lite Hibernate | | 29[b] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s<br>▪ PTW and DRX = 1.28s | 41[f] | µA |
| | Lite Hibernate Cycle[c] | | 42[f] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s<br>▪ PTW and DRX = 1.28s | 90[f] | µA |
| | Lite Hibernate Cycle[c] | | 93[f] | µA |
| DRX | Sleep | 1.28s | 3 | mA |
| | Hibernate | | 2 | mA |
| | Sleep | 2.56s | 2.5 | mA |
| | Hibernate | | 1.3 | mA |
| | Running | DRX independent, +KSLEEP=2 or Wake active | 40 | mA |
| Standby | | Module registered, Idle mode, without TX power/data transfer | 15 | mA |

a. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario

b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode will from 15µA to 50µA based on chip-set variation distribution.

c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep

d. Values are floor current and T3324-dependent

e. See Extended DRX (eDRX) for details.

f. Values are floor current, PTW and DRX-dependent. Values will have some difference due to a number of active cycles being sampled.

**Table 3-7: HL7812 LPM Current Consumption - Cat-M1[a]**

| Modem Radio State | Lowest Power Mode | Details | Typ | Unit |
|---|---|---|---|---|
| OFF | OFF | ▪ Module is switched off by AT command and VBATs are connected<br>▪ Power supplies (VBAT_BB, VBAT_RF) are connected | 1.8 | µA |
| PSM | | TAU—Occurrence is network dependent | 43 | µAh |
| | Hibernate | Floor current during PSM dormant | 1.8 | µA |
| | Lite Hibernate | | 30[b] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 24h<br>▪ T3324 = 20s | 8 | µA |
| | Lite Hibernate Cycle[c] | | 33[d] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 1h<br>▪ T3324 = 20s | 85 | µA |
| | Lite Hibernate Cycle[c] | | 90[d] | µA |
| eDRX[e] | | Calibration—Applies to eDRX 81.92s and longer | 3 | µAh |
| | Hibernate | Floor current during eDRX | 30[b] | µA |
| | Lite Hibernate | | 32[b] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s<br>▪ PTW and DRX = 1.28s | 50[f] | µA |
| | Lite Hibernate Cycle[c] | | 52[f] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s<br>▪ PTW and DRX = 1.28s | 100[f] | µA |
| | Lite Hibernate Cycle[c] | | 110[f] | µA |
| DRX | Sleep | 1.28s | 3 | mA |
| | Hibernate | | 2 | mA |
| | Sleep | 2.56s | 2.5 | mA |
| | Hibernate | | 1.3 | mA |
| | Running | DRX independent, +KSLEEP=2 or Wake active | 40 | mA |
| Standby | | Module registered, Idle mode, without TX power/data transfer | 15 | mA |

a. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario

b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.

c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep

d. Values are floor current and T3324-dependent.

e. See Extended DRX (eDRX) for details.

f. Values are floor current, PTW and DRX-dependent. Values will have some difference due to a number of active cycles being sampled.

### Table 3-8: HL7810 LPM Current Consumption - NB[a]

| Modem Radio State | Lowest Power Mode | Details | Typ | Unit |
|---|---|---|---|---|
| OFF | OFF | ▪ Module is switched off by AT command.<br>▪ Power supplies (VBAT_BB, VBAT_RF) are connected. | 2.8 | µA |
| PSM | | TAU—Occurrence is network dependent | 43 | µAh |
| | Hibernate | Floor current during PSM dormant | 2.8 | µA |
| | Lite Hibernate | | 31[b] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 24h<br>▪ T3324 = 20s | 12 | µA |
| | Lite Hibernate Cycle[c] | | 33[d] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 1h<br>▪ T3324 = 20s | 120 | µA |
| | Lite Hibernate Cycle[c] | | 115[d] | µA |
| eDRX[e] | | Calibration—Applies to eDRX 81.92s and longer | 4 | µAh |
| | Hibernate | Floor current during eDRX | 28[b] | µA |
| | Lite Hibernate | | 32[b] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s<br>▪ PTW and DRX = 2.56s | 70[f] | µA |
| | Lite Hibernate Cycle[c] | | 72[f] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s<br>▪ PTW and DRX = 2.56s | 210[f] | µA |
| | Lite Hibernate Cycle[c] | | 212[f] | µA |
| DRX | Sleep | 1.28s | 4.5 | mA |
| | Hibernate | | 3.8 | mA |
| | Sleep | 2.56s | 3.5 | mA |
| | Hibernate | | 2.3 | mA |
| | Sleep | 10.24s | 2.5 | mA |
| | Hibernate | | 1 | mA |
| | Running | DRX independent, +KSLEEP=2 or Wake active | 45 | mA |
| Standby | | Module registered, Idle mode, without TX power/data transfer | 15 | mA |

a. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario

b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.
c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep
d. Values are floor current and T3324-dependent.
e. See Extended DRX (eDRX) for details.
f. Values are floor current, PTW and DRX-dependent. Values will have some difference due to a number of active cycles being sampled.

**Table 3-9: HL7812 LPM Current Consumption - Cat-NB[a]**

| Modem Radio State | Lowest Power Mode | Details | Typ | Unit |
|---|---|---|---|---|
| OFF | OFF | Module is switched off by AT command and VBATs are connected | 1.8 | µA |
| PSM | Hibernate | Floor current during PSM dormant | 1.8 | µA |
| | Lite Hibernate | | 30[b] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 24h<br>▪ T3324 = 20s | 8 | µA |
| | Lite Hibernate Cycle[c] | | 33[d] | µA |
| | Hibernate Cycle[c] | ▪ T3412 = 1h<br>▪ T3324 = 20s | 117 | µA |
| | Lite Hibernate Cycle[c] | | 120[d] | µA |
| eDRX[e] | | TAU—Occurrence is network dependent | 48 | µAh |
| | | Calibration—Applies to eDRX 81.92s and longer | 4 | µAh |
| | Hibernate | Floor current during eDRX | 30[b] | µA |
| | Lite Hibernate | | 33[b] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s<br>▪ PTW and DRX = 2.56s | 75[f] | µA |
| | Lite Hibernate Cycle[c] | | 80[f] | µA |
| | Hibernate Cycle[c] | ▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s<br>▪ PTW and DRX = 2.56s | 220[f] | µA |
| | Lite Hibernate Cycle[c] | | 227[f] | µA |
| DRX | Sleep | 1.28s | 4.2 | mA |
| | Hibernate | | 3.5 | mA |
| | Sleep | 2.56s | 3.2 | mA |
| | Hibernate | | 2 | mA |
| | Sleep | 10.24s | 2.2 | mA |
| | Hibernate | | 0.6 | mA |
| | Running | DRX independent, +KSLEEP=2 or Wake active | 45 | mA |
| Standby | | Module registered, Idle mode, without TX power/data transfer | 15 | mA |

a. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario

b. The floor current of PSM lite hibernate, eDRX lite hibernate, and eDRX hibernate mode is from 15µA to 50µA based on chipset variation distribution.

c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep

d. Values are floor current and T3324-dependent.

e. See Extended DRX (eDRX) for details.

f. Values are floor current, PTW, and DRX-dependent. Value will have some difference due to a number of active cycles being sampled.

**Table 3-10: NTN NB-IoT (Non-GPS) Current Consumption**

| Modem Radio State | Lowest Power Mode | Details | Current | Unit |
|---|---|---|---|---|
| DRX | Hibernate | 1.28s | TBD | mA |
| PSM | TAU | Occurrence is network-dependent | TBD | µAh |
| | Hibernate | Floor current during PSM dormant | TBD | µA |
| | Hibernate Cycle | ▪ T3412 = 1h<br>▪ T3324 = 20s | TBD | µA |
| eDRX | Calibration | Applies to eDRX 81.92s | TBD | µAh |
| | Hibernate | Floor current during eDRX | TBD | µA |
| | Hibernate Cycle | ▪ eDRX cycle (TI-eDRX) = 81.92s<br>▪ PTW and DRX = 2.56s | TBD | µA |

**Table 3-11: NTN NB-IoT (Dynamic+GNSS) Current Consumption**

<table>
<tr><th>Modem Radio State</th><th>Lowest Power Mode</th><th>Details</th><th colspan="2">Current</th><th>Unit</th></tr>
<tr><td rowspan="3">PSM</td><td>TAU</td><td>Occurrence is network-dependent</td><td>warm start: TBD</td><td>cold start: TBD</td><td>µAh</td></tr>
<tr><td>Hibernate</td><td>Floor current during PSM dormant</td><td>warm start: TBD</td><td>cold start: TBD</td><td>µA</td></tr>
<tr><td>Hibernate Cycle</td><td>▪ T3412 = 1h<br>▪ T3324 = 20s</td><td>warm start: TBD</td><td>cold start: TBD</td><td>µA</td></tr>
<tr><td rowspan="3">eDRX</td><td>Calibration</td><td>Applies to eDRX 81.92s</td><td colspan="2">TBD</td><td>µAh</td></tr>
<tr><td>Hibernate</td><td>Floor current during eDRX</td><td colspan="2">TBD</td><td>µA</td></tr>
<tr><td>Hibernate Cycle</td><td>▪ eDRX cycle (TI-eDRX) = 81.92s<br>▪ PTW and DRX = 2.56s</td><td colspan="2">TBD</td><td>µA</td></tr>
<tr><td>DRX</td><td>Hibernate</td><td>1.28s</td><td colspan="2">TBD</td><td>mA</td></tr>
</table>

**Table 3-12: HL7810 Current Consumption - LTE Cat-M1 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values)[a] |
|---|---|---|---|
| LTE Cat-M1<br>▪ Modem State: Connected<br>▪ 4RB DL at MCS 14 1RB_UL at MCS 15<br>▪ Maximum 3 UL sub-frames and 3 DL sub-frames every 10 ms<br>▪ Transferring UDP payload data rates: concurrent 280 kbps DL + 45 kbps UL | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 200-240 mA |
| | | 0 dBm | 120-190 mA |

a. Ranges reflect variations between band/channel combinations

**Table 3-13: HL7812 Current Consumption — LTE Cat-M1 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values)[a] |
|---|---|---|---|
| LTE Cat-M1<br>▪ Modem State: Connected<br>▪ 4RB DL at MCS 14 1RB_UL at MCS 15<br>▪ Maximum 3 UL sub-frames and 3 DL sub-frames every 10 ms<br>▪ Transferring UDP payload data rates: concurrent 280 kbps DL + 45 kbps UL | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 170-230 mA |
| | | 0 dBm | 120-140 mA |

a. Ranges reflect variations between band/channel combinations

**Table 3-14: HL7810 Current Consumption - LTE NB-1 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values) |
|---|---|---|---|
| NB1 DL peak throughput (27.2kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers downlink: 12 MCS.TBS:13 MCS.TBS:13 | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 110-140 mA |
| | | 0 dBm | 90-125 mA |
| NB1 UL peak throughput (62.5kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers uplink:3 MCS.TBS:13 | | 23 dBm | 120-150 mA |
| | | 0 dBm | 100-130 mA |

**Table 3-15: HL7810 Current Consumption - LTE NB-2 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values) |
| --- | --- | --- | --- |
| NB2 DL peak throughput (127kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers downlink: 12 MCS.TBS:13<br>MCS.TBS:13 | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 150-220 mA |
| | | 0 dBm | 100-170 mA |
| NB2 UL peak throughput (158kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers uplink:3 MCS.TBS:13 | | 23 dBm | 300-360 mA |
| | | 0 dBm | 150-310 mA |

**Table 3-16: HL7812 Current Consumption - LTE NB-1 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values)[a,b] |
| --- | --- | --- | --- |
| NB1 DL peak throughput (27.2kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers downlink: 12<br>MCS.TBS:13 | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 100-110 mA |
| | | 0 dBm | 90-100 mA |
| NB1 UL peak throughput (45.7 kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers uplink: 12<br>MCS.TBS:13 | | 23 dBm | 100-120 mA |
| | | 0 dBm | 80-90 mA |

a. Typical average current values for 1 time slot.
b. Measured at 3.7V, 25°C.

**Table 3-17: HL7812 Current Consumption - LTE NB-2 Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values) |
| --- | --- | --- | --- |
| NB2 DL peak throughput (127kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers downlink: 12 MCS.TBS:13 | 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85 | 23 dBm | 160-190 mA |
| | | 0 dBm | 120-130 mA |
| NB2 UL peak throughput (158kbps)<br>UL Subcarrier spacing: 15KHz<br><br>Subcarriers uplink: 12 MCS.TBS:13 | | 23 dBm | 220-285 mA |
| | | 0 dBm | 150-170 mA |

**Table 3-18: HL7812 Typical Current Consumption - 2G Connected Mode**

| Parameter | Band | Output Power | Avg. Current (Typical Values) |
|---|---|---|---|
| PCL5 | 850/900 MHz | 32.5 dBm | 290 mA |
| PCL19 | | 5 dBm | 130 mA |
| PCL0 | 1800/1900 MHz | 29.5 dBm | 220 mA |
| PCL15 | | 0 dBm | 120 mA |

# 4: Detailed Interface Specifications

This chapter describes the interfaces supported by the HL781x module and provides specific voltage, timing, and circuit recommendations for those interfaces, as appropriate

## 4.1 VGPIO

The VGPIO (GPIO voltage output) 1.8 V supply state is:

- ON (available)— Voltage output is high when module is in Active, Sleep, or Lite Hibernate mode
- OFF (not available)— Voltage output is low when module is in OFF, Reset, or Hibernate mode

VGPIO can be used to:

- Pull-up signals such as I/Os. For additional details, see I/O Behavior in Hibernate Mode.
- Supply LED drivers
- Indicate the module power state
- Control buffering of module I/O (required in Hibernate)

Table 4-1 and Table 4-2 describe the VGPIO supply.

**Table 4-1: VGPIO Pin Description**

| Pad # | Signal Name | I/O[a] | Description |
|---|---|---|---|
| C45 | VGPIO | PO | GPIO voltage supply |

a. Signal direction with respect to the module

Refer to the following table for the electrical characteristics of the VGPIO supply.

**Table 4-2: VGPIO Electrical Characteristics**

| Parameter | | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Voltage level | | 1.75 | 1.8 | 1.85 | V | Applies to Active, Sleep, and Lite Hibernate modes |
| Current capability | Active, Sleep | – | – | 25 | mA | Total current supplied by VGPIO should not exceed 25 mA. |
| | Lite Hibernate | – | – | 1 | mA | |
| Output capacitance | | – | – | 1 | µF | External decoupling capacitance should not exceed 1 µF. |

### 4.1.1 I/O Behavior in Hibernate Mode

The following behaviors apply, only in Hibernate mode, to I/Os that are referenced to VGPIO (i.e. UART, GPIO, Clock, UIM1, Indication, and ADC signal groups— see Table 2-2); they do not apply in Lite Hibernate or Sleep modes.

- VGPIO is OFF (voltage output is low)

*Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate—Isolation Requirements.*

- No I/O should be biased as no internal source exists. The maximum allowed voltage is ±0.2V at any I/O.
- All I/Os that are referenced to VGPIO will be in an undefined state.

The host should ignore all activity on these signals until the module has initialized and reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see Unmanaged POWER_ON_N (Default) and Wakeup from Low Power Modes.

## 4.2 USIM Interface

The HL781x implements a USIM interface that can be used to control either:

- the module's eSIM (internal, embedded SIM—optional and SKU-dependent)
  or
- an external 1.8V USIM (UIM1); 3V USIM is not supported

To associate USIM1 with the eSIM or external USIM, use the AT+KSIMSEL command. For details, refer to HL78xx AT Commands Interface Guide.

### 4.2.1 eSIM Interface

eSIM is an internal interface supporting Sierra Smart Connectivity. For details about using the HL781x's eSIM with Sierra Smart Connectivity, refer to the Ready-to- Connect Module Integration Guide. For additional information on Sierra Smart Connectivity, explore www.sierrawireless.com or contact Semtech.

### 4.2.2 External UIM1 Interface

The USIM1 interface is fully compliant with GSM 11.11 recommendations concerning USIM functions.

Table 4-3 describes the USIM1 interface.

**Table 4-3: UIM1 Pin Description**

| Pad # | Signal Name | I/O[a] | Description | I/O Type |
|---|---|---|---|---|
| C26 | UIM1_VCC | PO | USIM1 Power supply | 1.8V (VGPIO) |
| C27 | UIM1_CLK | O | USIM1 Clock | 1.8V (VGPIO) |
| C28 | UIM1_DATA | I/O | USIM1 Data | 1.8V (VGPIO) |
| C29 | UIM1_RESET | O | USIM1 Reset | 1.8V (VGPIO) |
| C64 | UIM1_DET[b] | I | USIM1 Detection | 1.8V (VGPIO) |

a. Signal direction with respect to the module
b. Buffer is required if UIM_DET1 is powered from host; not required if powered from VGPIO. UIM1_DET can be used as GPIO3 if external SIM is not required.

*Note: UIM1_VCC max output current is 50 mA in Active and Sleep modes, 1 mA in Lite Hibernate, and Off in Hibernate. For UIM1 electrical interface details, see UIM1.*

## 4.2.3 UIM1_DET

UIM1_DET is used to detect the insertion or removal of a USIM in the USIM socket connected to the main USIM interface (UIM1).

When a USIM is:

- Inserted— UIM1_DET is HIGH.
- Removed— UIM1_DET is LOW.

*Note: In Hibernate mode, UIM1_DET is in an undefined state.*

To enable or disable the USIM detect feature, use the AT+KSIMDET command. For details, refer to HL78xx AT Commands Interface Guide.

# 4.3 USB Interface

The HL781x provides a full speed USB 2.0 interface that conforms to the Universal Serial Bus Specification, Revision 2.0. Table 4-4 and Table 4-5 describe the USB interface.

**Table 4-4: USB Pin Description**

| Pad # | Signal Name | I/O[a] | Description |
|---|---|---|---|
| C12 | USB_D- | I/O | USB Data Negative |
| C13 | USB_D+ | I/O | USB Data Positive |
| C16 | USB_VBUS | PI | USB VBUS |

a. Signal direction with respect to the module

**Table 4-5: USB Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Voltage at pins USB_D+ / USB_D- | 3.15 | 3.3 | 3.45 | V |
| USB_VBUS | 4.75 | 5.0 | 5.25 | V |

**Important:** *For USB operation, USB_VBUS is a mandatory connection. The host must ensure USB_VBUS is provided before establishing USB communication. When USB operation is enabled, the lowest power mode supported is Active—the module cannot enter Low Power state. When USB operation is disabled, the lowest power mode supported is Hibernate.*

For USB enumeration timing, refer to Unmanaged POWER_ON_N (Default) and Wakeup from OFF Mode. Simultaneous UART and USB is supported by default, but can be affected by the+KUSBCOMP command. For details, refer to HL78xx AT Commands Interface Guide.

# 4.4 General Purpose Input/Output (GPIO)

The HL781x provides several GPIOs, some of which are multiplexed with other signals, as described in Table 4-6. For electrical specifications, see Table 3-3.

**Table 4-6: GPIO Pin Descriptions**

| Pad # | Signal Name | Alternate Function | Default State[a] | I/O Type |
|---|---|---|---|---|
| C1 | GPIO1 | - | Input Pull-down | 1.8V (VGPIO) |
| C10 | GPIO2 | Alternative default Ring Indicator (Active High Output) | Input Pull-down | 1.8V (VGPIO) |
| C40 | GPIO7 | Module activity indicator | Input Pull-down | 1.8V (VGPIO) |
| C41 | GPIO8 | VBAT_PA_EN (Output) | Input Pull-down | 1.8V (VGPIO) |
| C46 | GPIO6 | Low power monitoring | Input Pull-down | 1.8V (VGPIO) |
| C51 | GPIO14 | UART3_CTS (Output) | Input Pull-down | 1.8V (VGPIO) |

**Table 4-6: GPIO Pin Descriptions (Continued)**

| Pad # | Signal Name | Alternate Function | Default State[a] | I/O Type |
|---|---|---|---|---|
| C52 | GPIO10 | UART3_TX (Input) | Input Pull-down | 1.8V (VGPIO) |
| C53 | GPIO11 | UART3_RTS (Input) | Input Pull-down | 1.8V (VGPIO) |
| C54 | GPIO15 | UART3_RX (Output) | Input Pull-down | 1.8V (VGPIO) |
| C64 | GPIO3 | UIM1_DET (Input) | Input Pull-down | 1.8V (VGPIO) |
| C65 | GPIO4 | - | Input Pull-down | 1.8V (VGPIO) |
| C66 | GPIO5 | - | Input Pull-down | 1.8V (VGPIO) |

a. Default state is software-controlled when module has initialized and reached AT-READY state. Default state is configurable by customer using AT+KGIOCFG command. For details, refer to HL78xx AT Commands Interface Guide (Doc# 41111821).

Table 4-6 notes the default state for each signal. By default, at power up, all GPIOs are configured as inputs. During power up, power down, reset and Hibernate, the signals are in an undefined state. Therefore, the host should ignore all activity on I/Os until the module has reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see Unmanaged POWER_ON_N (Default) and Wake Up Signal (WAKEUP).

## 4.4.1 GPIO7 Usage

The GPIO7 can be set as a module activity indicator via AT commands **AT+KGPIOCFG** or **AT+KGPIO**. For details, see HL78xx AT Command Guide. When set as a module activity indicator, the GPIO7 will indicate High activity once the module is active. Power IC levels can be controlled using GPIO7 to initiate power saving methods. Note that power saving methods may also be affected by the overall hardware schematic design.

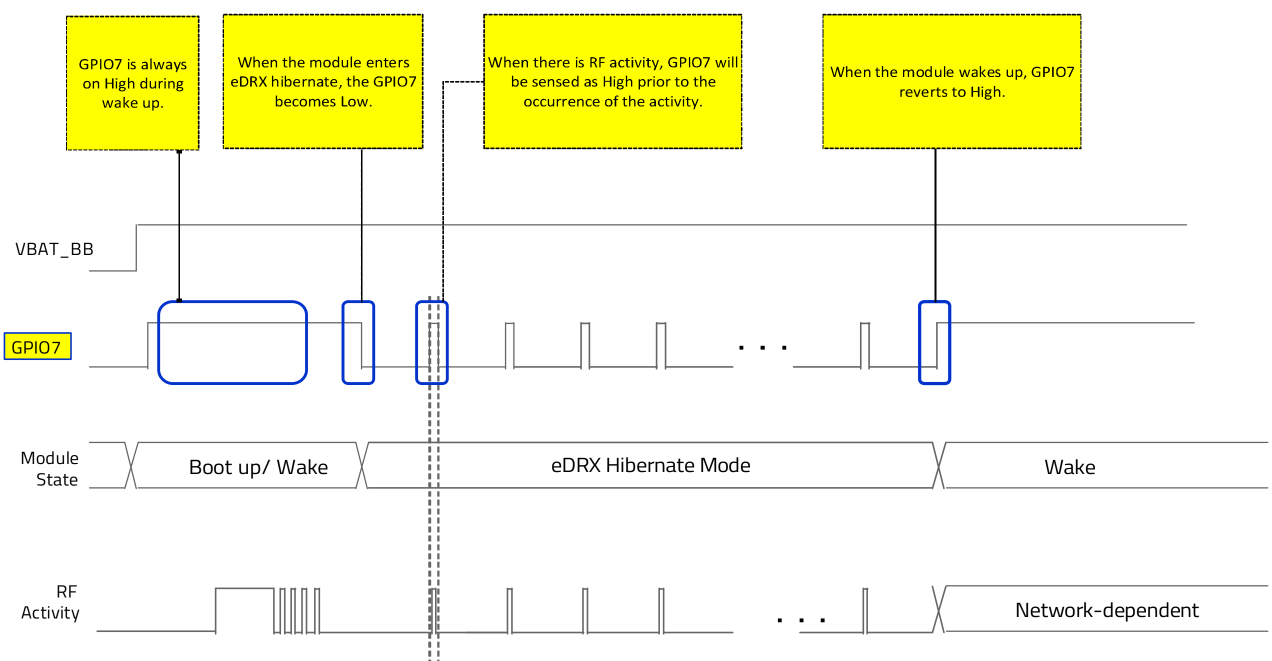


*Figure 4-1: GPIO7 Waveform Behavior*

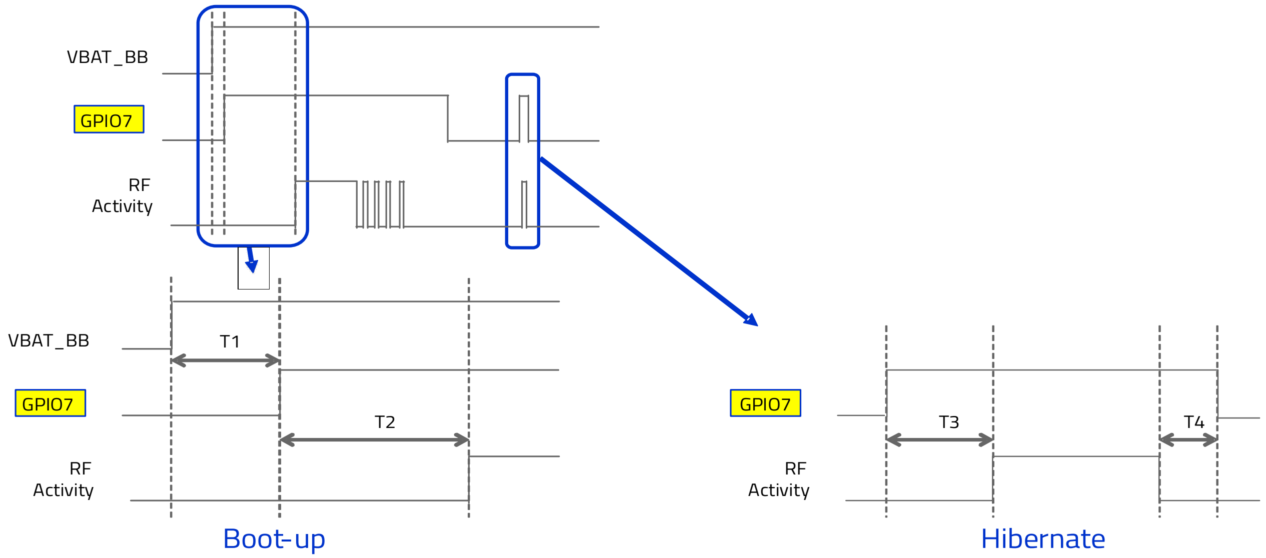


*Figure 4-2: GPIO7 Waveform—Boot up and Hibernate mode*

### Table 4-7: GPIO7 Timing for Boot Up and Hibernate Mode

| Parameter | Description | Min | Max |
|---|---|---|---|
| T1 | Delay between VBAT_BB and GPIO7 | - | 42 ms |
| T2 | Delay between GPIO7 and RF activity | 2.848 sec | 4.5 sec |
| T3_eDRX | Delay between GPIO7 and RF activity under eDRX | 48.8 ms | 79.2 ms |
| T3_PSM | Delay between GPIO7 and RF activity under PSM | 400 ms | 672 ms |
| T4_eDRX | Delay between RF activity and GPIO7 under eDRX | 10.4 ms | 17.76 ms |
| T4_PSM | Delay between RF activity and GPIO7 under PSM (Wake up by TAU) | 4.576 sec | 9.168 sec |

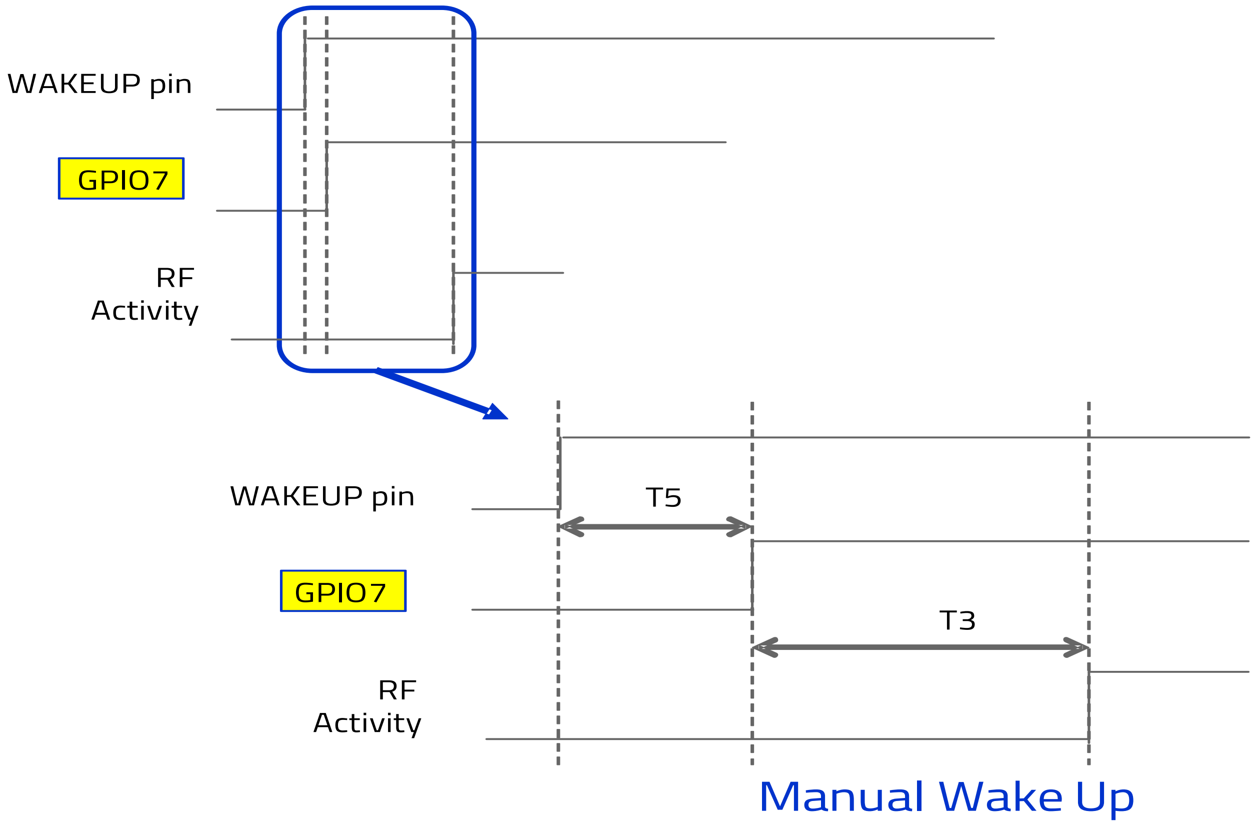


*Figure 4-3: GPIO7 Waveform—Manual Wake Up*

**Table 4-8: GPIO7 Timing for Manual Wake Up**

| Parameter | Description | Min | Max |
|---|---|---|---|
| T5_eDRX | High during wake up state | - | 720 µs |
| T5_PSM | | - | 720 µs |

# 4.5 Main Serial Link (UART1)

The HL781x implements the UART1 serial interface (up to 921.6 kbps, default rate of 115.2 kbps) for communication between the module and a PC or host processor. UART1 consists of a flexible, 8-wire asynchronous serial, 1.8V interface that complies with RS- 232 interface. UART1 can also be used to upgrade the module firmware locally.

Simultaneous UART and USB is supported by default, but can be affected by the +KUSBCOMP command. For details, refer to HL78xx AT Commands Interface Guide.

*Note: The host platform may use UART1 as an 8-wire, 4-wire, or 2-wire interface as shown in Figure 4-4, Figure 4-5, and Figure 4-6.*

Note that in Hibernate mode the host platform (MCU) interfaces can remain powered— it is important that the host interfaces do not back-power the module.

The UART1 interface is not active during Hibernate mode, so the host should ignore all activity on UART1 during Hibernate. If the module will enter Hibernate mode, Semtech recommends adding buffer circuits to ensure UART signals are not driven high (i.e. >0.2V).

Note that a buffer is not required in Lite Hibernate mode. For detailed information, refer to I/O Behavior in Hibernate Mode.

Table 4-9 describes the UART1 interface.

**Table 4-9: UART1 Pin Description**

| Pad # | Signal Name[a] | Default State[b,c] | Active | I/O Type | Description |
|---|---|---|---|---|---|
| C2 | UART1_RI | Output | L | 1.8V (VGPIO) | Ring Indicator<br>Data reception, SMS, etc. |
| C3 | UART1_RTS | Input with pull-down | L | 1.8V (VGPIO) | Request To Send |
| C4 | UART1_CTS | Output | L | 1.8V (VGPIO) | Clear To Send[d]<br>The module is ready to receive AT commands. |
| C5 | UART1_TX | Input with pull-down | - | 1.8V (VGPIO) | Transmit data |
| C6 | UART1_RX | Output | - | 1.8V (VGPIO) | Receive data |
| C7 | UART1_DTR | Input with pull-up | L | 1.8V (VGPIO) | Data Terminal Ready[e] |
| C8 | UART1_DCD | Output | L | 1.8V (VGPIO) | Data Carrier Detect<br>Signal data connection in progress |
| C9 | UART1_DSR | Output | L | 1.8V (VGPIO) | Data Set Ready<br>Signal UART interface is ON |

a. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention—PC view). For example, UART1_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART1_RX is an output from the module to the host.
c. Default state is software-controlled when module has initialized and reached AT-READY state.
d. Host can monitor UART1_CTS and VGPIO to determine when the module is ready to receive AT commands (AT-READY). The UART1 inter- face is not active during Hibernate mode, so the host should ignore all activity on UART1_CTS during Hibernate.
e. UART1_DTR has software-controlled pull-up (PU) (if enabled by using AT+KSLEEP with the <mngt> parameter set to 0), which is active only when module has initialized and reached AT-READY state. When the signal is low, the module wakes in all operational modes except Hibernate. When the signal is high, the module can enter sleep mode or lite hibernate mode but not hibernate mode.

*Note: If possible, it is highly recommended to add 0 on every line on the host platform to help the debug process. This will force the UART signal layout to the top PCB layer and allow access to the signal on the resistors.*

## 4.5.1 Ring Indicator (UART1_RI or Alternative)

UART1_RI is an active-low output signal that indicates incoming events (e.g. SMS, data reception, etc.).

The signal is available in all power modes except Hibernate mode. In Hibernate mode, the UART_RI signal is in an undefined state.

Therefore, if a customer platform requires a RI signal to wake its host processor on SMS or IP reception, an alternative signal must be used.

The AT+KRIC command can configure GPIO2 (by default) as an inverted RI signal (RI_inverse_gpio). (For details, refer to HL78xx AT Commands Interface Guide (Doc# 41111821) and HL78xx Low Power Modes Application Note (Doc# 2174229)).

*Note: Because GPIO2 is in an undefined state while in (and exiting) Hibernate, use the following recommendations when GPIO2 is used as an RI signal: If firmware is used, enable the internal PD on GPIO2 using AT+KRIC (default state is No Pull).*

## 4.5.2 UART1_RTS/UART1_CTS

UART1_RTS (Request to Send) is an active-low input signal used for module flow control (in combination with UART1_CTS).

By default, the UART1_RTS signal state is software-controlled as pull-down, and the host platform must drive this signal. The signal can be configured as a pull-up using the AT+KHWIOCFG command (minimum firmware version 4.6.8)— for details, refer to HL78xx AT Commands Interface Guide (Doc# 41111821)

For detailed UART1 flow control information (including use of UART1_RTS and UART1_CTS), refer to HL78xx Low Power Modes Application Note (Doc# 2174229)).

## 4.5.3 UART Application Examples

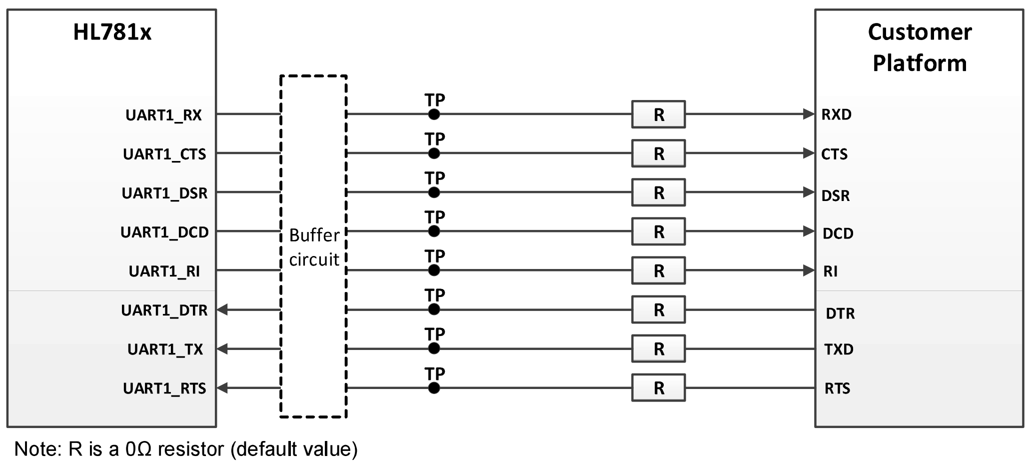


*Figure 4-4: 8-wire UART Application Example*

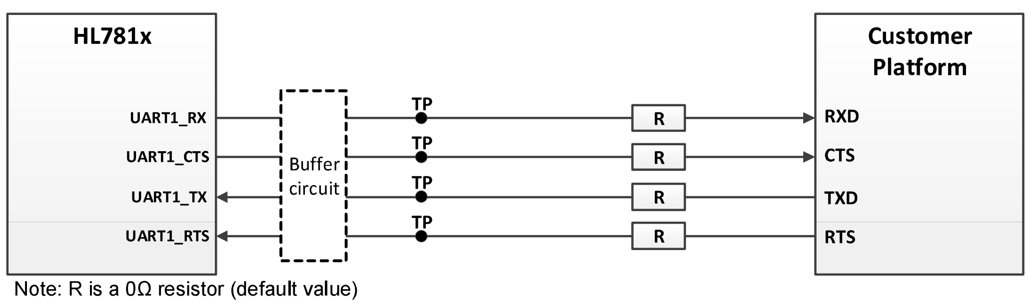


*Figure 4-5: 4-wire UART Application Example*

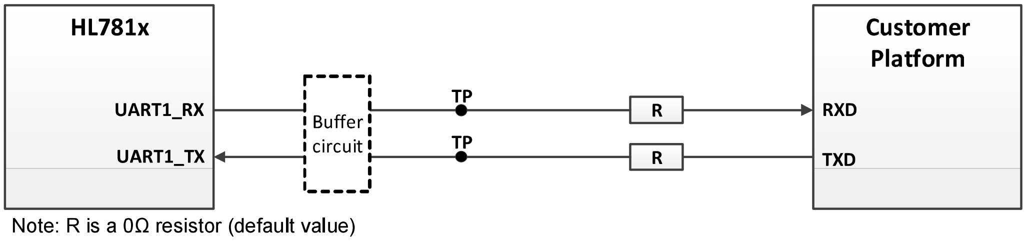


*Figure 4-6: 2-wire UART Application Example*

*Note: All UART signals operate at 1.8V. A voltage level shifter is required when connecting to a 3V3 domain.*

# 4.6 Power On Signal (POWER_ON_N)

The POWER_ON_N hardware control signal can be used by the host platform to turn the module on.

The signal is internally biased high by default. Bias voltage is dependent on the module mode— 1.3–1.4V in Active or Sleep mode, and 1.1–1.2V in Hibernate or Lite Hibernate mode.

The module has two possible operational modes— Host-managed and unmanaged:

- Unmanaged (default configuration)— The module starts regardless of the POWER_ON_N state. In this mode, the POWER_ON_N signal must be left open.

*Note: If RESET_IN_N is low, the module will not start until RESET_IN_N is released.*

- Host-Managed— A low-level pulse must be provided by the host to switch the module ON. Use an open drain/ open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))).

Table 4-10 and Table 4-11 describe the POWER_ON_N signal.

**Table 4-10: POWER_ON_N Pin Description**

| Pad # | Signal Name | I/O[a] | Description |
|---|---|---|---|
| C59 | POWER_ON_N[b] | I | Powers the module ON |

a. Signal direction with respect to the module
b. Signal provided by host. Does not need to be buffered, and can be directly connected to module using an open drain/collector type circuit.

**Table 4-11: POWER_ON_N Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input Voltage-Low (v) | – | – | 0.3 | V |

To ensure safe power on, the module VBAT (VBAT_BB/VBAT_RF) must be discharged below 0.3V before re-applying VBAT power.

# 4.6.1 Unmanaged POWER_ON_N (Default)

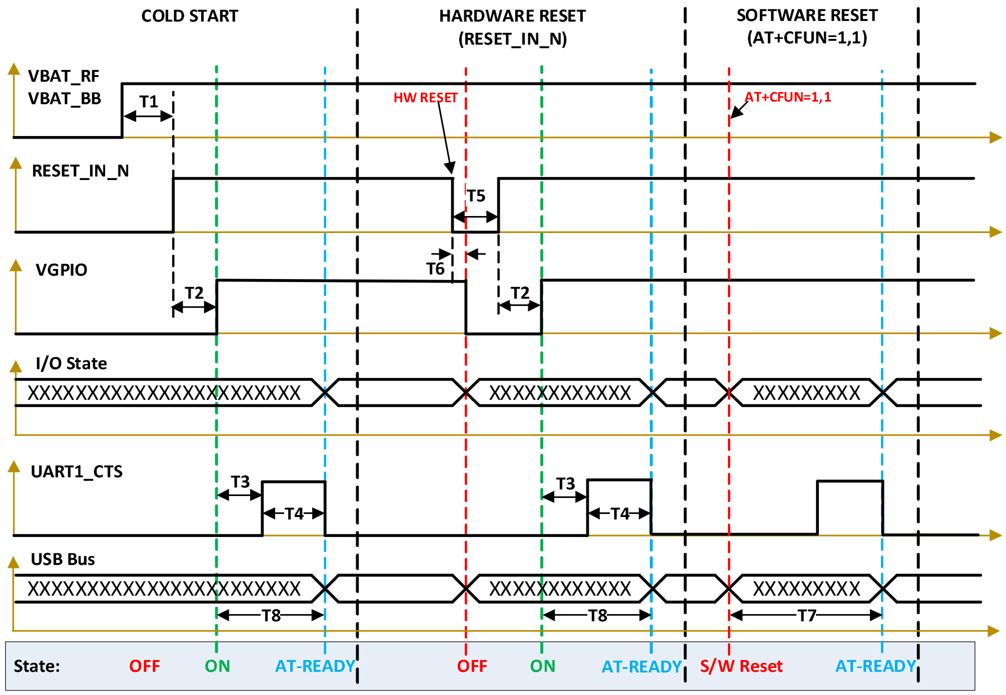


*Figure 4-7: Power On and Reset Sequence (unmanaged POWER_ON_N)*

**Important:** *At completion of T4/T8/T7, the module is ready to receive AT commands ('AT-READY') via UART1 or USB.*

**Table 4-12: POWER_ON_N Timing (unmanaged)[a]**

| Parameter | Min | Typ | Max[b] | Unit |
|---|---|---|---|---|
| T1: Delay between VBAT_BB and RESET_IN_N | – | – | 200 | ms |
| T2: Delay between RESET_IN_N and VGPIO | – | – | 60 | ms |
| T3: Delay between VGPIO and UART1_CTS | – | – | 100 | µs |
| T4: Delay | – | – | 10[c] | s |
| T5: HW RESET_IN_N assertion time | 100 | – | – | µs |
| T6: Off delay between VGPIO and RESET_IN_N | – | – | 30 | µs |
| T7: Delay between software reset and AT-READY (UART/USB) | – | – | 10 | s |
| T8: Delay between VGPIO and USB enumeration | – | – | $T3_{max} + T4_{max}$ | s |

a. Timing of first power cycle after FOTA/FW upgrade is not captured in this table.
b. Measurements taken with HL78xx Development Kit
c. Maximum time may extend to 40 seconds if there is an NV backup restore operation. Maximum time may extend to 20 seconds if the SIM card is unavailable.

# 4.7 Power Down, Off, and VBAT Removal

## 4.7.1 Software Power Off in Unmanaged Mode

To power down the module via software:

1. Initiate the power down process:
   a. Use the +cfun=0 command to stop SIM processes.
   b. Use the +CPWROFF command (For details, refer to HL78xx AT Commands Interface Guide (Doc# 41111821).):
   AT+CPWROFF
   OK
   c. set WAKEUP to low within 0.5 seconds after receiving **OK.**
2. Monitor VGPIO— When VGPIO is low (e.g. < 0.2 V), the module is in OFF mode. (Note— The module can be woken from OFF mode by setting WAKEUP high. For timing details, see Wake Up Signal (WAKEUP)
3. It is now safe to remove power (VBAT_BB and VBAT_RF) from the module.

*Note: While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them—the signals should not be driven high (i.e. > 0.2 V). If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8~1.1 V).*

If the host cannot set WAKEUP to low within 0.5 seconds, power down the module using the following steps instead.

1. Initiate the power down process:

a. Use the AT+KSLEEP=2 command to disable sleep
b. Set WAKEUP to low (De-assert).
c. Use the AT+CFUN=0 command to stop SIM processes.
d. Use the AT+CPWROFF command (For details, refer to HL78xx AT Commands Interface Guide)
AT+CPWROFF
OK

2. Monitor VGPIO— When VGPIO is low (e.g. < 0.2 V), the module is in OFF mode.

(Note— The module can be woken from OFF mode by setting WAKEUP high. For timing details, see Wake Up Signal (WAKEUP)

3. It is now safe to remove power (VBAT_BB and VBAT_RF) from the module.

Note that the +KSLEEP parameters need to change to its original setting after rebooting or else the module cannot go to sleep because sleep is disabled by AT+KSLEEP=2.

## 4.7.2 Emergency Power Removal

The Software Power Off in Unmanaged Mode procedure (which uses AT commands) should be used to safely power down the module.

However, if the module's UART and USB interfaces cannot be accessed, or are unresponsive (i.e. do not respond after an AT command is issued (see Command Timeout appendix in HL78xx AT Commands Interface Guide), the following procedure can be used to power down the module, if necessary.

**Important:** *This procedure should be used with caution. If the module is interrupted while processing certain AT commands or performing a firmware upgrade, or the procedure is not followed correctly, the module may become unusable.*

1. Set RESET_IN_N low, and keep it asserted.
2. Monitor VGPIO- When VGPIO is low (e.g. < 0.2 V), the module is powered down.
3. Remove VBAT (both VBAT_BB and VBAT_RF) power.
4. Monitor VBAT- When VBAT is discharged below 0.3V, de-assert RESET_IN_N.

*Note: :To power up the module, it is critical that VBAT be fully discharged (or below 0.3V) and that RESET_IN_N must be de-asserted. For details, refer to Unmanaged POWER_ON_N (Default).*

While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them-the signals should not be driven high (i.e. > 0.2 V). If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8~1.1 V).

# 4.8 Reset Signal (RESET_IN_N)

The RESET_IN_N hardware control signal can be used to reset the module in any power state.

To reset the module, assert RESET_IN_N low for 100µs (minimum)—this action immediately resets the module. For timing details, see Figure 4-7 (HARDWARE RESET segment).

Use an open drain/open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))),

Do not add a pull-up resistor on this signal as it is internally biased high by default. The bias voltage depends on the module operating state- 1.3-1.4V in Active and Sleep modes, and 1.1-1.2V in Hibernate and Lite Hibernate modes.

*Note: For power-sensitive applications, the module does not reach minimal power consumption when held in reset. Therefore, it is not recommended to hold the module in reset state for long periods.*

**Warning:** *RESET_IN_N should only be used to reset the module if it is unresponsive to AT commands and a power cycle cannot be performed. If used inappropriately (e.g. to reset during a firmware upgrade), memory corruption can occur.*

*As an alternative, Semtech recommends implementing a software reset using AT+CFUN=1,1. For details, refer to the HL78xx AT Commands Interface Guide.*

**Warning:** *During a module reset:*
- *All I/Os will be in an undefined state.*
- *I/Os must not be driven high (over 0.2 V), otherwise the module may be damaged*
- *RESET_IN_N must not be set low during a power cycle, otherwise the module will not boot.*
- *VBAT_BB must always be >3.2V when reset is asserted.*

Table 4-13 and Table 4-14 describe the RESET_IN_N signal.

**Table 4-13: RESET_IN_N Pin Description**

| Pad # | Signal Name | I/O[a] | Active | Description |
|---|---|---|---|---|
| C11 | RESET_IN_N[b] | I | L | Reset signal |

a. Signal direction with respect to the module.
b. Signal provided by host. Does not need to be buffered, and can be directly connected to module using an open drain/collector type circuit.

Refer to the following table for the electrical characteristics of the RESET_IN_N interface.

**Table 4-14: RESET_IN_N Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input Voltage-Low | – | – | 0.3 | V |
| Reset assertion time | 0.1 | 1 | – | ms |

# 4.9 Analog to Digital Converter (ADC)

The HL781x provides two general purpose ADC signals (ADC0, ADC1). These converters are 12-bit resolution ADCs with voltage range of 0–1.8V.

Typical ADC use is for monitoring external signals. The AT+KADC command is used to read the ADC values. For details, refer to HL78xx AT Commands Interface Guide.