

## RF card block diagram

### Overview

The RF card converts the data coming from the digital card into RF signal and transmits it. In the opposite direction it receives the RF signal coming from the other CPE and converts it to digital signal. Transmit direction: The data coming from the digital card is converted by the *Base band* to analog signals called I/Q. Those signals are modulate with DQPSK modulation to IF signal of 280Mhz carrier by the *IF Modem* . Then the signal is up converted by the *UP/Down convertor* and amplified by the *Power amplifier*. Receive direction: the RF signal coming from the antenna is amplified by the *LNA U1017* and down converted to IF signal ( 280MHz ), then the IF is converted to I/Q signals by the *IF Modem U1012*. Those signals are converts to Data and clock signal, and drives to the Digital card.

### Description

#### *Base band processor U1004*

Receive direction: the Base band receives the I/Q signals coming from the *IF modem* those signals are mixed with BPSK PN disspreading. The PN code length is 11bits with rate of 22MCP, then A/D converters converts the signal to data and clock signals, discrambles the data and send it to the digital card in NRZ data and clock format.

Transmit direction: the Base band accepts the data from the digital card, the data is in Data and clock NRZ format at 2Mbps rate, scrambles it, differentially encodes it as DQPSK, and mixes it with BPSK PN spreading. The PN code is 11bits length with rate of 11MCPS. Those signals called I/Q are transferred to the *IF modem*.

#### *IF MODEM U1012*

Receive direction: the IF receives an IF signal of 280MHz with 17.6 Base band range. Two mixers down converts the IF signal coming from the base band filter SAW. each one is 90° shifted from the other. The Reference frequency is coming from *VCO2* and divide by 2. The two signals then are filtered with LPF and transmit to the *Base band processor*.

Transmit direction: the *IF MODEM* accepts the I/Q signals coming from the *Bases band processor* filters them with LPF filter of 8.8Mhz, up convert the I/Q signals with up converters, which 90° shifted from each other. Then combine them to IF signal.

## *Up/down converter U1019*

Receive direction: the *Up/down converter* accepts the RF signal from the *LNA*, amplify and filter it, then down converts it to IF signal using internal mixer and the frequency coming from *VCO1*.

Transmit direction: the *Up/down converter* accepts the IF signal from the *IF modem* up converts the signal to RF frequency using a mixer and the frequency coming from the *VCO1*. Then filter it and amplify with internal preamplifier.

## *SW/PWA U1028*

The *SW/PWA* is a power amplifier with integrated fast switch. The CPE operates in Half duplex mode, means there is two operations mode, transmit mode and receive mode. The integrated switch used to switch between the power amplifier and the receives signal coming from the antenna. The digital card controls the switch and determines when the CPE is in transmit mode or in receive mode. The power amplifier has a gain of 28db.

## *VCO2 Q1009*

This VCO is used as Fix oscillator. This VCO creates 560MHz frequency with 25ppm accuracy. The *Dual Synthesizer* controls the VCO to achieve the wanted accuracy.

## *VCO1 U1026*

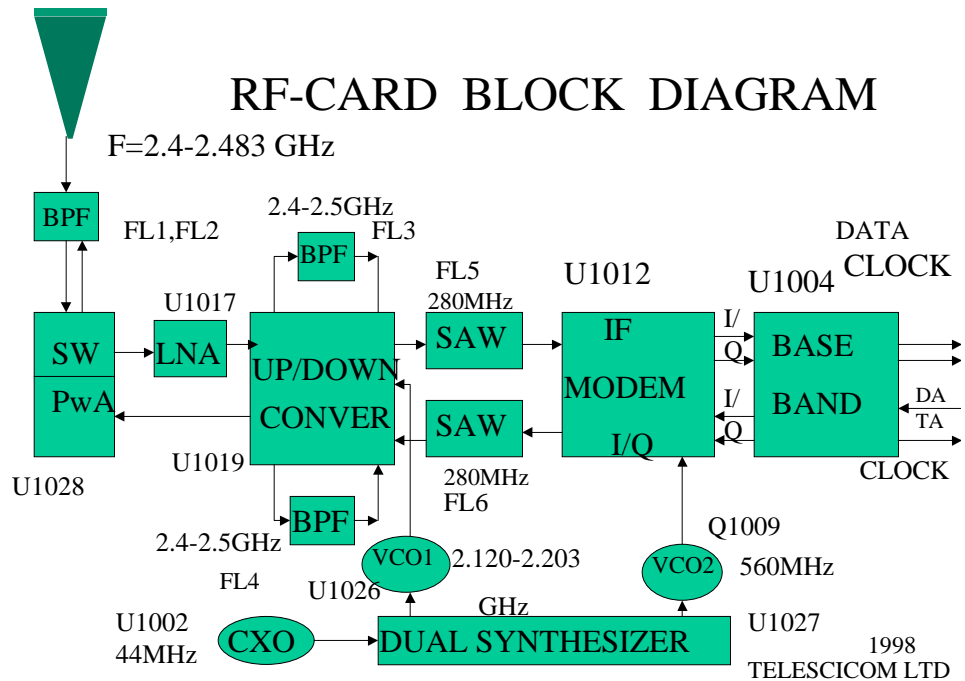
This is a programmable oscillator that used by the *UP/down converter*. The VCO operation range is 2.120Ghz to 2.203Ghz with accuracy of 25ppm. The *Dual Synthesizer* controls the VCO to achieve the wanted accuracy.

## *Dual synthesizer U1027*

The *Dual synthesizer* is phase lock controller. It is used to stabilize *VCO1* and *VCO2*. The *Dual synthesizer* use reference frequency of 44MHz with 25ppm accuracy coming from the crystal oscillator *CXO U1002*.

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## RF-CARD BLOCK DIAGRAM



## Digital card Block diagram

### **Overview**

The digital card drives the Data from the User interface (LAN interface) to the RF card, which modulate and transfer it to the other CPE. In the opposite direction the digital card receives Data from the RF card and drives it to the user interface (LAN interface).

### **Description**

#### *Controller LAN U48:*

The controller LAN U48 receives from J2 (through transformer U51) an Ethernet signal. Decode it and check the destination, if the destination is in the other CPE location than it transfer the Data to NRZ and clock signals and drives it to the Altera U20. In the opposite direction the Controller LAN receives Data from the Altera U20 in NRZ and Clock format transfer it to standard Ethernet signal and transmit the data to the Ethernet interface J2 (through transformer U51) the Data using the CSMA/CD method (Carrier Sense Multiple Access with Collision Detection).

#### *Altera U20:*

The Altera is the main processing engine of the CPE. The Altera gets the Ethernet packet from the Controller LAN, disassembles the packet to the desired length packets add some overhead and Error Code detecting data and keep this Data till it determines to transfer the Data. The determination for transmitting the data is made by logical function between some control signals coming from the RF card, and the control signals coming from J2 (if there is any). In the opposite direction, the Altera gets the Data received from the RF card, reassemble the packets to Ethernet packet and drives the packet to the controller LAN. The Altera has several registers, which are used to get statistical information and determine some operation options, those registers are accessible by the CPU U2.

The Altera is a programmable chip, means there is need for operation program in order to operate properly, the operation program is load by the Setting of Altera block, part of the operating program is load on the Flash U38.

## *CPU U2:*

The CPU load on the Altera the operation program, that store in the ROM chip U12, after loading the operation program the CPE start to function. At continuous mode operation the CPU reads and sets the Altera registers. The CPU has serial port (TXD & RXD) this port is use to communicate with the outside.

## *ROM U12:*

The operation program of the Altera is stored in this chip (also the Boot procedure for the CPU).

## *RAM U13:*

The RAM is used to store temporary data for statistical information.

