FCC ID: N4S201TRANSMITTER

TECHNICAL

DOCUMENTATION

Lectron 20

for

Technologie Lectron

by

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While reasonable precautions have been taken, **Christian Levesque** assumes no responsibility for any errors that may appear in this document.

1.0 SCOPE

This document describes the technical requirements of a radio system used in remote monitoring of gas levels and an in-depth an detailed circuit description of the transmitter and the receiver.

2.0 APPLICABLE DOCUMENTS

The design of the transmitter and receiver described herein has been based on the following governmental certification documents and individual product data sheets.

2.1 GOVERNMENT DOCUMENTS & INDUSTRY STANDARDS

RADIO STANDARDS PROCEDURE	RSP-100-ISSUE 6
LOW POWER RADIOCOMMUNICATION DEVICES	RSS-210-ISSUE 1
FEDERAL COMMUNICATIONS COMMISSIONS	FCC-CFR-47 PART 15

3.0 OPERATIONAL REQUIREMENT DEFINITION

The RF subsystem must meet the following operating requirements:

3.1 Constant stand-by state

The transmitter circuitry must be ready to be activated by the internal timer. Therefore, standby power consumption shall be kept at a minimum since the system will be operational 24 hours a day.

3.2 Low power operation

Being battery operated, the transmitter must consume minimal power while providing guaranteed circuit operation and RF characteristics.

3.3 Programming and expansion capabilities of the receiver

Some of the receiver's key parameters must be programmable over the phone line, thus the micro-controller can reprogram the EEPROM content, i.e., Customer toll-free telephone numbers, Customer ID, tank's identification number, low level setting, actual time and number of tanks handled by receiver. Sufficient memory space shall be reserved for future expansion and eventual expansion.

3.4 Battery related parameters and Micro-wave watchdog timer

The minimal battery-pack discharge cycle, under extreme conditions, shall exceed twelve (12) months. The transmitter shall be able to operate and meet the full specifications with only three (3) Alkaline batteries. Furthermore, the status of the transmitter's batteries being not transmitted, the receiver has to alert the control center of an extend lack of received updates from a specific transmitter.

Periodically, the transmitter shall transmit an encoded signal used by the matched receiver to indicate the local system that the transmitter are alive and well.

3.6 Reliable operation under adverse conditions

- Extended temperature range (-40/C to +85/C).
- Strong EMI fields (conducted and radiated).

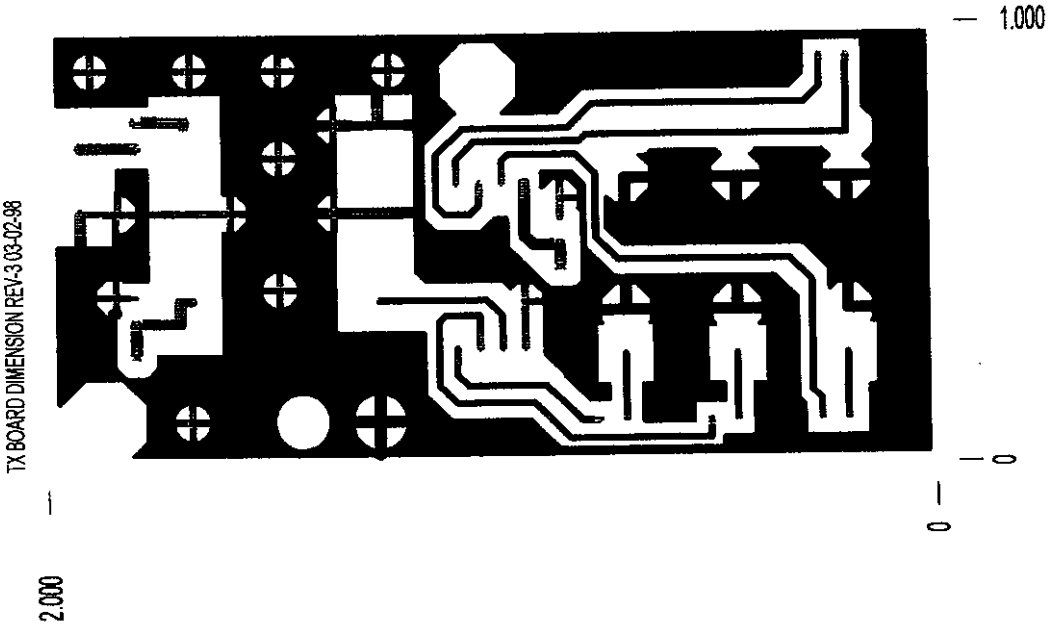
3.7 Operating range

The minimum distance for reliable coverage between the two modules will highly depend on the antenna types and location on the metal tanks. Typical distances should exceed 800 feet.

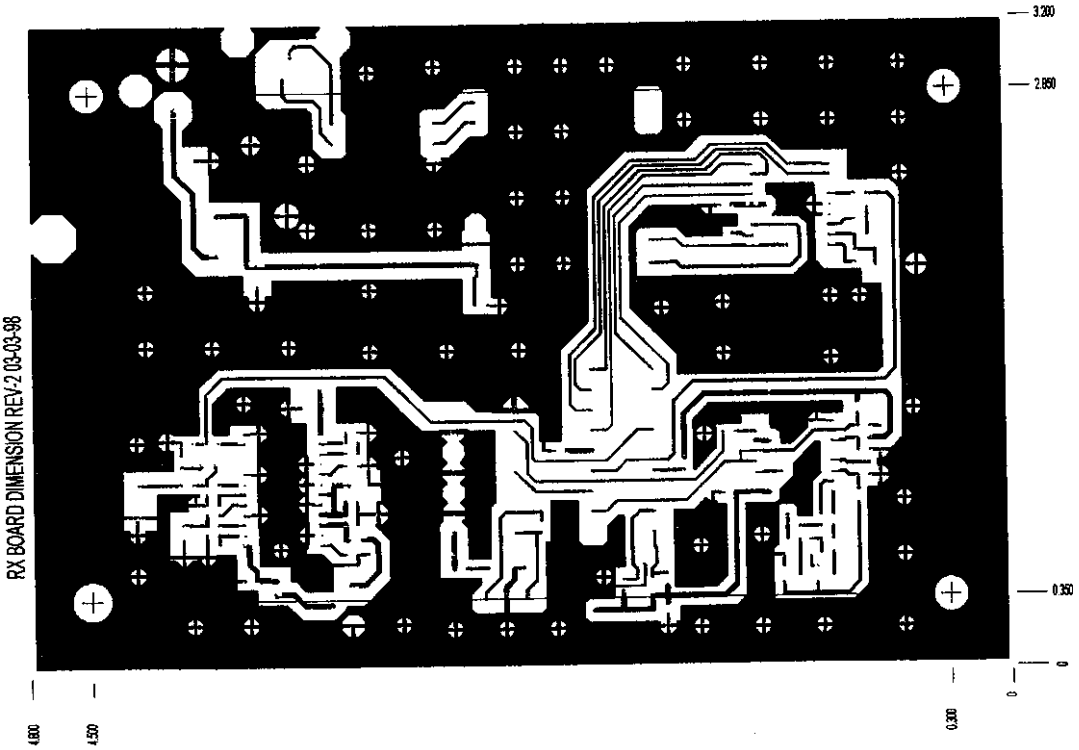
3.8 Small form factor

Without giving any dimensions, it is mandatory that the overall dimensions shall be kept to a minimum. The usage of SMT components is recommended.

The next picture shows the Transmitter's copper view:



The next picture shows the Receiver's copper view:



4.0 RF SUB-SYSTEM SPECIFICATIONS

The transmitter:

Frequency of operation:	315MHz
Field strength:	2.4mV/m @ 3meters (max.) (-27dBm)
Operating voltage:	3.0V to 5.0V
Transmitter peak power consumption:	12mA max.(typ. 8mA)
Transmitter stand-by power consumption:	<20μA
Data rate:	< 2Kbit/s
Input and output impedance:	50Ω
Temperature Range:	-40°C to +85°C

Power Source:	3 Alkaline Batteries

The receiver:

Sensitivity:	-100dBm min.
Operating range:	TBD.
Receiver power consumption:	30mA max.
Interference rejection:	70dB
Input and output impedance:	50Ω
Temperature Range:	0°C to +70°C
Power Source:	Regulated 12Volts from Wall Adaptor

5.0 THEORY OF OPERATION

5.1 PROPAGATION PROPERTIES OF WAVES

It is possible to predict the maximum distance between a transmitter and a receiver in free space, however it is important to know some basic parameters of our communication system, such as: the transmitted power, the antenna gain at both ends and the receiver threshold.

$$P_r = P_t + G_t + G_r - F_{sl}$$

where:

P_r = minimum detectable signal by the receiver in dBm
G_r = receiving antenna gain over isotropic in dBi
P_t = transmitted power in dBm
G_t = transmitting antenna gain over isotropic in dBi
F_{sl} = freespace loss in dB

then

$$F_{sl} = 96.6 + 20\log(\frac{d}{5280}) + 20\log(f)$$

where:

d = distance between transmitting and receiving antennas in foot
f = frequency in GHz

At 300 feet, the FSL would be 61.7dB, so for a system having a -27dBm transmitter, two isotropic antennas (0dB gain) the received signal would be at -88.7dBm. The figure 5.1 illustrate the relation between the FSL and the distance.

In order to relate to the RSS-210 Issue 1 numbers, the field strength at 3m can be converted, by using the two next equations, in transmitted power expressed in watts and in dBm.

$$P_w = \frac{(F_s * d)^2}{30 * G}$$

$$P_{dBm} = 10\log(\frac{P_w}{1 * 10^{-3}})$$

where:

F_s = RMS field strength in mV/m
d = distance in meters
G = gain of transmitter antenna

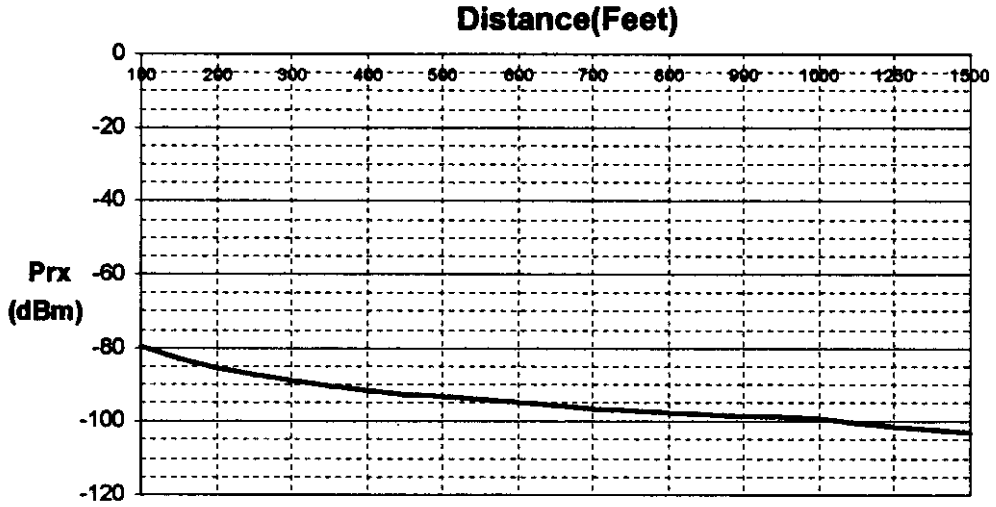


Figure 1: Received Power VS Distance in Feet

With 2.4mV/m of effective radiated power, the equivalent transmitted power is -27dBm is equivalent to 1.73μW radiated by an isotropic radiator in free space. The isotropic radiator or antenna is a hypothetical lossless antenna that radiates uniformly in all directions. To find out how much power is present at a certain distance from the radiator, we have to visualize a sphere with a radius (r) equal to the distance of interest.

The radiated power is evenly distributed on the surface of that sphere, to find out the power density (P_d) on one square meter, we divide the transmitted power (Watts) by the surface of the sphere:

$$P_d = \frac{P_t}{4 * \pi * r^2}$$

At 100m (328 foot) we calculate the power density to be 13.775pW/m^2.

If we double the radius of the sphere, the power density will decrease by a factor of 4, from which we derive the well known rule of thumb: "6dB for every time the distance is doubled or divided by 2".

To convert the power density in field strength, we use the well known expression for power P = E^2/Z_f. E being the field strength and Z_f the impedance of free space:

$$Z_f = \sqrt{(\frac{\mu_0}{e_0})}$$

where:

Z_f = Impedance of free space in S
:$_0$ = permeability of medium (4 * B * 10^{-7} H/m)
e_0 = electric permittivity of medium (10^{-9}/ (36 * B))

The value works out to be 120B or 376.7S. In one sense, an antenna can be considered to be a transformer, transforming the impedance of free space to the impedance of its output terminals.

So the power density calculated previously at 100m turns out to 72μV/m in free space. Finally we need to calculate the induced voltage (Vin) in the receiver antenna, which in the present case, is a loop antenna with a circumference equal to one wavelength at 315MHz.

$$Vin = 2 * \pi * F_s * n * \frac{A}{\lambda}$$

where:

n = number of turns of the loop antenna
A = surface of loop antenna(1λ)
λ = wavelength at frequency

Assuming the antenna is perfectly matched to 50Ω, Vin = 34.3μV_{pp} or -85.3dBm would be present at the input of the low noise amplifier. Then we can perform the reverse calculations to find out the maximum practical distance between the two antennas assuming one isotropic and one loop, which is 5626 feet for a receiver threshold of -110dBm. This number seems pretty good, however, the loop antenna's diameter used in the calculation was 12 inches, other parameters like proximity of the antenna to metallic surfaces will also effect the effective gain of the antenna by 6 to 10dB, distances in the order of 1000 feet are more realistic.

5.2 THE TRANSMITTER

To minimize the power consumption, amplitude modulation with a modulation index of 100% was selected, it is normally called OOK (On-Off Keying), the RF output power being present for a logic "1" and off for a logic "0" according to the 66/33 principle.

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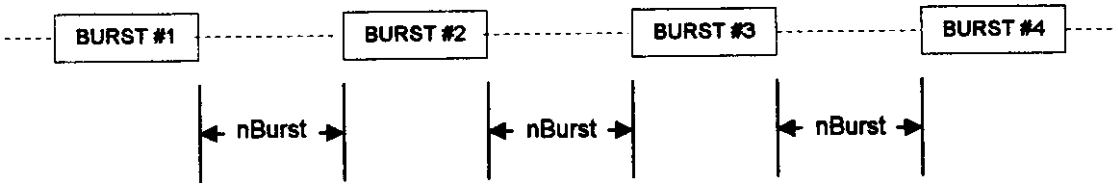
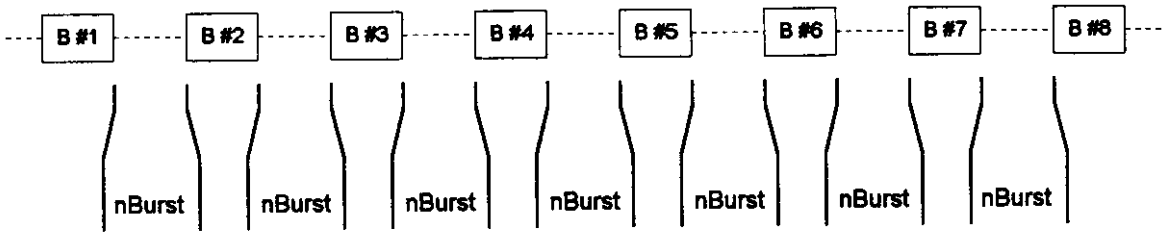
Normal Transmission Session



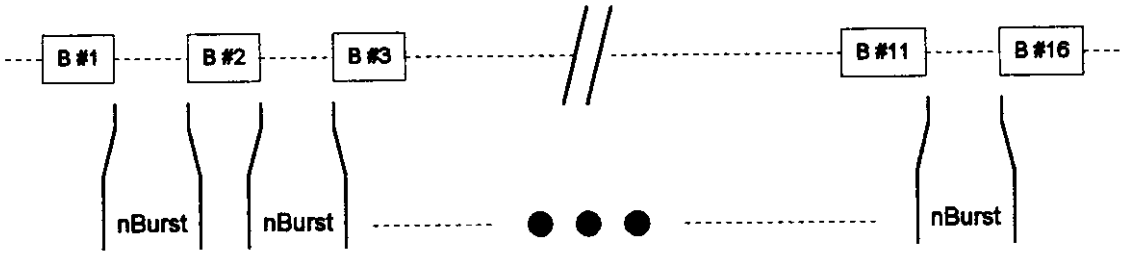
Where n=Integer Between 1 and 32

Low Level Transmission Session



Where n=Integer Between 1 and 32

Power Up Transmission Session



A logic state "1" is asserted when the CPU's GP0 is high, thus turning the RF unit (U9) "ON". The RF unit will transmit as long as the high level is present on the GP0 pin. The Value of L5 will vary with the antenna type and proximity to metallic structures. A loop antenna should offer the best performances since it's near field is govern by the magnetic component of the electromagnetic field.

6.1.2 OPTICAL GAS LEVEL SENSING

The microprocessor U8 does measure the tank's content level by means of three Reflective Optical Sensors LEDA, LEDB and LEDC (OPB745). The diode side of the three sensors are controlled independently by three outputs from the CPU. The following table shows the relations

Access to the telephone network is ensure by an integrated Data Arrangement Module (DAA). On the isolated side, a single chip half duplex modem capable to operate at 300 baud per second. A caller ID decoder is also supported.

An 8bit RISC microprocessor performs the data extraction, transmitter and customer's ID recognition, parity verification and the interface with the modem and caller Id chip. A small amount of EEPROM is also available to store the customer identification number, telephone number, number of tanks and other pertinent information.

A single chip Half Duplex MODEM (U6) and DAA (U7) ensure reliable telecommunication at 300Bauds per second with the remote computer via the standard telephone line. As future option, a called ID IC (U10) is also supported.

6.0 DETAILED CIRCUIT OPERATION

6.1 THE TRANSMITTER BOARD

6.1.1 THE TRANSMITTER CIRCUIT

The controller, U8, an 8bit RISC CPU has 512byte of internal EPROM for program area and an other 25 bytes of RAM data memory. The CPU operates from it's internal 4.00 MHz RC oscillator. The CPU spend most of its time in sleep mode consuming less than 50µA waiting for the watch-dog timer to overflow, thus restarting a communication session. The normal session is composed of 4 burst, the low level burst is sent 8 times while the power up burst is transmitted 16 times, the 2 next figures illustrates the construction of a burst and the three types of communication sessions. The number of times a specific burst is sent does represent a tradeoff between the probability of good reception and the average transmitted power dissipated during one transmission session. In order to preserve the transmitter's batteries, the smaller the average dissipated power.

Status Bits Allocation	
Bit #	Bit Description (7,6,5,4,3,2,1,0)
0(LSB)	Tank Level (LED B)
1	Tank Level (LED A)
2	Tank Level (LED C)
3	Burst Type (00= Normal, 01= Low Level, 10= Installation)
4	Burst Type (00= Normal, 01= Low Level, 10= Installation)
5	Spare
6	Spare
7(MSB)	Spare

Burst Construction

START	SYSTEM ID (16Bits)	CUSTOMER ID (16Bits)	TANK ID (8Bits)	STATUS(8Bits)	STOP

4: α = number of burst
5: $\beta = \alpha - 1$, the number of gaps between bursts.
6: I_{tx} = RF current consumption during a transmission (8mA).
7: I_{active} = current consumption for the CPU only.
8: I_{pd} = sleep mode current (CPU + Leakage).
9: $I_{battery}$ = rated battery capacity, 2.5A/hour

The next table shows the worst-case battery life at different temperatures and for the two types of burst. All currents are maximum values.

BATTERY LIFE IN DAYS (WORST CASE)					
T_{days}	α	I_{active}	I_{pd}	I_{tx}	T (°C)
2073.711	4	1.60E-03	5.00E-05	7.50E-03	85
2075.254	4	4.00E-04	5.00E-05	7.00E-03	25
2075.929	4	2.50E-04	5.00E-05	6.50E-03	-40
2063.742	8	1.60E-03	5.00E-05	7.50E-03	85
2067.127	8	4.00E-04	5.00E-05	7.00E-03	25
2068.509	8	2.50E-04	5.00E-05	6.50E-03	-40

6.2 THE RECEIVER BOARD

6.2.1 Antenna Issues

The coupling of the signal into the TRF1400 device is of paramount importance if the maximum system sensitivity is to be attained. The input network (C16,C17,C18 and L2) provided in the evaluation circuit is designed to match the receiver input to a nominal 50Ωload. A trap to reduce interference from 105-MHz broadcast signals is also included in this network.
The antenna that is used with this receiver should not only be matched to the TRF1400 input impedance, but should also be of an efficient design. A quarter-wave monopole, for example, is a good choice. Loop antennas may also be used, but their performance may vary widely given the available area and proximity to the circuit board. Loop antennas, even those shorter than one wavelength, tend to exhibit distinct nulls in the antenna response pattern as well. If possible, the antenna should be mounted away from the receiver circuit board. Unfortunately, in many instances system requirements do not allow this, and they impose conflicting requirements of space, ease of input matching, and efficiency. If requirements dictate that the antenna be included in a receiver module or other space-restricted area, an antenna that is close to an ideal form should be selected and then examined to determined how it might be integrated into the available space. If this is not possible or not possible without folding the element over the circuit board, the antenna should be swept with a network analyzer to determine the effects of the proximity to the ground plane and other devices. Where possible, the antenna should be trimmed to achieve matching or to approach a region on the Smith Chart where a 1-element match to 50Ω may be achieved. A folded antenna should be kept at least 0.5 inch from the ground plane to avoid excessive sensitivity to mechanical vibration. The design of such an integrated antenna may be empirical, as is often the case in non-ideal situations.

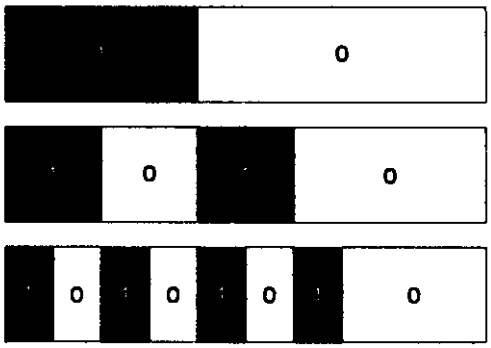
6.2.2 The RF CIRCUIT

The TRF1400 is an integrated Super-regenerative receiver that converts the OOK signal at

between the CPU's outputs and the measured levels.

Sensors/Ports						
Tank	Optical Sensors			CPU Output Ports		
Level	LEDB	LEDA	LEDC	GP2	GP1	GP5
<15%	0	0	0	0	0	0
15%	1	0	0	1	0	0
20%	0	1	0	0	1	0
25%	1	1	0	1	1	0
30%	0	0	1	0	0	1
35%	1	0	1	1	0	1
40%	0	1	1	0	1	1
>45%	1	1	1	1	1	1
1= No Reflected Light (Black), 0= Reflected Light (White)						

The next picture shows the label used to generate the optical patterns.



Optical Label

6.1.2 Expected Battery life

It is possible to evaluate the battery life by using the next equation and by replacing " by 4 and $ by 3 for a normal burst and for an A2B burst " becomes 8 and $ becomes 7.

$$T_{days} = \frac{I_{battery}}{\frac{I_{pd} + I_{tx} * \alpha * \frac{96}{14400e-3} + I_{active} * \beta * \frac{96}{14400e-3}}{24}}$$

To use the previous equation, the following assumptions were made:

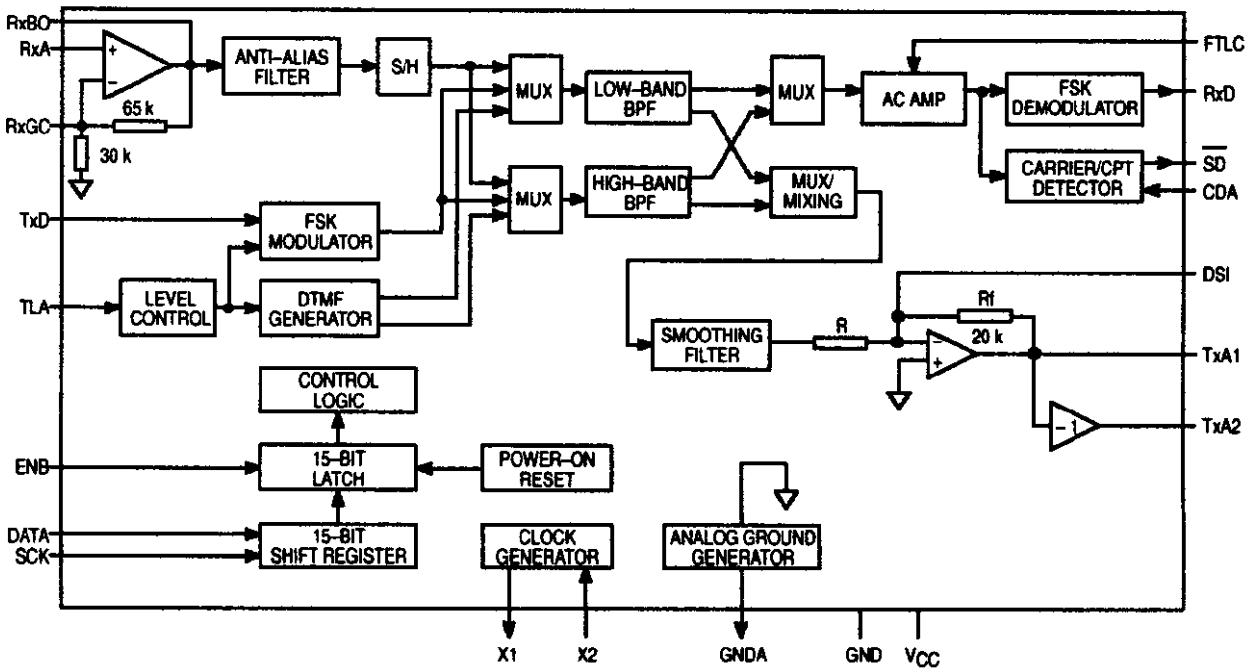
1: At 2kbit/sec. a 48bit burst will last 96ms.
2: The minimum gap between two successive burst is 96ms.
3: The average watch-dog period is 4 hours (14400000ms).

CPU PORT ASSIGNMENT				
CPU PORT	PIN	NET NAME	2nd Function	Main Function
RA0	17	ID_RDY		CALLER ID
RA1	18	/RING		DAA
RA2	1	SCL		EEPROM
RA3	2	SDA		EEPROM
RB0	6	RX_DATA		RF RECEIVER
RB1	7	/OH		DAA
RB2	8	ENB		MODEM
RB3	9	SCK		MODEM
RB4	10	DATA		MODEM
RB5	11	/SD		MODEM
RB6	12	RXD/ID_DATA	CALLER ID	MODEM/CALLER ID
RB7	13	TXD		MODEM

6.2.4 The Modem

Under normal circumstances, the modem should be set in receiving mode only for a pre-defined period of time at power-up (few minutes), otherwise, the transmit mode should be the only active mode when the Caller ID feature is not installed. The "Number to call" will be permanently stored in the EEPROM (U2). It will be possible to change this number remotely during a low-level call. The block diagram is shown in the next figure:

BLOCK DIAGRAM



There is three distinctive telephone call, the first one is the "Power-up" call, the second

315MHz down to a baseband filtered signal.

The RF signal applied to the RFIN1 terminal is amplified by LNA1 and typically passed through an external LC (C20,C21,L3) matching network before being applied to the input of LNA2. The combined gain of the two LNAs is 40 dB, with an input 1-dB compression point of –80 dBm and a noise figure of 5 dB (nominal). The amplified signal is output at RFOUT2 and passed through an external pre-selector bandpass SAW filter (F1) from RFM before being applied to the third stage of amplification at terminal RFIN3. L4-C23 and L1-C9 serves as matching network between the SAW filter and the TRF1400. The third stage of amplification consists of an amplifier with a single-ended input and differential outputs followed by six high-gain differential log-detecting amplifier stages with an equivalent gain of 60 dB (nominal), which forms a detector circuit. First, the signal is converted to a differential signal for increased noise immunity. Next, the differential signal is passed through the six high-gain differential log-detecting amplifiers. Each log-detecting amplifier is biased such that when an RF signal is present, an imbalance is caused in its bias circuit. The imbalance in each of the six stages is converted to a voltage that is then summed into a baseband envelope representation of the RF signal. This signal then passes through an auto-leveling circuit before being applied to a comparator to produce the TTL-level baseband signal output that appears at BBOUT. An external low-pass filter (R6 and C15) connected to BBOUT attenuates high-frequency transients in the output signal. The filtered signal RX_DATA is fed to the CPU U1.

An internal clock (SCLK) is used by the TRF1400 for processing the demodulated incoming data stream and for controlling the Manchester-decoding and timing-recovery logic sections of the device. The frequency of SCLK is set by an external resistor connected between the OSCR and OSCC terminals and an external capacitor connected between OSCC and ground, and is adjustable between 2.5 kHz and 50 kHz. For baseband output, SCLK is set to 5 times the received baseband data rate (500 Hz to 2 kHz). Incoming baseband data is then sampled at 5 times its transmitted data rate. TTL-level baseband data is output at BBOUT whenever the TRF1400 receives ASK-modulated data in any format.
The frequency of the internal clock oscillator is set by connecting a resistor between OSCR and OSCC and a capacitor between OSCC and ground. The following equation defines the oscillator frequency (SCLK speed) as a function of the external resistor and capacitor:

$$Fosc = 1 / (1.386 * ((R4 + R5) + Rs) * (C13 + Cp))$$

Where: (R4+R5) is the external resistor connected between OSCR and OSCC.
Rs is the internal series resistance, typically 1.9 kW or less.
C13 is the external capacitor connected between OSCC and ground.
Cp is parasitic capacitance and is dependent on board layout — typical value is 8.5 pF.

6.2.3 The CPU CIRCUIT

The Clock for the CPU PIC16C58A (U1) is derived from a ceramic resonator (X1) tuned at 3.58MHz. The oscillator circuit (U3) is also used to generate the modem and caller ID circuits. This oscillator is always active. U1 is a single chip RISC micro-controller with 2kbyte of EPROM program space and 72 SRAM data register.

The signal from the RF receiver is connected to the edge detect interrupt input line such that the CPU could spend more time in sleep mode or perform other things. All of the important parameters are stored in an I2C EEPROM memory (U2). The next table shows the port assignment:

at – 44 dBm (typ) for off to on, and – 47 dBm (typ) for on to off. The minimum hysteresis is 2 dB. This pin has a very high input impedance so it should be connected to GND with a 0.1 μF capacitor to keep it well regulated. An external voltage may be applied to this pin to adjust the carrier detect threshold. The following equations may be used to find the CDA voltage required for a given threshold voltage.
V CDA = 245 × V on
V CDA = 347 × V off.

GND Ground Pin (Pin 5)
This pin is normally tied to 0 V.

TLA Transmit Carrier Level Adjust (Pin 6)
This pin is used to adjust the transmit carrier level that is determined by the value of the resistor (RTLA) connected between this pin and GND. The maximum transmit level is obtained when this pin is connected to GND (RTLA = 0).

X1 Crystal Oscillator Output (Pin 7)
Connecting a 3.579545 MHz ± 0.1% crystal between X1 and X2 will cause the transmit frequencies to be within ± 64 MHz of nominal. X1 is capable of driving several CMOS gates. An external clock may be applied to X2. X1 should then be left open.

X2 Crystal Oscillator Input (Pin 8)
Refer to X1.

SD Carrier/Call Progress Tone Detect (Pin 9)
This pin is the output from the carrier detector or call progress tone detector. This pin works as a carrier detector in the FSK mode and as the call progress tone detector in the CPTD mode. The output goes to a logic low level when the input signal reaches the minimum threshold of the detect level that is adjusted by the CDA voltage. When SD = H, the receive data output (RxD) is clamped high to avoid errors that may occur with loop noise. The SD pin is also clamped high in the other modes except during the power–down mode.

RxD Receive Data Output (Pin 10)
This pin is the receive data output. A high logic level of this pin indicates that the mark carrier frequency has been received, and a low logic level indicates the space carrier frequency has been received.

TxD Transmit Data Input (Pin 11)
This pin is the transmit data input, The mark frequency is generated when this pin is at the logic high level. The space frequency is generated when the pin is at a logic low.

DATA Serial Data Input (Pin 12)
This pin is the 15–bit serial data input. This data deter-mines the mode, DTMF signal, transmit attenuation, carrier detect time, channel, and transmit squelch.

SCK Shift Resister Clock Input (Pin 13)
This pin is the clock input for the 15–bit shift register. Serial data is loaded into the shift register n the rising edge of this clock.

ENB Enable Input (Pin 14)
Data is loaded into the 15–bit shift register when this pin is at a logic low. When this pin transitions from a logic high to low, the data is transferred to the internal latch on the falling edge of ENB. New data loaded into the shift register will not affect the device operation until this pin transitions from high to low.

V CC Positive Power Supply (Pin 15)
This pin is normally tied to the + 5.0 V. A 0.1 μF decoupling capacitor should be used.

SI Driver Summing Input (Pin 16)
This pin is the inverting input of the line driver. An external signal is transmitted through an external series resistor RDSI. The differential gain G DSI = (V TXA1 – V TXA2)/V DSI is deter-mined by the following equation. G DSI = – 2Rf / R DSI , Rf 9 20 kW .DSI should be left open when not used.

TxA2 Inverting Transmit Analog Carrier Output (Pin 17)
This pin is the line driver inverting output. The signal is equal in magnitude, but 180° out of phase with the TxA1 (refer to TxA1).

TxA1 Non–Inverting Transmit Analog Carrier Output (Pin 18)
This pin is the line driver non–inverting output of the FSK and tone transmit analog signals. A + 6 dBm (max) differential output voltage can be obtained by connecting a 1.2 kW load resistor between Tx1 and Tx2. Attention must be set so as not to exceed this level when an external input is added to the DSI pin. A telephone line (600 W) is driven through an external 600 W resistor. In this case, the output level be-comes about half of differential output.

RxA Receive Signal Input (Pin 19)
This pin is the receive signal input. The pin has an input impedance of 50 kW (min).

RxGC Receive Gain Adjust (Pin 20)
This pin is used to adjust the receive buffer gain. To adjust the gain, the signal from the RxBO through a

one is the "Low level" call and the third one is the "Maintenance" call.

6.2.4.1 The Power-up Call

At power-up, at least for the first time, when no customer information is available in the EEPROM and after the installation of all remote transmitters is done. A pre-defined period of time, such as 20 to 30 minutes shall be allowed to the remote transmitters to identify themselves, that includes the necessary time for the technician to perform the installation. Once the period of time is elapsed, the receiver will initiate a call to the service center by means of the pre-programmed telephone in the EEPROM. This call can be made during the installation process during normal business hours.

6.2.4.2 The Low Level Call

Once a remote transmitter detects a low level on it's tank, it triggers the transmission of the low level burst. The receiver will then, according to it's configuration, call the Gas service center. This call will be made after normal business hours, i.e., after 20:00:00hours and before 6:00:00hours in the morning.

6.2.4.3 The Maintenance Call

Once a remote transmitter is powered up again, to change batteries as an example, it will transmit again for 16 bursts, the receiver as to differentiate this sequence from the power up installation session by comparing the ID number previously stored in the EEPROM. The receiver will then, according to it's configuration, call the service center. In the event where a specific remote transmitter does not transmit for extended period of time (maybe half a day or a full day), the receiver will also call the service center to report the malfunction. This call will be made after normal business hours, i.e., after 20:00:00hours and before 6:00:00hours in the morning.

6.2.4.4 The Decision making Process

Once the CPU has decoded and validated two consecutive received bursts, coming from an authorized transmitter, action can be taken. Of course, if a low level situation is detected, the call will be delayed until the OFF business hours.

6.2.4.5 The Modem Chip Pinout

RxBO Receiver Buffer Output (Pin 1)
This pin is the receive buffer output.

FTLC Filter Test (Pin 2)
This pin is a high–impedance filter output. It may be used to check the receive filter. This pin also may be used as a demodulator input. In normal operation, this pin is connected to the GNDA through a 0.1 µF bypass capacitor. This pin handles very small signals so care must be used with the capacitor's wiring

GNDA Analog Ground (Pin 3)
Analog ground is internally biased to (VCC–VSS)/2. It should be tied to ground through a 0.1 µF and 100 µF capacitor.

CDA Carrier Detect Level/CPTD Level Control (Pin 4)
The carrier/call progress tone detect level is programmed with a CDA pin voltage.
When this pin is held open, the CDA voltage is set to 1.2 V with an internal divider. The detect level is set

Transmit Attenuator: Four–bit serial data (A3 – A0) sets up the analog transmit level in the FSK, answer tone, DTMF, analog loopback, and single tone mode. The range of the transmit attenuator is 0 –15 dB in 1 dB steps. The external signal (DSI) is not affected by this attenuator.

Tone Frequency: The DTMF tones or the single tone mode is selected by the 4–bit serial data (T3 – T0).

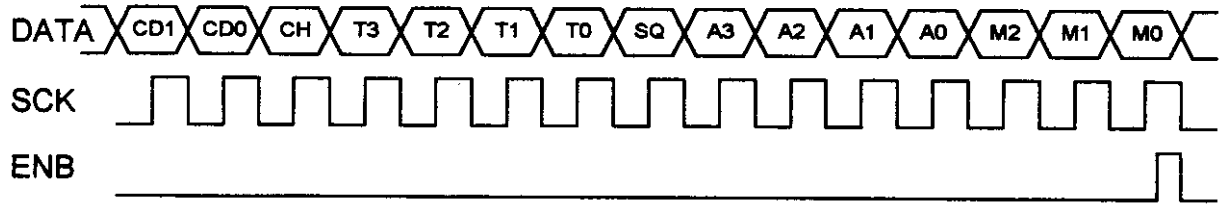
Transmit Attenuator				
A3	A2	A1	A0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

				Tone Frequency (Hz)			
				DTMF Mode			
T3	T2	T1	T0	Low Group	High Group	Keypad	Single Tone Mode
0	0	0	0	941	1633	D	941
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633

divider is added as a feedback. This pin may be held open when the gain adjustment is not needed.

6.2.4.6 The Communication with the Modem Chip

The communication with the Modem is ensure via a three wire serial data port between the CPU (U1). The data has to be sent in a specific format and sequence, please refer to the next figure and tables for specific Modem settings:



Where:

Function Modes				Output		
M1	M2	M3	Function Mode	RxD	SD	TxA1 & TxA2
0	0	0	FSK	Received Digital Signal	Carrier Detect	FSK
0	0	1	Analog Loopback			
0	1	0	CPTD	H	CPTD	VCC/2
0	1	1	Answer Tone	H	H	Answer Tone
1	0	0	DTMF	H	H	DTMF Tone
1	0	1	Single Tone	H	H	Single Tone
1	1	0	Power Down 1	HIGH-Z	HIGH-Z	HIGH-Z
1	1	1	Power Down 2	HIGH-Z	HIGH-Z	HIGH-Z

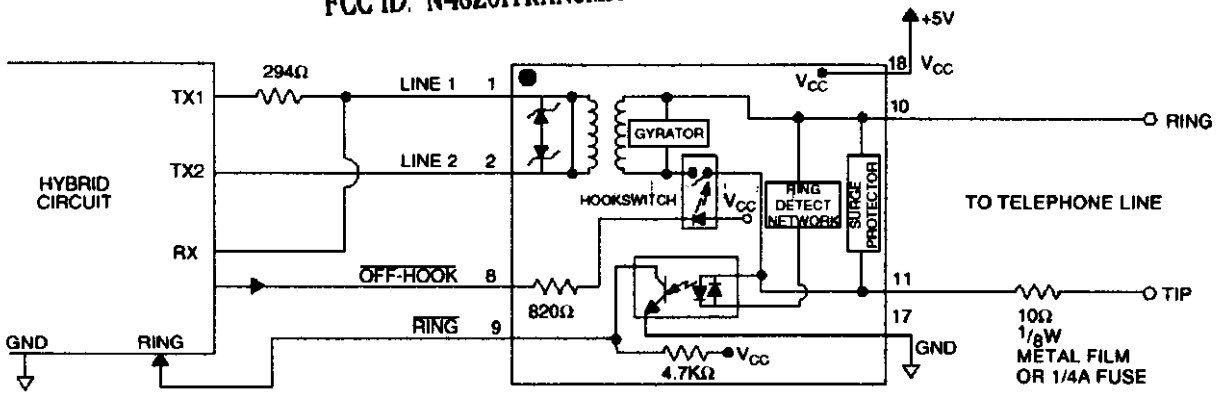
Answer Tone Mode: The transmitter works as 2100 Hz answer tone generator. The receiver is disabled.

DTMF Mode: The transmitter works as a DTMF tone generator. The receiver is disabled.

Single Tone Mode: The transmitter output is one of the DTMF eight frequencies. The receiver is disabled.

Power–Down Mode 1: Internal circuits except the oscillator are disabled, and all outputs except the X1 pin go to the high impedance state. The supply current decreases to 300 mA (max).

Power–Down Mode 2: All circuits including the oscillator stop working and all out-puts go to the high impedance state. The supply current decreases to 1.0 mA (max).



In the previous diagram, the Hybrid circuit is part of the modem chip U6.

6.2.6 Caller ID Feature

This feature is not supported at this time.

7.0 The Wireline Communication Link

The information necessary was not available at the time of redaction, this document will be updated as soon as the information is available.

8.0 The Remote User Interface

The remote software will be described in greater details as soon as it's design has been proven. Boorland C++ will be used for development.

9.0 TEST PROCEDURES

9.1 THE TRANSMITTER

The RF portion of the transmitter is tested with the help of a test software that turns the SAW oscillator on continuously, so we can measure the transmitted frequency and output power. Over the temperature range and with an input voltage variation of 4Volts +/-2Volts, the output frequency shall be between 315MHz +/- 500KHz. The output power shall be between -10dBm and -2dBm.

The remainder portion of transmitter circuitry is tested with the standard operating software. The watch-dog period shall be accelerated to values between 5sec and 12sec.

9.2 THE RECEIVER

A detailed procedure will be included after verification on sufficient units.

10.0 Certification Issues

The bit stream coming from the transmitter has an even distribution of "0" and "1" over an extended period of time, at least 25 burst shall be capture for proper analysis.

1	1	1	1	852	1633	C	1633

SQ	Squelch
0	Disable
1	Enable

CH	Channel
0	2 (Answer)
1	1 (Originate)

CD0	CD1	Carrier Detect Time (Typ)	
		Ton (ms)	Toff (ms)
0	0	450	30
0	1	15	30
1	0	15	15
1	1	80	10

TRANSMIT SQUELCH: The 1–bit serial data (SQ) controls the transmit analog signal. The FSK signal, DTMF tones, single tone, and answer tone are disabled. The external signal to the DSI will be transmitted at that time. The internal line driver works at all times except during the power–down mode.

CHANNEL: The transmit and receive channel is set up with a 1–bit serial data (CH) when the function mode is either in FSK or analog loopback. When the function mode is either on the FSK or analog loopback mode, the transmit and receive channel is set up with a 1–bit serial data (CH).

CARRIER DETECT TIME: The carrier detect time (see Figure 4 and Table 5) is set by 2–bit serial data (CD1, CD0). t on indicates the amount of time the carrier is greater than V on threshold must be present be-fore SD goes low. t off , on the other hand, indicates the amount of delay time SD goes high after the carrier level becomes lower than V off threshold.

POWER–ON RESET: When the power is switched on, this device has the following conditions, Function Mode = FSK, Transmit Attenuator = 0 dB, Transmit Squelch = Enable, Channel = 1 (Originate)

6.2.5 The DAA

The Data Access Arrangement module CYG2000 (U7) does isolate the modem and the other circuitry from the adverse environment of the telephone network. The DAA module integrates the following functions; the Hook-switch, ring detection, gyrator, surge protection and transformer coupling. Please refer to the next figure for interconnection details.

Special softwares will be needed for each of the certification test, however. They are not known at this time.

11.0 LIST OF ACTIVE COMPONENTS

For the transmitter:

U8:	PIC12C508	RISC Micro-controller
U9:	At1003	315MHz RF transmitter

For the receiver:

U1:	24C00T	EPROM
U2:	PIC16C58	RISC Micro-controller
U3:	74HC04	Hex Inverter
U4:	78M05	Voltage Regulator
U5:	TRF1400	RF Receiver
U6:	MC145444	Modem
U7:	CYG2000	DAA
U10:	MC145447	Caller ID

Bill of Material V002

Item Number	Reference Designator	Description	Manufacturer Part Number	Manufacturer	Package	Unit Cost (USD)	Quantity	Total
MULTI-FUNCTION RECEIVER								
SEMICONDUCTORS								
1	U6	Multi-function 300 Bauds Modem	MC145444DW	Motorola	SOIC-20	5.25	1	5.25
2	U7	Data Access Arrangement Module	CYG2000	CP Clare Corp.	Dip	14.95	1	14.95
3	U1	8-Bit RISC CMOS Microcontroller	PIC16C58XAT-4	Microchip	DIP-18	3.03	1	3.03
4	U2	128 Bit I2C Bus Serial EEPROM	24C00T-/OT	Microchip	SOT23-5	0.03	1	0.03
5	U5	RF Telemetry Receiver	TRF1400DWR	TI	SOIC-24	1.85	1	1.85
6	U3	HEX CMOS Flip-flop	74HC04N	TI	DIP-14	0.23	1	0.23
		Sub-Total (USD)					**6**	**20.09**
DISCRETE COMPONENTS								
7	U4	Voltage Regulator, 5V, 500mA	NJM78M05FA-ND	JRC	TO-220F	0.30	1	0.30
		Sub-Total (USD)					**1**	**0.30**
PASSIVE COMPONENTS								
8	F1	315MHz SAW filter	RF1211	RFM	Dip	1.40	1	1.40
9	C6, C25	Aluminium Electro. Capacitor, 16V, 47uF	ECE-A1CKS470	Panasonic	Dip	0.03	2	0.06
10	C5, C7	Tantalum Capacitor, 16V, 1uF, A size	NCT-T-105-16-M-A	NIC	3216	0.11	2	0.22
11	C11, C14	Tantalum Capacitor, 6V, 10uF, A size	NCT-T-106-6-M-A	NIC	3216	0.15	2	0.30
12	C20	Ceramic Capacitor, 3.3pF, 16V	GM010Y5V3R3M25	Murata	0603	0.02	1	0.02
13	C18	Ceramic Capacitor, 3.9pF, 16V	MCH18-2-F-039M	Murata	0603	0.02	1	0.02
14	C3, C4, C21	Ceramic Capacitor, 18pF, 16V	GM010Y5V181M25	Murata	0603	0.02	3	0.05
15	C16, C17	Ceramic Capacitor, 22pF, 16V	GM010Y5V220M25	Murata	0603	0.02	2	0.03
16	C15, C19, C22	Ceramic Capacitor, 100pF, 16V	GM010Y5V101M25	Murata	0603	0.02	3	0.05
17	C13	Ceramic Capacitor, 220pF, 16V	MCH18-2-F-221M	Murata	0603	0.02	1	0.02
18	C10, C29	Ceramic Capacitor, 0.01uF, 16V	GM010Y5V103M25	Murata	0603	0.03	2	0.06

FCC ID: N4S201TRANSMITTER

Bill of Material V002

Item Number	Reference Designator	Description	Manufacturer Part Number	Manufacturer	Package	Unit Cost (USD)	Quantity	Total
			Total (USD)					**29.38**
			Number of Components for the Receiver				**59**	

Caller ID Feature

37	U10	Caler ID Chip	MC145447DW	Motorola	SOIC-16	1.38	1	1.38
38	C32, C33, C38	Ceramic Capacitor, 0.01uF, 16V	GM010Y5V103M25	Murata	0603	0.03	3	0.09
39	C34, C35, C36, C37, C39,	Ceramic Capacitor, 0.1uF, 16V	GM010Y5V104M25	Murata	0805	0.03	5	0.15
40	D1, D2	Dual Diodes	BAV99ZXTR-ND	Zetex	sot-23	0.12	2	0.24
41	R23	Chip Resistor, 270K, 10%, 0603	CR0603J274	CHIPTECH	0603	0.01	1	0.01
42	R18, R19	Chip Resistor, 1K, 10%, 0603	CR0603J102	CHIPTECH	0603	0.01	2	0.01
43	R21	Chip Resistor, 18K, 10%, 0603	CR0603J183	CHIPTECH	0603	0.01	1	0.01
44	R20	Chip Resistor, 470K, 10%, 0603	CR0603J474	CHIPTECH	0603	0.01	1	0.01
45	R24	Chip Resistor, 3.3M, 10%, 0603	CR0603J335	CHIPTECH	0603	0.01	1	0.01
46	R22	Chip Resistor, 15K, 10%, 0603	CR0603J153	CHIPTECH	0603	0.01	1	0.01
							18	**1.90**

FCC ID: N4S201TRANSMITTER

Bill of Material V002

Item Number	Reference Designator	Description	Manufacturer Part Number	Manufacturer	Package	Unit Cost (USD)	Quantity	Total
19	C1, C2, C8, C12, C24, C26, C27, C28,C30, C40	Ceramic Capacitor, 0.1uF, 16V	GM010Y5V104M25	Murata	0805	0.03	10	0.30
20	L3	Chip Inductor, SMT, 5%, Q=12(min), 39nH	ELJ-RE39NJF3	Panasonic	0603	0.17	1	0.17
21	L2	Chip Inductor, SMT, 5%, Q=12(min), 47nH	ELJ-RE47NJF3	Panasonic	0603	0.17	1	0.17
22	L1, L4	Chip Inductor, SMT, 5%, Q=12(min), 56nH	ELJ-RE56NJF3	Panasonic	0603	0.17	2	0.34
23	R11, R12	Chip Resistor, 10, 10%, DIP, 1/8 WATT	MF.125-5-10	Any	DIP	0.15	2	0.30
24	R9	Chip Resistor, 620, 10%, 0603	CR0603J621	CHIPTECH	0603	0.01	1	0.01
25	R6, R7, R8	Chip Resistor, 1K, 10%, 0603	CR0603J102	CHIPTECH	0603	0.01	3	0.02
26	R13, R14	Chip Resistor, 10K, 10%, 0603	CR0603J103	CHIPTECH	0603	0.01	2	0.01
27	R1	Chip Resistor, 33K, 10%, 0603	CR0603J333	CHIPTECH	0603	0.01	1	0.05
28	R4,R5	Chip Resistor, 100K, 10%, 0603	CR0603J104	CHIPTECH	0603	0.01	2	0.01
29	R2,R3	Chip Resistor, 3.3M, 10%, 0603	CR0603J335	CHIPTECH	0603	0.01	2	0.01
		Sub-Total (USD)					**46**	**2.20**
CONNECTORS,HARDWARE, MISC. COMPONENTS								
30	P1	DC Power Jack, Male, 3.5mm, Right Angle	PJ-202A	Cui-Stack	Dip	0.15	1	0.15
31	P2	Wall Mount DC Transformer, 9V, 500mA	DPD09005-P-5	Cui-Stack		1.65	1	1.65
32	J1	Telephone Line Modular Connector	GLN64	KYCON	Dip	1.5	1	1.5
33	X1	3.579545MHz Ceramic Resonator, 0.1%	EFO-EC3584A4	Panasonic	Dip	0.25	1	0.25
34	PCB1	Main PCB		Any		0.68	1	0.68
35		Antena		Custom		0.5	1	0.5
		Sub-Total (USD)					**6**	**4.73**
36		Estimated Pick and place Cost (0.035$/part)						2.065

Bill of Material V001

Item Number	Reference Designator	Description	Manufacturer Part Number	Manufacturer	Package	Unit Cost (USD)	Quantity	Total
8	LEDA, LEDB, LEDC	Optical sensors	OPB745	Optek	Dip	1.10	3	3.3
9		Akaline Battery, AA size, 1.5V	MN1500	DURACELL		0.26	3	0.78
10		PCB		Any		0.26	1	0.26
11		Antenna		Custom		0.5	1	0.5
Sub-Total (USD)							**8**	**4.84**
12		Estimated Pick and place Cost (0.035$/part)						0.595
Total (USD)								**11.58**
Number of Components for the Transmitter							**17.00**	

FCC ID: N4S201TRANSMITTER

Bill of Material V001

Item Number	Reference Designator	Description	Manufacturer Part Number	Manufacturer	Package	Unit Cost (USD)	Quantity	Total
REMOTE TRANSMITTER								
SEMICONDUCTORS								
1	U8	8-Bit RISC CMOS Microcontroller	PIC12C508-04I/SM	Microchip	SOIC-8	1.23	1	1.23
2	U9	315MHz transmitter	AT1003	RFM	SMT	4.73	1	4.73
		Sub-Total (USD)					**2**	**5.96**
DISCRETE COMPONENTS								
		Sub-Total (USD)					**0**	**0.00**
PASSIVE COMPONENTS								
3	C31	Ceramic Capacitor, 0.01uF, 16V	GM010Y5V103M25	Murata	0603	0.02	1	0.02
4	C30	Ceramic Capacitor, 0.1uF, 16V	GM010Y5V104M25	Murata	0805	0.03	1	0.03
5	R13, R14, R16	Chip Resistor, 270, 10%, 0603	CR0603J274	CHIPTECH	0603	0.01	3	0.02
6	R15	Chip Resistor, 1K, 10%, 0603	CR0603J103	CHIPTECH	0603	0.01	1	0.01
7	L5	Chip Inductor, 47nH, 10%, 0603	ELJ-RE47NJF3	Panasonic	0603	0.12	1	0.12
		Sub-Total (USD)					**7**	**0.19**
CONNECTORS,HARDWARE, MISC. COMPONENTS								

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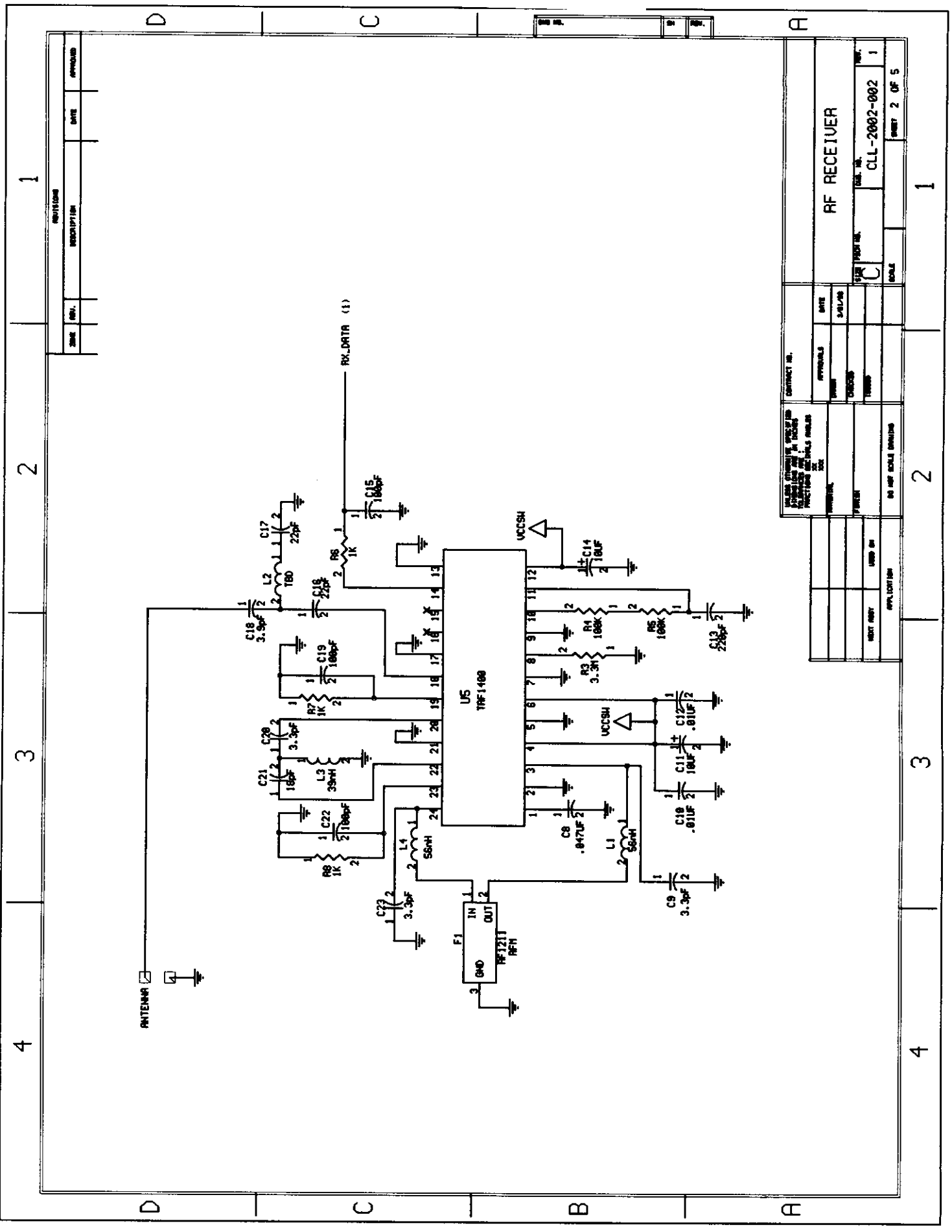

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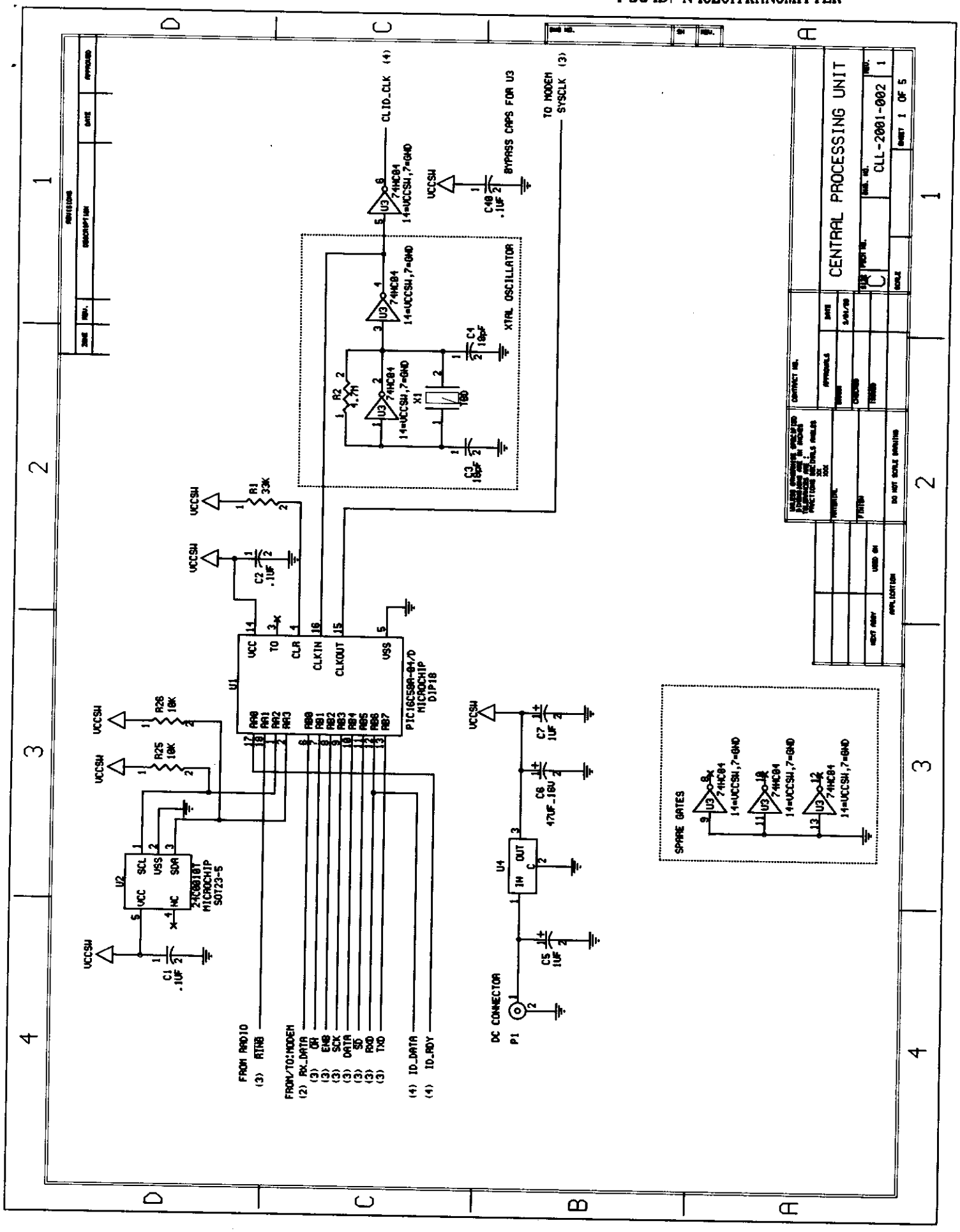

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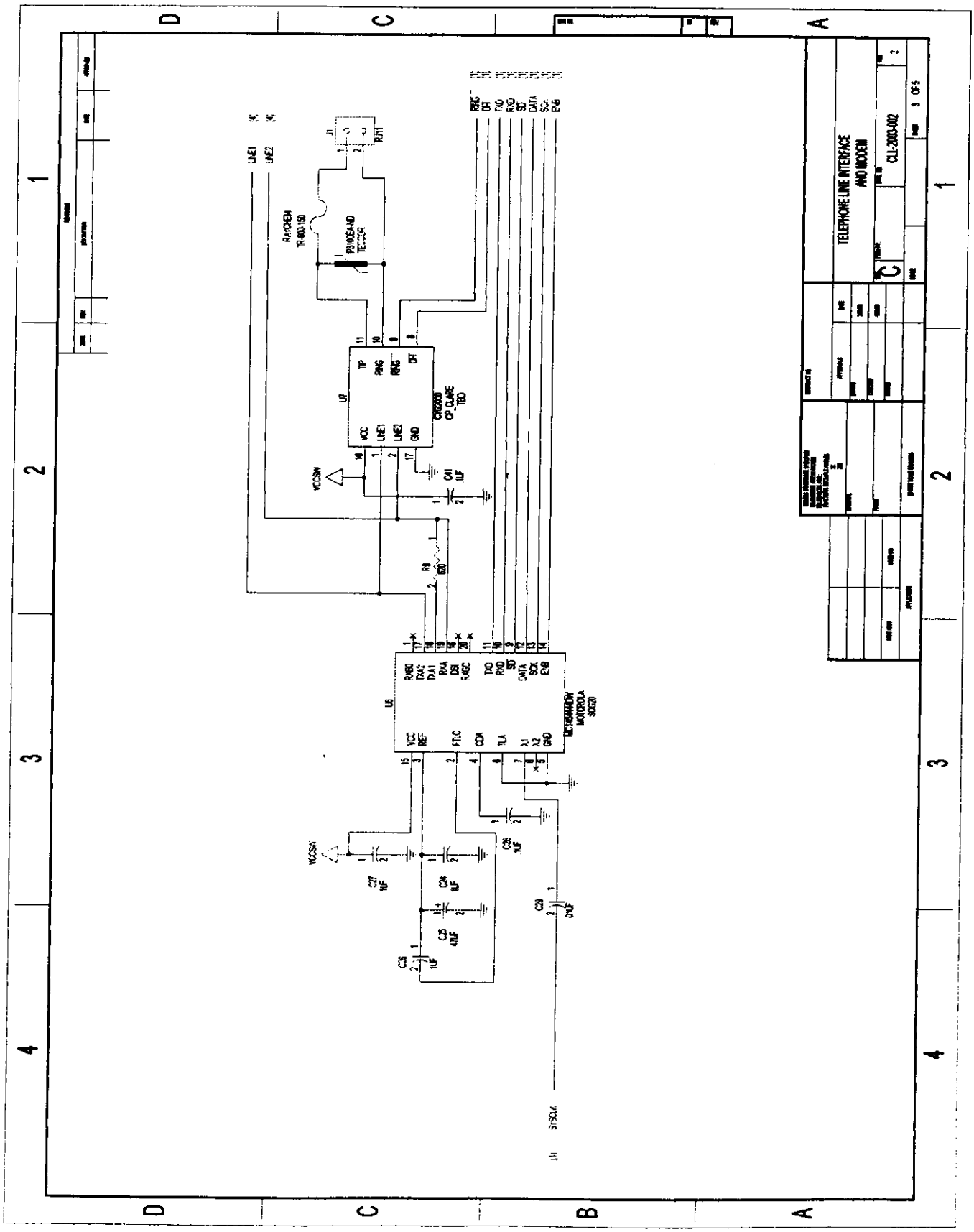

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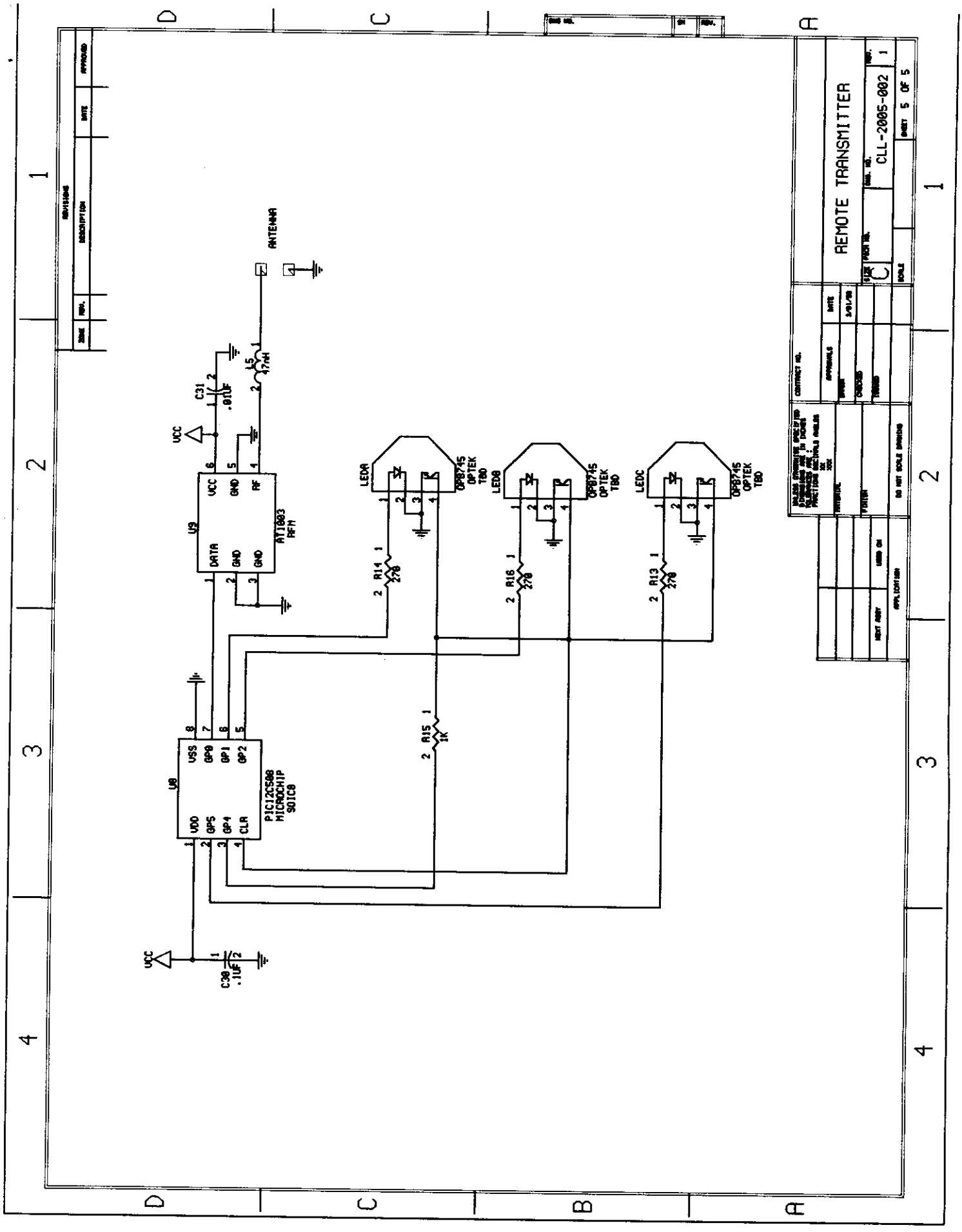

WARNING Part 15 Intentional Radiator

NOTE :

Changes or modifications not expressly approved by *LECTRON Technologies Inc.* Could void the user`s authority to operate the equipment.

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