Key Mark Technology (HK) Co., Ltd.

Room 904, Sun Cheong Ind. Bldg. 1 Cheung Shun Street. LCK. HK.

Tel : 85202345 2355 Fax : 852 2345 2377

TXB1 Transmitter Module

Overview :

The TXB1 is a FSK transmitter module that transmittes. It uses the TX4915 (Low Power ASK/FSK Transmitter IC) and discrete components. The TX4915 transmitter IC intended for applications in the North American and European VHF/UHF bands. The integrated voltage-controlled oscillator (VOC), phase/frequency detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop (PLL). In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when then PLL in out-of-lock.

Features

- Small size
- Low power consumption
- Simple-to-use
- Comply with FCC part 15 requirements

Sample circuit for FSK application with ASK transmitter IC

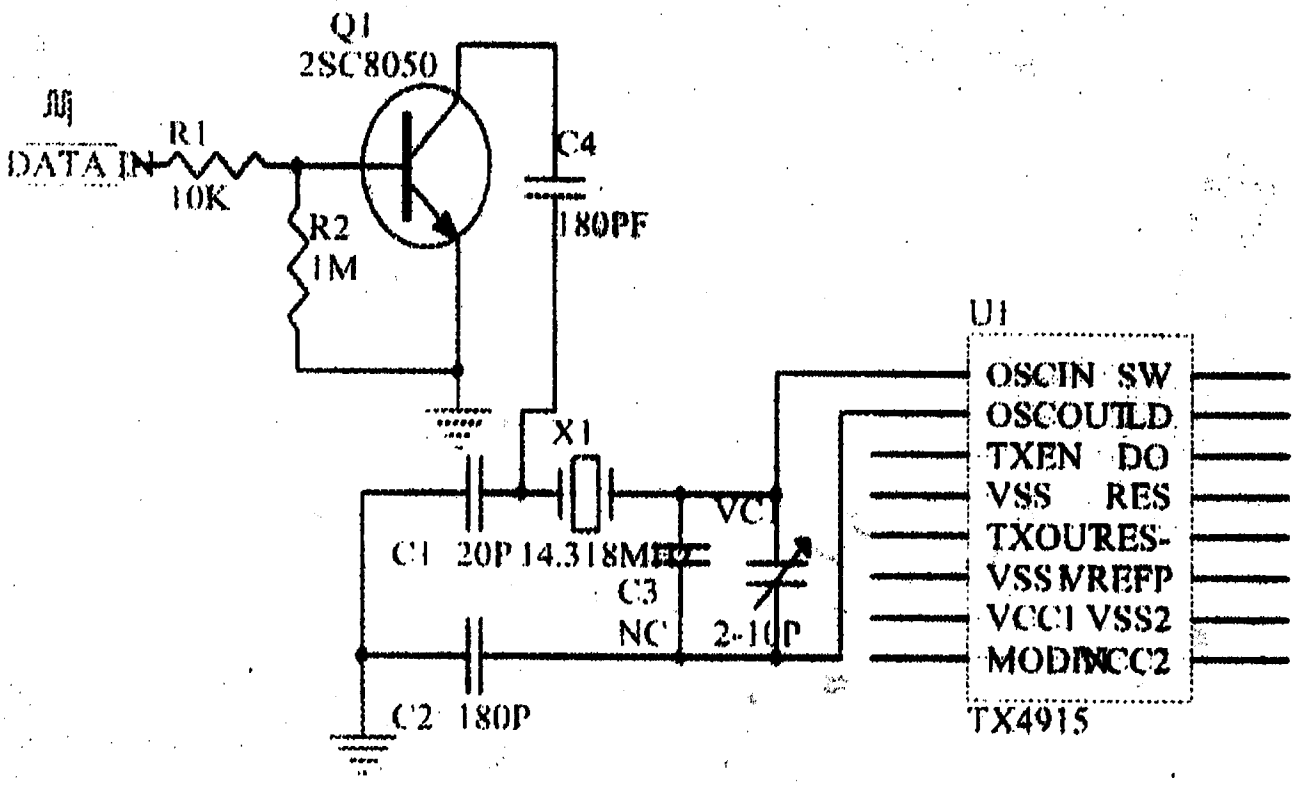


FIG 1. CRYSTAL IN(FSK)

KEF PSW4000 Remote Controller

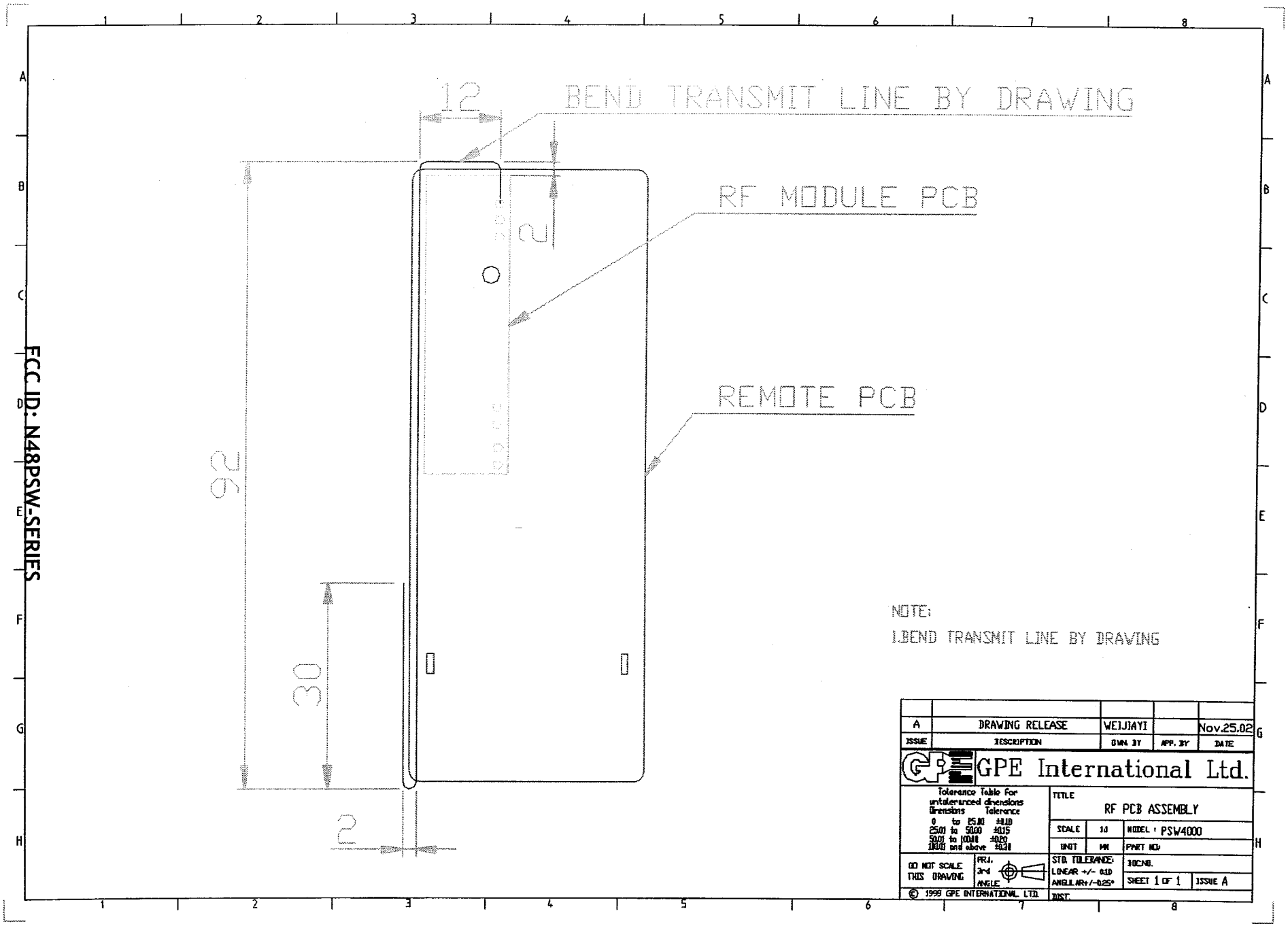
Power Supply: The power of the transmitter is taken from 2 AAA batteries. The batteries are used in series to provide a nominal voltage of 3.0VDC for the MCU and RF module. There is a MCU inside the transmitter. The batteries supply a 3.0VDC voltage to the MCU continuously without a voltage regulator. The batteries do not supply a 3.0VDC voltage to the RF module directly. Instead, the batteries will only supply a 3.0VDC voltage to the RF module through the MCU when a keypad is pressed.

Keypad Inputs: Except the STANDBY/ON keypad, there are six keypads controlling three functions. These three functions are INPUT LEVEL, CROSSOVER FREQUENCY and PHASE ADJUST. Each function has 2 keypads to control the increment and decrement by the users. K1 and K2 represent the decrement and increment of the INPUT LEVEL from MIN to MAX respectively. K3 and K4 represent the decrement and increment of the CROSSOVER FREQUENCY from 40Hz to 140Hz respectively. K5 and K6 represent the decrement and increment of the PHASE ADJUST from 0 deg to 180 deg respectively. K7 represents the choice of STANDBY or ON status.

Operation: Once a keypad is pressed, a current will supply to the corresponding pin of the MCU. The MCU will encode a corresponding 1KHz signal. This MCU is operated by a 4MHz XTAL. Then, the encoded 1KHz signal will then pass to the RF Module. This signal will then further modulate by a FREQUENCY MODULATION CIRCUIT with a 433MHz crystal inside the RF module. This RF module is operated by a 6.78MHz XTAL. At the same time, the MCU will supply a 3.0VDC voltage to the RF module from the batteries. Then, the SAW FILTER will filter the modulated signal to become to desired 433MHz transmitting signal. This 433MHz signal will then be transmitted through the antenna. The transmission power is less than 10mW and the remote range is 10M. There will be no transmitting signal for the remote controller unless a keypad is pressed.

RF Module: The RF Module (TXB1) is a FSK transmitter module that transmits. It uses the TX4915 (Low Power ASK/FSK Transmitter IC) and discrete components. This TX4915 transmitter IC intended for applications in the North American and European VHF/UHF bands and comply with FCC part 15 requirements.

Data Structure: The transmitting signal consists of 4 parts: LEAD CODE, HIGH ADDRESS, LIGHT ADDRESS and DATA. LEAD CODE is 1 bit with a 10ms period level low preceeding a 340us period level high. HIGH ADDRESS and LIGHT ADDRESS both are 8 bits, totally 16 bits representing the address of each remote controller. DATA is 8 bits representing the different transmitting data. Within the address and data, BIT "1" consists of a 680us period level low preceeding a 340us period level high. BIT "0" consists of a 340us period level low preceeding a 680us period level high.



FCC ID: N48PSW-SERIES

HiMARK
the wireless IC company

TX4915 Low Power ASK Transmitter IC

Advance Information

Description

The TX4915 is a low power ASK transmitter IC intended for applications in the North American and European VHF/UHF bands. The integrated voltage-controlled oscillator (VCO), phase/frequency detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop (PLL). In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock.

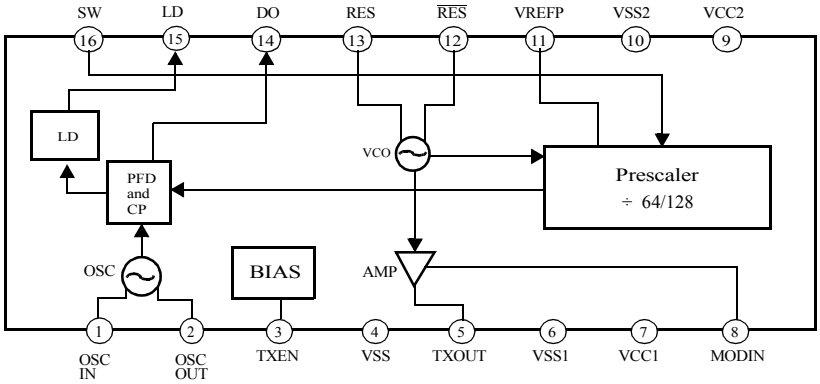
Features

- Output frequency range: 100 – 960MHz
- Supply voltage range: 2.2 – 3.6V
- Low current consumption with power down capability
- On-chip VCO with integrated PLL (÷ 64/128) dual modulus prescaler
- Out-of-lock inhibit circuit
- SSOP-16 package (0.64mm pitch)

Applications

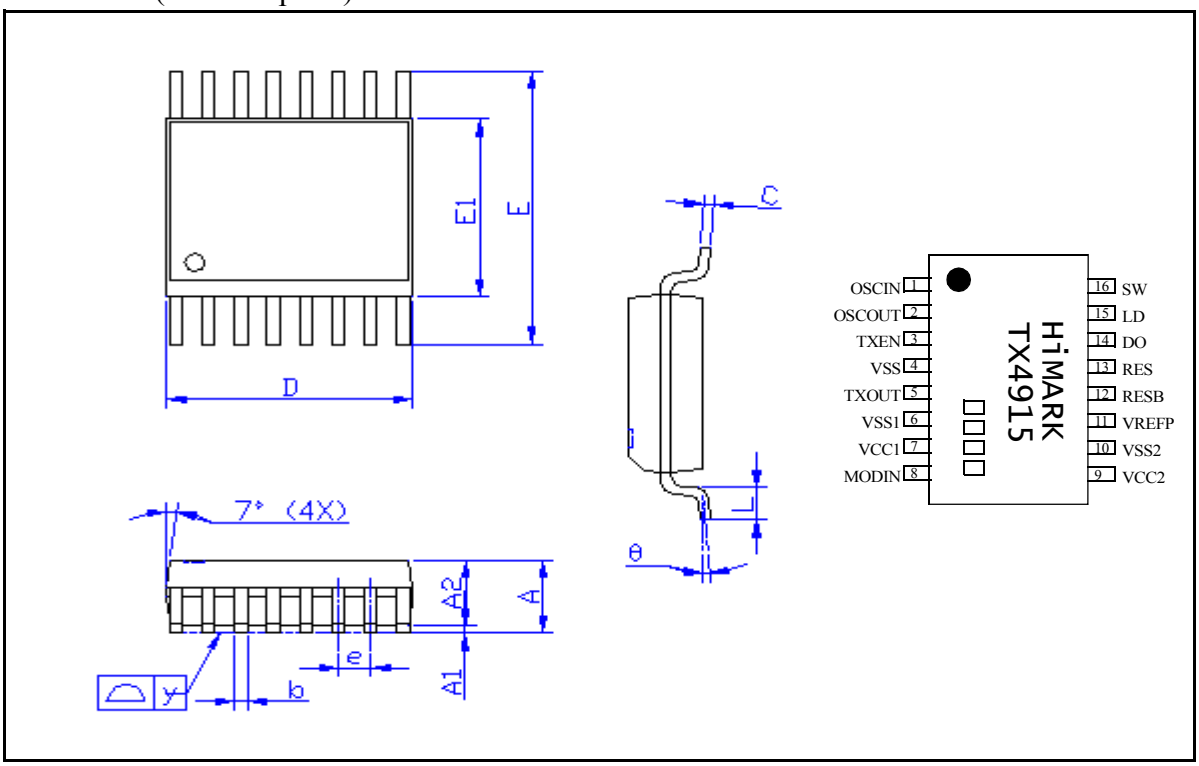
- Wireless mouse
- Car alarm and home security systems
- Remote control systems

Block Diagram



Package and Pin Assignment

SSOP-16 (0.64mm pitch)



Symbol	Dimensions in mm			Dimensions in inches		
	min.	nom.	max.	min.	nom.	max.
A	1.35	1.60	1.75	0.053	0.064	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.19	—	0.25	0.007	—	0.010
D	4.80	—	5.00	0.189	—	0.197
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e	—	0.64	—	—	0.025	—
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

Pin Descriptions

Number	Name	Description
1	OSCIN	This pin is connected directly to the base of the reference oscillator transistor. The reference oscillator uses a modified Colpitts configuration.
2	OSCOUT	This pin is connected directly to the emitter of the reference oscillator transistor.
3	TXEN	Transmitter enable control (TXEN = low = power down mode; TXEN = high = normal operation mode).
4	VSS	Ground connection for the transmit output amplifier.
5	TXOUT	Transmitter output. This pin is an open collector and requires a pull-up inductor for bias/matching and a tapped capacitor for matching.
6	VSS1	Ground connection for the transmit driver amplifier.
7	VCC1	Nominal supply voltage for the transmit driver amplifier.
8	MODIN	ASK modulation input. An external resistor is used to bias the entire transmit amplifier chain through this pin.
9	VCC2	Nominal supply voltage for the VCO and PLL circuitry.
10	VSS2	Ground connection for the PLL circuitry.
11	VREFP	Bias voltage reference pin.
12	$\overline{\text{RES}}$	Differential open collector VCO outputs.
13	RES	
14	DO	Output of the charge pump. An R-C network from this pin to ground is used to establish the PLL bandwidth.
15	LD	Lock detector output. This pin is used to set the threshold of the lock detect circuitry which enables or disables the transmit amplifier. A shunt capacitor should be used to set an R-C time constant with the on-chip series 1kΩ resistor. The time constant should be set to approximately 15 times the reference period.
16	SW	Prescaler modulus control input (SW = high = ÷ 64; SW = low = ÷ 128).

Absolute Maximum Ratings

V_{SS}, V_{SS1}, V_{SS2} = 0V

Parameter	Rating	Unit
Supply voltage range	– 0.3 to +3.6	V_{DC}
Power-down voltage	–0.3 to V_{CC}	V
MODIN voltage	–0.3 to +1.1	V
Operating ambient temperature	–40 to +85	°C
Storage temperature	–40 to +150	°C

Recommended Operating Conditions

V_{SS}, V_{SS1}, V_{SS2} = 0V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	V_{CC}	2.2	3.0	3.6	V
Operating temperature	T_A	–10	+25	+60	°C

Electrical Characteristics

(V_{CC1}, V_{CC2} = 3V, V_{SS}, V_{SS1}, V_{SS2} = 0V, TXEN = high, T_A = 25°C, f_{RF} = 433.92MHz unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Power supply						
Supply voltage	V_{CC1}, V_{CC2}		2.2	3.0	3.6	V
Total dc current (normal operation)	I_{DC}	50% duty cycle, 10kHz data applied to the MODIN input (R_{MODIN} = 33kΩ)		8		mA
Total dc current (power-down mode)	$I_{standby}$	TXEN = low			1	µA
Overall						
RF input frequency range	f_{RF}		100		960	MHz
Modulation				ASK		
Modulation frequency					100	kHz
Output power		50 Ω load	6			dBm
ON/OFF ratio				80		dB
PLL						
Prescaler divide ratio		SW = high = ÷ 64 SW = low = ÷ 128	64		128	
VCO gain	K_{VCO}	Frequency and board layout dependent		12		MHz/V
Phase noise		10kHz offset, 5kHz loop BW		–80		dBc/Hz
		100kHz offset, 5kHz loop BW		–98		dBc/Hz
2nd harmonic					–20	dBc
3rd harmonic					–35	dBc
Reference frequency					17	MHz
Crystal frequency spurs		50kHz PLL loop BW		–50		dBc
Charge pump current	I_{CP}		-50		50	µA
Stand-by mode control						
Receiver enable/disable voltage	V_{TXEN}	TXEN = high = normal operation	Vcc - 0.3V			V
		TXEN = low = power-down mode			0.3	V
Turn-on time				1	2	ms
Turn-off time				1	2	ms

Functional Description

The TX4915 is a low-power ASK transmitter IC designed for applications operating within the frequency range of 100 to 960MHz. In particular, it is intended for transmitter applications in 315/433MHz band remote keyless entry and 868/915MHz ISM-band systems. In addition, the TX4915 possesses a PLL-only mode which allows it to be simply used as a local oscillator source. The integrated voltage-controlled oscillator (VCO), phase/frequency detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the normal operation mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock.

Reference crystal oscillator

The OSCIN and OSCOUT inputs (pins 1 and 2) provide connections to an on-chip transistor which may be used to implement a Colpitts crystal oscillator. The Colpitts oscillator configuration is a low parts count topology which achieves reasonable phase noise performance. Optionally, an external signal may be ac-coupled into the OSCIN pin to provide a reference source. The OSCIN input drive level should be near $500mV_{pk-pk}$ to prevent overdriving the on-chip transistor in order to keep the phase noise and reference spurs to a minimum.

Voltage controlled oscillator

The VCO uses a tuned differential amplifier topology with the bases and collectors cross-coupled to provide positive feedback and the necessary 360° phase shift. A tuned circuit is connected to the open collector outputs and is comprised of both on-chip varactors and user-selectable off-chip inductors. The choice of inductor values determines the frequency band of operation.

Dual-modulus prescaler

A series of flip-flops divides the VCO frequency by either 64 or 128, depending upon the logic level of the SW input (pin 16). SW = high will select the ÷ 64 mode and SW = low will select the ÷ 128 mode. The divided-down signal is then applied to the phase/frequency detector where its phase/frequency is compared with the phase/frequency of the crystal reference.

Phase/frequency detector and charge pump

The phase/frequency detector (PFD) is implemented using the “tri-state comparator” topology while the charge pump (CP) consists of a current source and sink for charging and discharging the off-chip loop filter. When the VCO and reference inputs to the PFD are both phase- and frequency-locked, the CP output enters a high impedance state. Otherwise, the CP will either charge or discharge the loop filter.

Out-of-lock inhibit circuitry

The out-of-lock inhibit circuitry is used to disable the transmitter output when the VCO is not locked to the reference oscillator and comply with regulatory limits during the unlocked condition. An off-chip shunt capacitor connected to the LD output (pin 15) is used to set an R-C time constant (together with an on-chip series 1kΩ resistor.) This time constant should be set to be approximately 15 times the reference period.

Transmit amplifier chain

A transmit amplifier chain consists of a driver amplifier followed by an open collector output stage. The open collector TXOUT output (pin 5) requires an external pull-up inductor for bias. This inductor may be used as part of an L-C matching circuit for transforming the amplifier output impedance to that of an external loop antenna. To achieve optimum power-added efficiency, the peak-to-peak RF voltage swing at the TXOUT pin should be twice the supply voltage. Also, the output amplifier has its own ground pin (VSS) in order to improve isolation.

The transmitter chain is designed for amplitude-shift-keying/on-off keying (ASK/OOK), with the modulation data provided at the MODIN input (pin 8). When $V_{MODIN} > 0.7V$, an output signal is transmitted, and when $V_{MODIN} \leq 0.7V$, no output signal is transmitted.

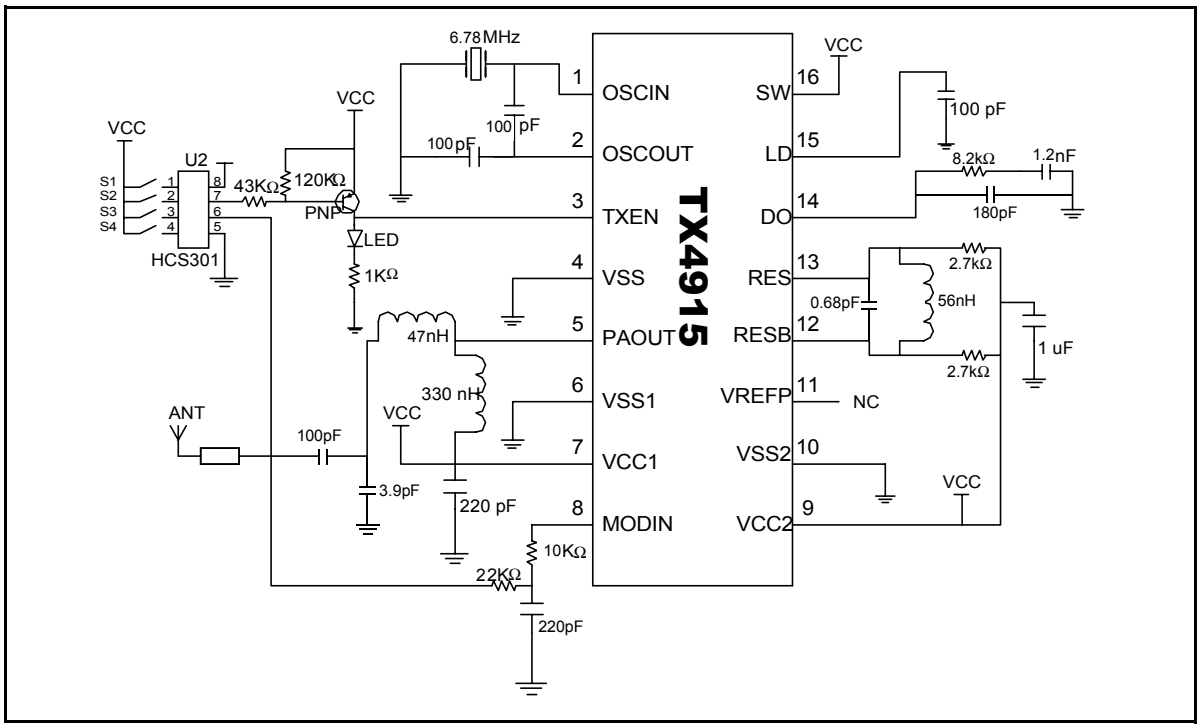
Operation modes

The table below summarizes the TX4915's three operating modes — power-down, PLL-only and transmit, which are controlled by the TXEN and MODIN inputs.

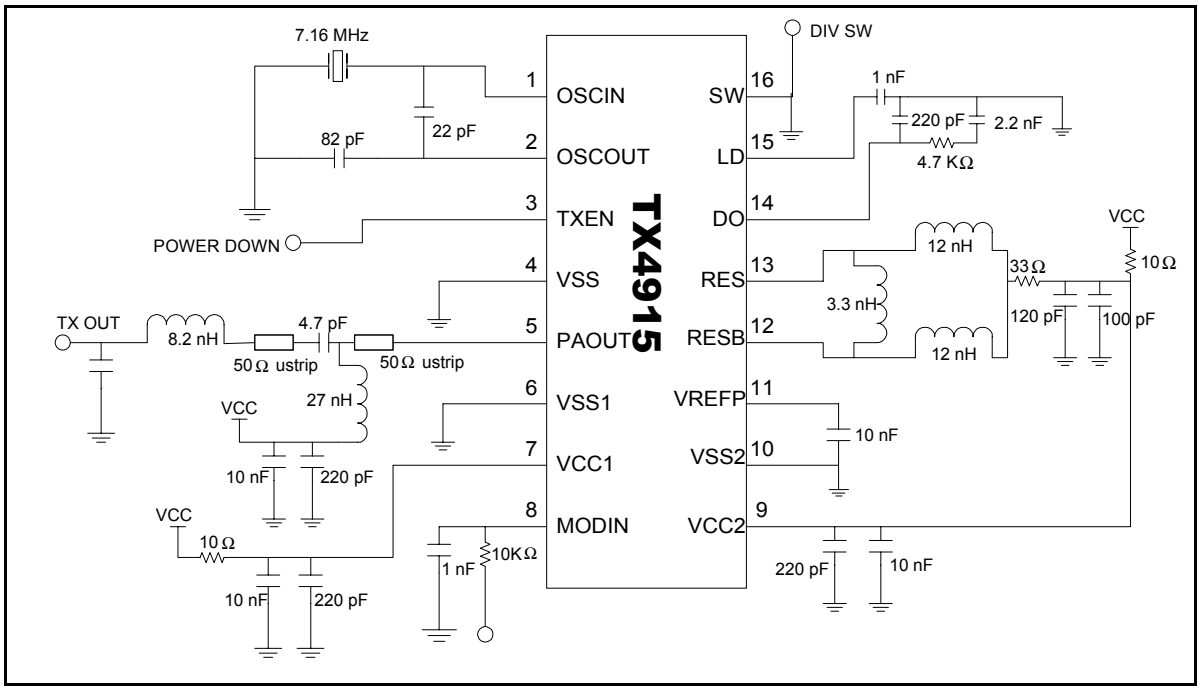
TXEN	MODIN	Operation Mode
L	L	Power-down
H	L	PLL-only
H	> 0.7V	Transmit

Application Circuit

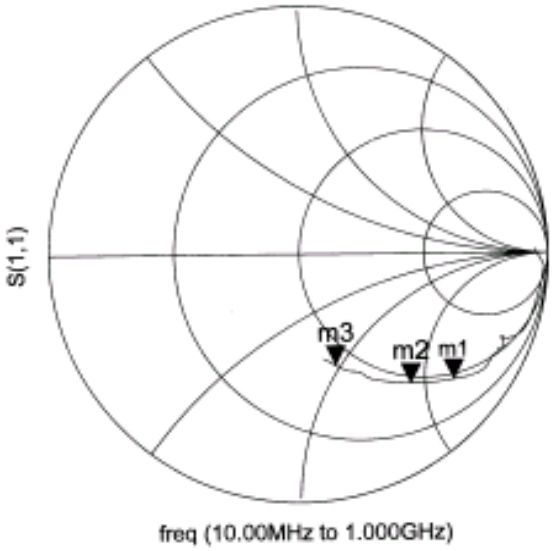
433.92 MHz



916.5 MHz



PA Output Impedance (typical)



Frequency (MHz)	Mag	Phase
303	0.80	-39.00
315	0.79	-39.90
318	0.79	-40.20
418	0.70	-48.10
434	0.69	-49.40
868	0.47	-72.30
915	0.46	-74.20

1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87Ri family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A address/data bus architecture and a large number of bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

KS86C4204/C4208/P4208 MICROCONTROLLER

The KS86C4204/C4208/P4208 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87Ri CPU core. The KS86C4204/C4208/P4208 is a versatile microcontroller, with its A/D converter, SIO, IIC and a zero-crossing detection capability it can be used in a wide range of general purpose applications.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C4204/C4208/P4208 have 4-Kbyte or 8-Kbyte of program memory on-chip (ROM) and 208-bytes of general purpose register area RAM.

Using the SAM87Ri design approach, the following peripherals were integrated with the SAM87Ri core:

- Four configurable I/O ports (24 pins)
- Nine interrupt sources with one vector and one interrupt level
- Two 8-bit timer/counter with various operating modes
- Analog to digital converter with 12 input channels and 10-bit resolution
- One synchronous SIO module
- One IIC module
- Two 12-bit PWM output

The KS86C4204/C4208/P4208microcontroller is ideal for use in a wide range of electronic applications requiring simple timer/counter, PWM, ADC, SIO, IIC, ZCD and capture functions. KS86C4204/C4208/P4208 is available in a 28/32-pin SOP and a 30-pin SDIP package.

OTP

The KS86P4208 is an OTP (One Time Programmable) version of the KS86C4204/C4208 microcontroller. The KS86P4208 has on-chip 8-Kbyte one-time-programmable EPROM instead of masked ROM. The KS86P4208 is fully compatible with the KS86C4204/C4208, in function, in D.C. electrical characteristics and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 208-byte general purpose register area (RAM)
- 4K/8K byte internal program memory (ROM)

Instruction Set

- 41 instructions
- The SAM87RI core provides all the SAM87 core instruction except the word-oriented instruction, multiplication, division, and some one-byte instruction

Instruction Execution Time

- 375 ns at 16 MHz fosc(minimum)

Interrupts

- 9 interrupt sources and 1 vector
- One interrupt level

General I/O

- Four I/O ports (total 24pins)
- Bit programmable ports

Serial I/O

- One synchronous serial I/O module
- Selectable transmit and receive rates

Multi-Master IIC-Bus

- Serial peripheral interface

Zero-Crossing Detection Circuit

- Zero crossing detection circuit that generates a digital signal in synchronism with an AC signal input

Built-in reset Circuit (LVD)

- Low voltage detector for safe reset

Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with three operating mode
- One 8-bit timer/counter

PWM module

- 12-bit PWM 2-ch (Max: 250KHz)
- 6-bit base + 6-bit extension frame
- One 8-bit timer/counter

A/D Converter

- 12 analog input pins
- 10-bit conversion resolution

Buzzer Frequency Range

- 200 Hz to 20 kHz signal can be generated

Oscillator Freqeuncy

- 1-MHz to 16-MHz external crystal oscillator Maximum 16-MHz CPU clock
- RC: 4MHz(typ)

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 3.0 V to 5.5 V (LVD)
- 1.8 V to 5.5 V (No LVD)

OTP Interface Protocol Spec

- Serial OTP

Package Types

- KS86C4204/C4208
  32-pin SOP-450 (3V LVD)
  30-pin SDIP-400 (3V LVD)
  28-pin SOP-375

BLOCK DIAGRAM

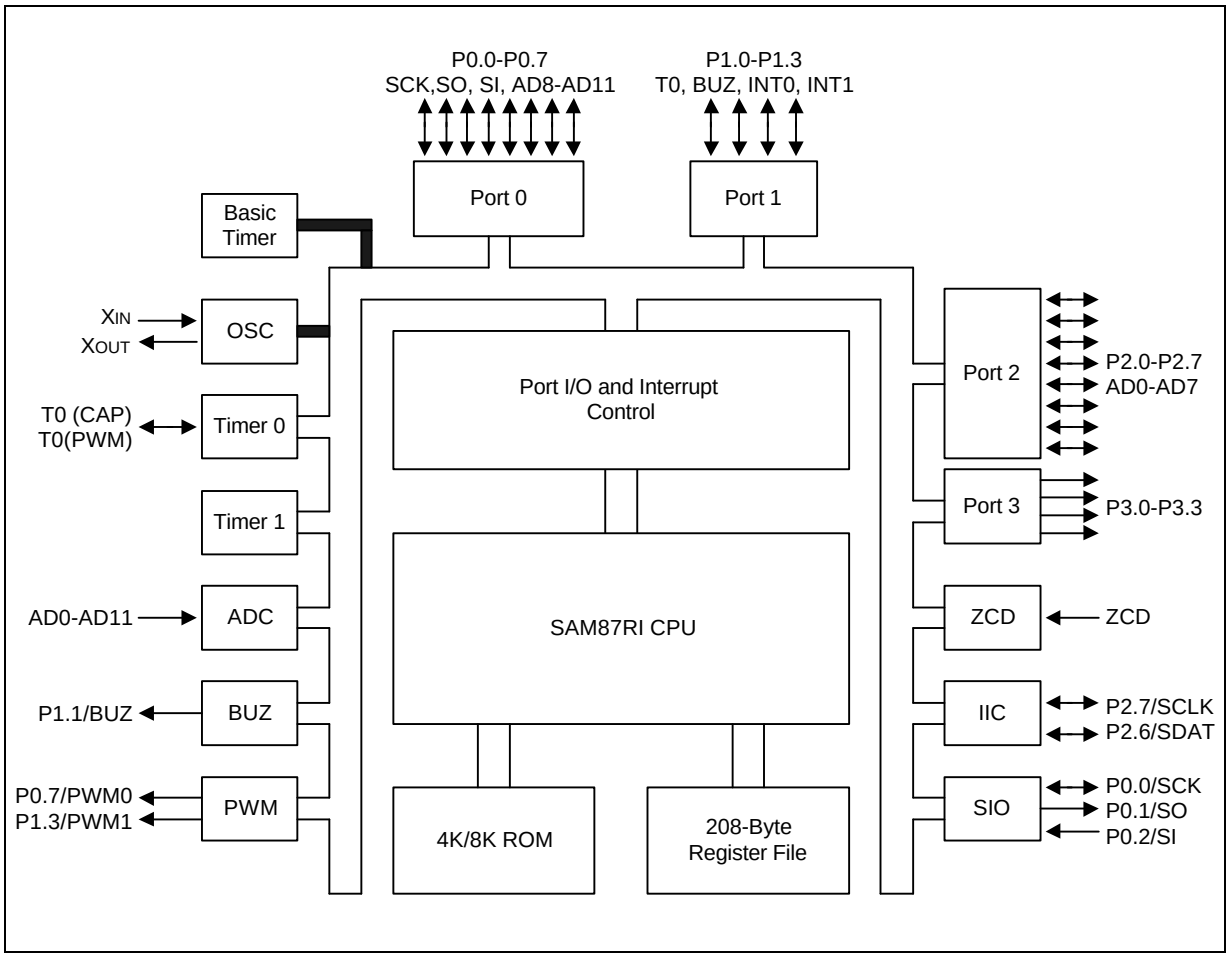


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

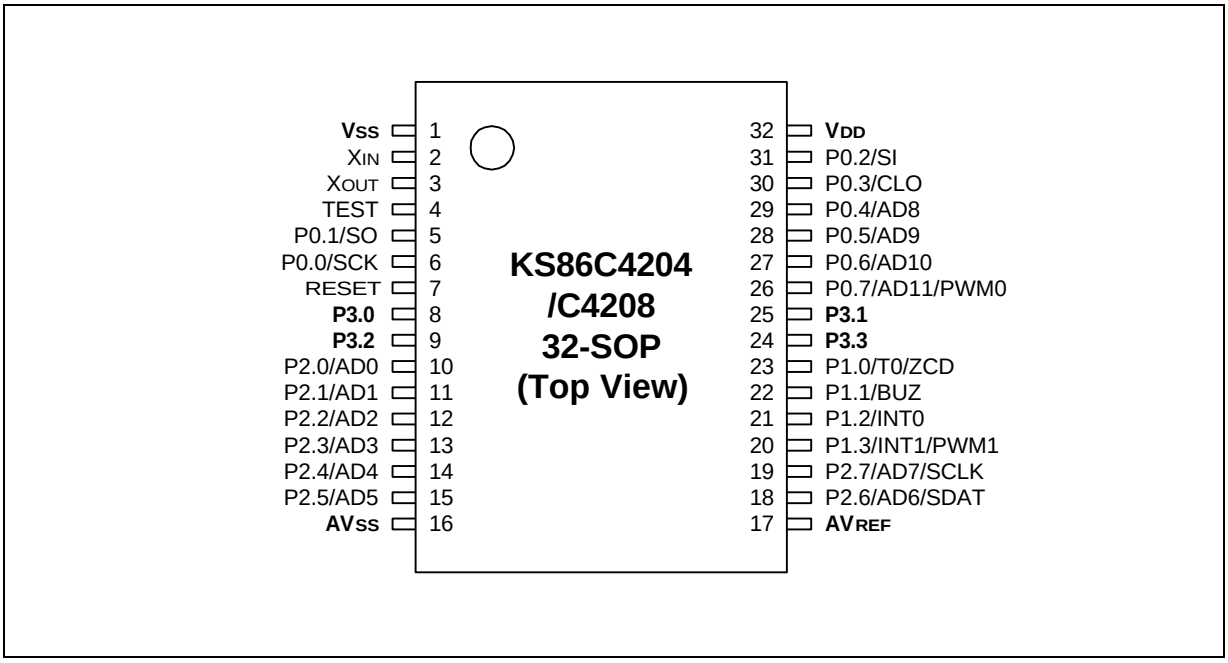


Figure 1-2. Pin Assignment Diagram (32-Pin SOP Package)

PIN ASSIGNMENTS (Continued)

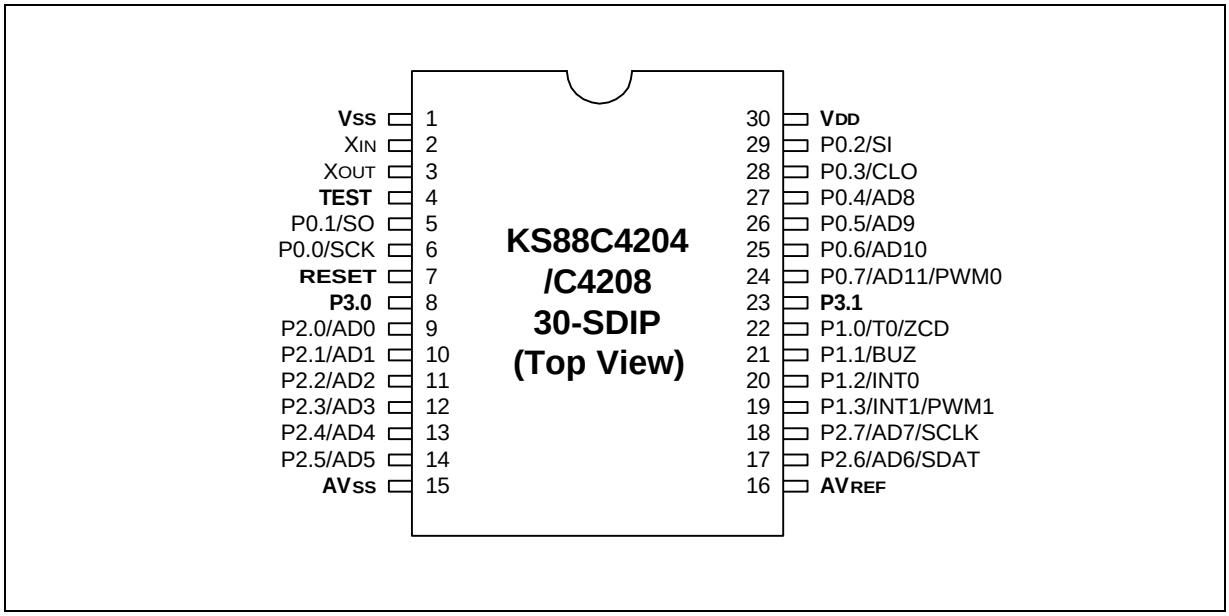


Figure 1-3. Pin Assignment Diagram (30-Pin SDIP Package)

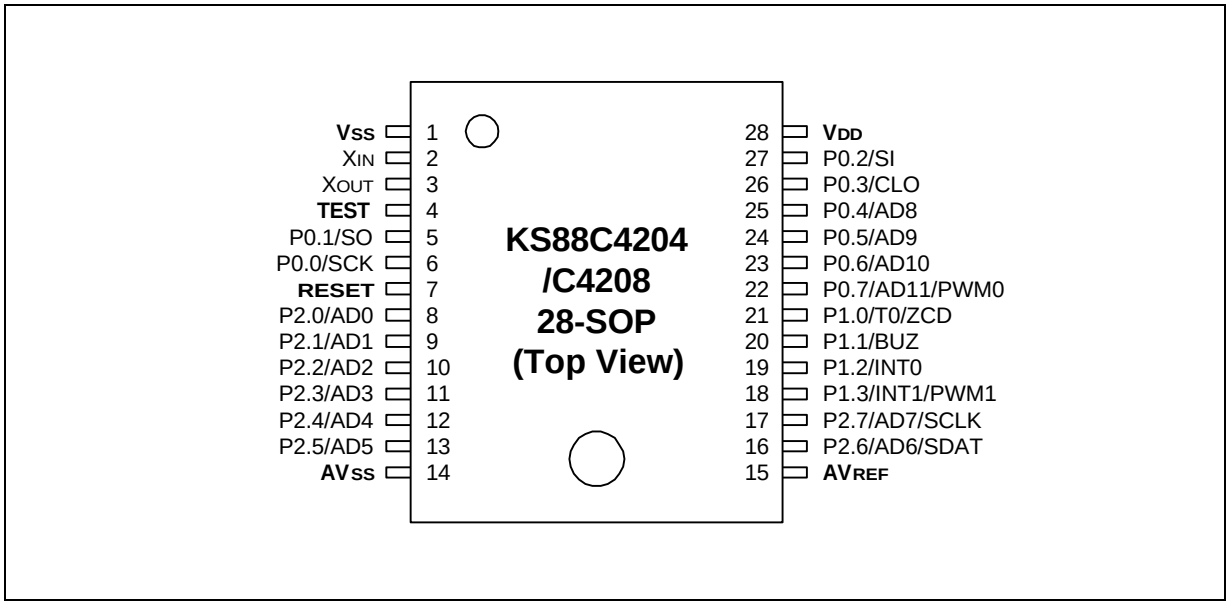


Figure 1-4. Pin Assignment Diagram (28-Pin SOP Package)

PIN DESCRIPTIONS

Table 1-1. KS86C4204/C4208/P4208 Pin Descriptions

Pin Names	Pin Type	Pin Description	Pin Type	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software.	E E-1	SCK,SO,SI , CLO, AD8-AD11
P1.0-P1.3	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 1 pins can also be used as alternative functions.	D	T0/ZCD BUZ INT0 INT1
P2.0-P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open drain output. Pull up resistors are assignable by software. Port 2 can also be used as external interrupt, A/D input.	E-1	AD0-AD7
P3.0-P3.3	O	Push-pull or open-drain output port. Pull-up resistors are assignable by software.	E-2	–
X_{IN}, X_{OUT}	–	Crystal/ceramic, or RC oscillator signal for system clock.	–	–
RESET	I	System RESET signal input pin.	B	–
TEST	I	Test signal input pin (for factory use only: must be connected to V_{SS})	–	–
AV_{REF}, AV_{SS}	–	A/D converter reference voltage input and ground	–	–
V_{DD}, V_{SS}	–	Voltage input pin and ground	–	–
SCK	I/O	Serial interface clock input or output	E	P0.0
SO	O	Serial data output	E	P0.1
SI	I	Serial data output	E	P0.2
CLO	O	System clock output port	E	P0.3
SCLK SDAT	I/O	IIC CLOCK IIC DATA	E-1	P2.7 P2.6
BUZ	O	200 Hz-20 kHz frequency output for buzzer sound.	D	P1.1
ZCD	I	Zero crossing detector input	D	P1.0
T0	I/O	Timer 0 capture input or 10-bit PWM output	D	P1.0
INT0 INT1	I	External interrupt input	D	P1.2 P1.3
PWM0 PWM1	O	12-bit PWM output	E-1 D	P0.7 P1.3
AD0-AD11	I	A/D converter input	E-1	P2.0-P2.7 P0.4-P0.7

PIN CIRCUITS

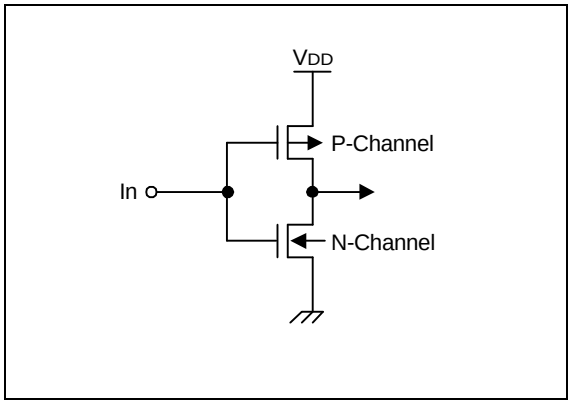


Figure 1-5. Pin Circuit Type A

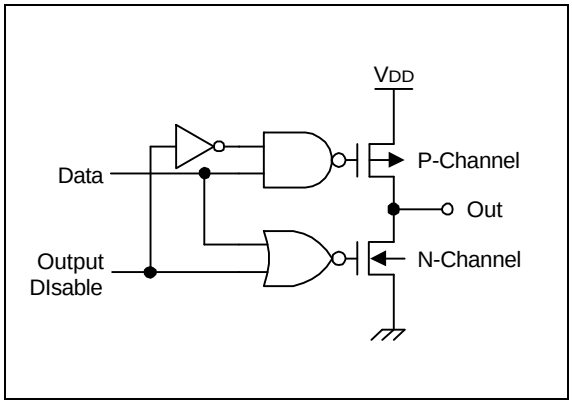


Figure 1-7. Pin Circuit Type C

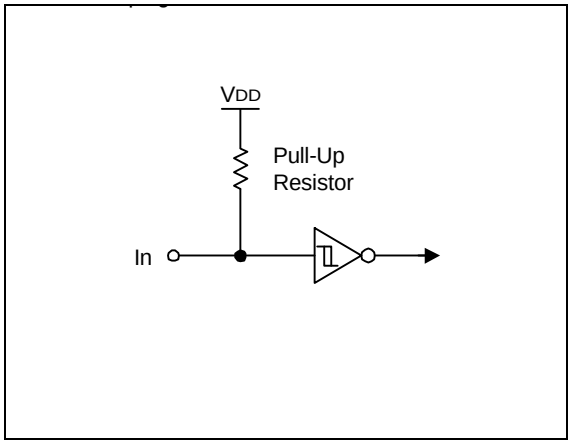


Figure 1-6. Pin Circuit Type B

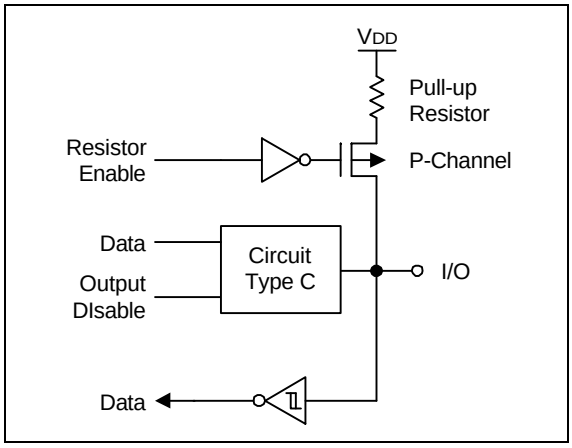


Figure 1-8. Pin Circuit Type D

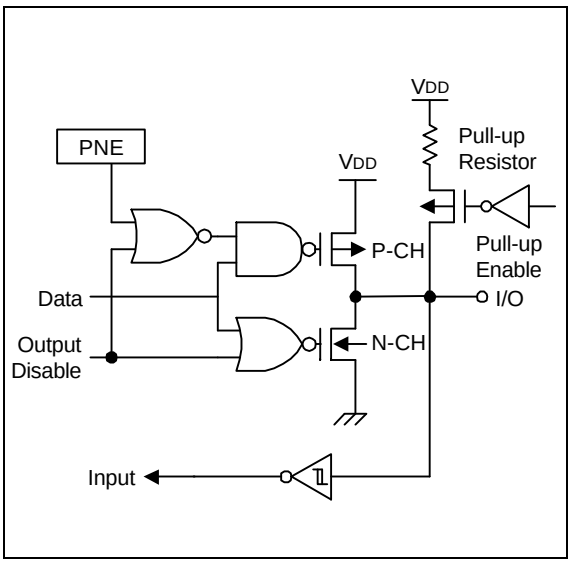


Figure 1-9. Pin Circuit Type E

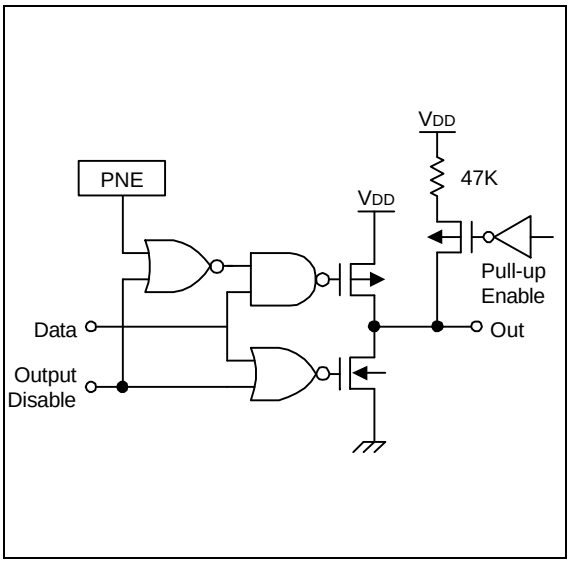


Figure 1-11. Pin Circuit Type E-2

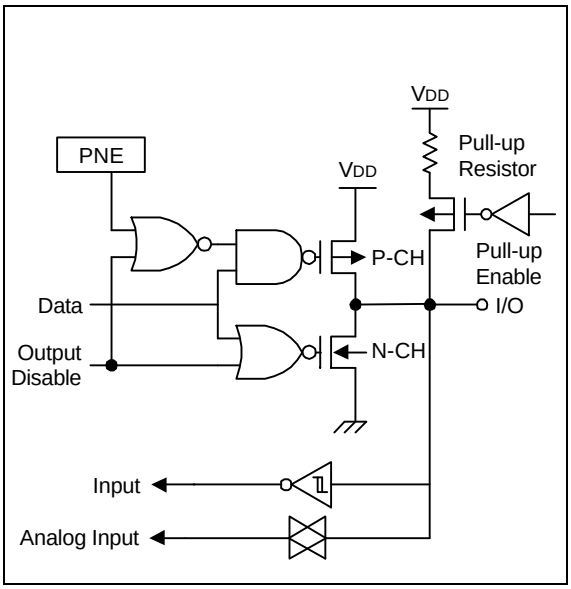


Figure 1-10. Pin Circuit Type E-1

16 ELECTRICAL DATA

OVERVIEW

In this section, the following KS86C4204/C4208/P4208 electrical characteristics are presented in tables and graphs:

— Absolute maximum ratings
— D.C. electrical characteristics
— A.C. electrical characteristics
— Operating Voltage Range
— Schmitt trigger input characteristics
— Oscillator characteristics
— Oscillation stabilization time
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a RESET
— Power-on RESET circuit characteristics
— A/D converter electrical characteristics
— Zero-crossing detector
— Zero Crossing Waveform Diagram

Table 16-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_I	All input ports	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All output ports	– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O pin active	– 25	mA
		All I/O pins active	– 80	
Output current low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 1, 2, 3	+ 100	
		Total pin current for ports 0	+ 200	
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C

Table 16-2. D.C. Electrical Characteristics(30SDIP, 32SOP)

(T_A = – 40°C to + 85°C, V_{DD} = 3.0 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input high voltage	V_{IH1}	Ports 0, 1, 2 and RESET	V_{DD}= 3.0 to 5.5 V	0.8 V_{DD}	–	V_{DD}	V
	V_{IH3}	X_{IN} and X_{OUT}		V_{DD} – 0.1			
Input low voltage	V_{IL1}	Ports 0, 1, 2 and RESET	V_{DD}= 3.0 to 5.5 V	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN} and X_{OUT}				0.1	
Output high voltage	V_{OH}	I_{OH} = – 10 mA ports 0-3	V_{DD}= 4.5 to 5.5 V	V_{DD} – 1.5	V_{DD} – 0.4	–	V
Output low voltage	V_{OL}	I_{OL} = 25 mA port 0-3	V_{DD}= 4.5 to 5.5 V	–	0.4	2.0	V
Input high leakage current	I_{LIH1}	All input pins except I_{LIH2}	V_{IN} = V_{DD}	–	–	1	µA
	I_{LIH2}	X_{IN}, X_{OUT}	V_{IN} = V_{DD}			20	
Input low leakage current	I_{LIL1}	All input pins except I_{LIL2} and RESET	V_{IN} = 0 V	–	–	– 1	µA
	I_{LIL2}	X_{IN}, X_{OUT}	V_{IN} = 0 V			– 20	
Output high leakage current	I_{LOH}	All output pins	V_{OUT} = V_{DD}	–	–	2	µA
Output low leakage current	I_{LOL}	All output pins	V_{OUT} = 0 V	–	–	– 2	µA
Pull-up resistor	R_P	V_{IN} = 0 V Port 0-2	V_{DD} = 5 V	30	47	70	KΩ
		RESET	V_{DD} = 5 V	100	200	350	
Supply current	I_{DD1}	RUN mode 16-MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	11	20	mA
		4-MHz CPU clock	V_{DD} = 3 V		1.5	4	
	I_{DD2}	Idle mode 16-MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	3	8	
		4-MHz CPU clock	V_{DD} = 3.3 V		0.5	2	
	I_{DD3}	Stop mode	V_{DD} = 4.5 to 5.5 V	–	65	100	µA
			V_{DD} = 3.3 V		45	80	

NOTE: D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resisters, output port drive current, ZCD and ADC.

Table 16-3. D.C. Electrical Characteristics (28SOP)

(T_A = – 40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

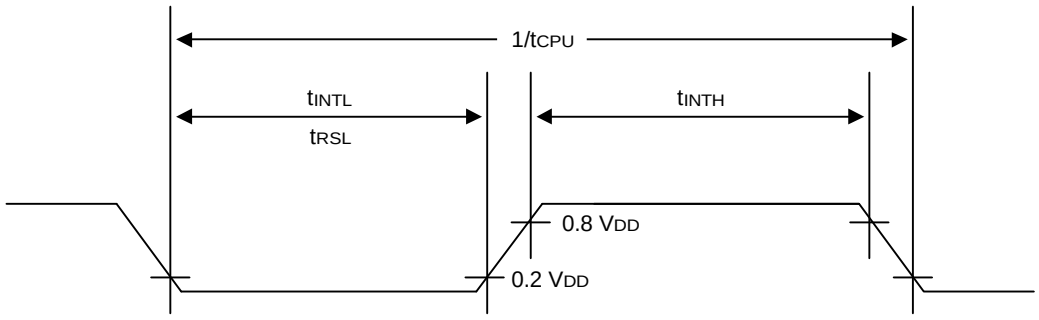
Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input high voltage	V_{IH1}	Ports 0, 1, 2 and RESET	V_{DD}= 1.8 to 5.5 V	0.8 V_{DD}	–	V_{DD}	V
	V_{IH3}	X_{IN} and X_{OUT}		V_{DD} – 0.1			
Input low voltage	V_{IL1}	Ports 0, 1, 2 and RESET	V_{DD}= 1.8 to 5.5 V	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN} and X_{OUT}				0.1	
Output high voltage	V_{OH}	I_{OH} = – 10 mA ports 0-3	V_{DD}= 4.5 to 5.5 V	V_{DD} – 1.0	V_{DD} – 0.4	–	V
Output low voltage	V_{OL}	I_{OL} = 25 mA port 0-3	V_{DD}= 4.5 to 5.5 V	–	0.4	2.0	V
Input high leakage current	I_{LIH1}	All input pins except I_{LIH2}	V_{IN} = V_{DD}	–	–	1	µA
	I_{LIH2}	X_{IN}, X_{OUT}	V_{IN} = V_{DD}			20	
Input low leakage current	I_{LIL1}	All input pins except I_{LIL2} and RESET	V_{IN} = 0 V	–	–	– 1	µA
	I_{LIL2}	X_{IN}, X_{OUT}	V_{IN} = 0 V			– 20	
Output high leakage current	I_{LOH}	All output pins	V_{OUT} = V_{DD}	–	–	2	µA
Output low leakage current	I_{LOL}	All output pins	V_{OUT} = 0 V	–	–	– 2	µA
Pull-up resistor	R_P	V_{IN} = 0 V Port 0-2	V_{DD} = 5 V	30	47	70	KΩ
		RESET	V_{DD} = 5 V	100	200	350	
Supply current	I_{DD1}	RUN mode 16-MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	11	20	mA
		3-MHz CPU clock	V_{DD} = 1.8 to 2.2 V		1	3	
	I_{DD2}	Idle mode 16-MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	3	9	
		3-MHz CPU clock	V_{DD} = 1.8 to 2.2 V		0.3	1.0	
	I_{DD3}	Stop mode	V_{DD} = 4.5 to 5.5 V	–	0.1	5	µA
			V_{DD} = 3 V				
			V_{DD} = 1.8 to 2.2 V				

NOTE: D.C. electrical values for Supply current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resisters, output port drive current, ZCD and ADC.

Table 16-4. A.C. Electrical Characteristics

(T_A = –40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width	t_{INTH}, t_{INTL}	Port 1v(INT0, INT1) V_{DD} = 5V ± 10%	–	200	–	ns
RESET input low width	t_{RSL} –	Input V_{DD} = 5V ± 10%	–	1	–	us



NOTE: The unit tcpu means one CPU clock period.

Figure 16-1. Input Timing Measurement Points

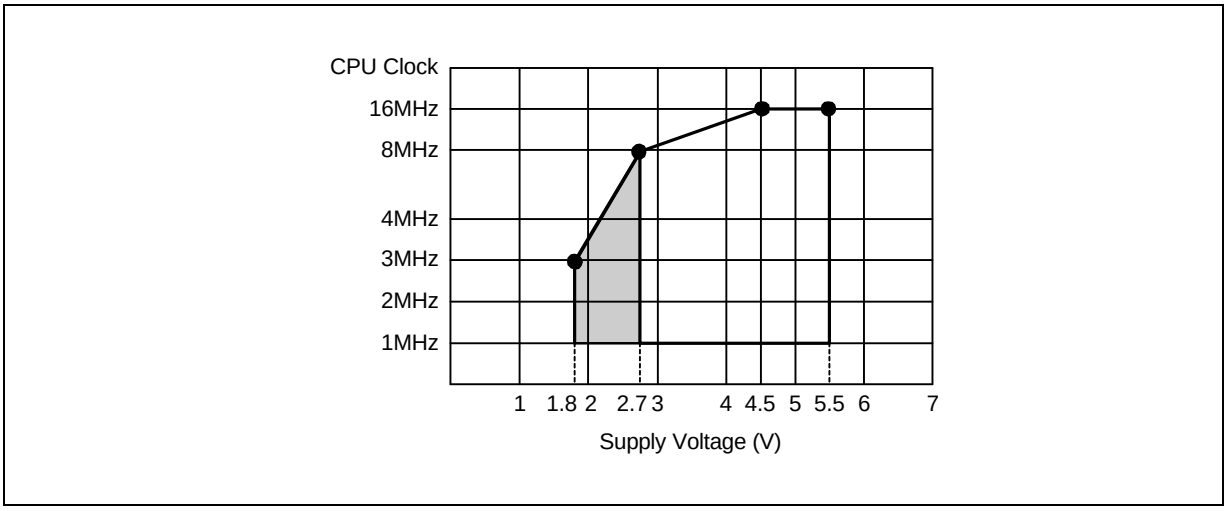


Figure 16-2. Operating Voltage Range (KS86C4204/C4208)

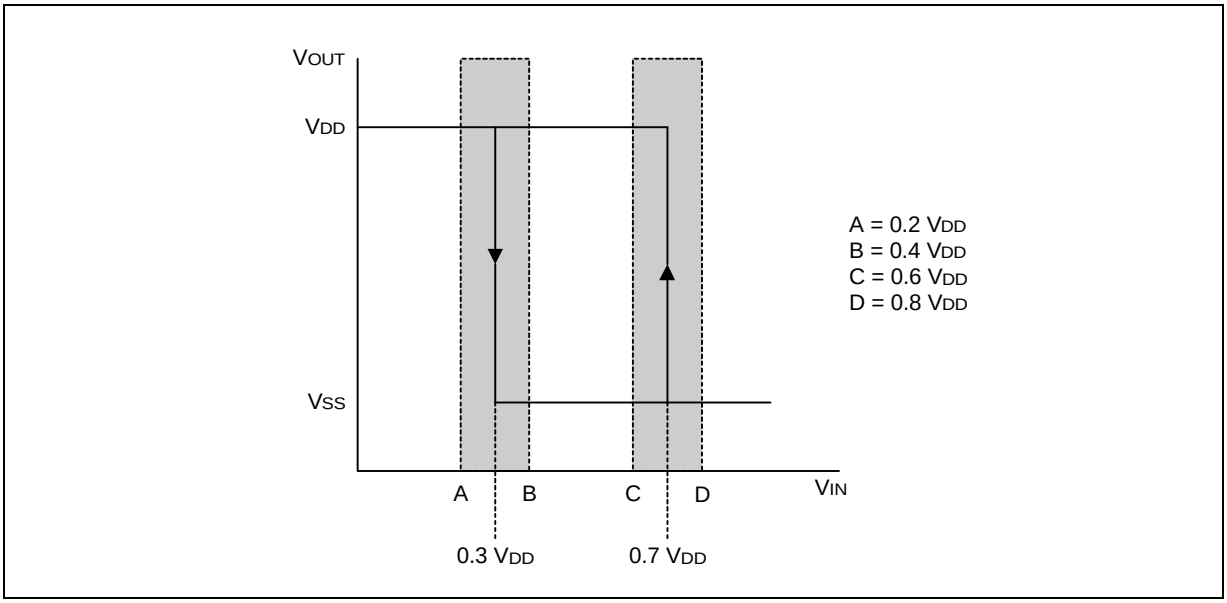


Figure 16-3. Schimtt Trigger Input Characteristic Diagram

Table 16-5. Oscillator Characteristics (30SDIP, 32SOP)

(T_A = – 40°C to + 85°C)

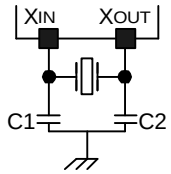
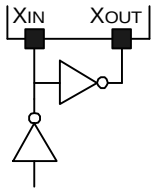
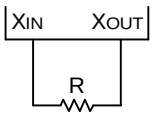
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal or ceramic		V_{DD} = 4.5 to 5.5 V V_{DD} = 3.0 to 4.5 V	1 1	– –	16 8	MHz
External clock (Main system)		V_{DD} = 4.5 to 5.5 V V_{DD} = 3.0 to 4.5 V	1 1	– –	16 8	
RC oscillator		V_{DD} = 4.75 to 5.25 V Tolerance: 10%	–	4	–	

Table 16-6. Oscillation Stabilization Time (28SOP)

(T_A = – 40°C to + 85°C)

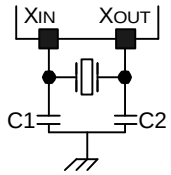
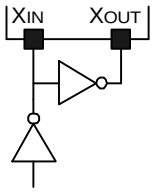
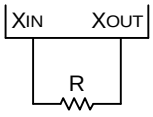
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal or ceramic		V_{DD} = 4.5 to 5.5 V V_{DD} = 2.7 to 4.5 V V_{DD} = 1.8 to 2.7 V	1 1 1	– – –	16 8 3	MHz
External clock (Main system)		V_{DD} = 4.5 to 5.5 V V_{DD} = 2.7 to 4.5 V VDD = 1.8 to 2.7 V	1 1 1	– – –	16 8 3	
RC oscillator		V_{DD} = 4.75 to 5.25 V Tolerance: 10%	–	4	–	

Table 16-7. Oscillation Stabilization Time

(T_A = – 40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	fosc > 1.0 MHz	–	–	20	ms
Main ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	
External clock (main system)	X_{IN} input high and low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator stabilization wait time	t_{WAIT} when released by a reset (1)	–	2^{16}/fosc	–	ms
	t_{WAIT} when released by an interrupt (2)	–	–	–	

NOTES:

1. fosc is the oscillator frequency.
2. The duration of the oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

Table 16-8. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C to + 85°C, V_{DD} = 1.8 V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Stop mode	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode; V_{DDDR} = 1.8 V	–	0.1	5	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

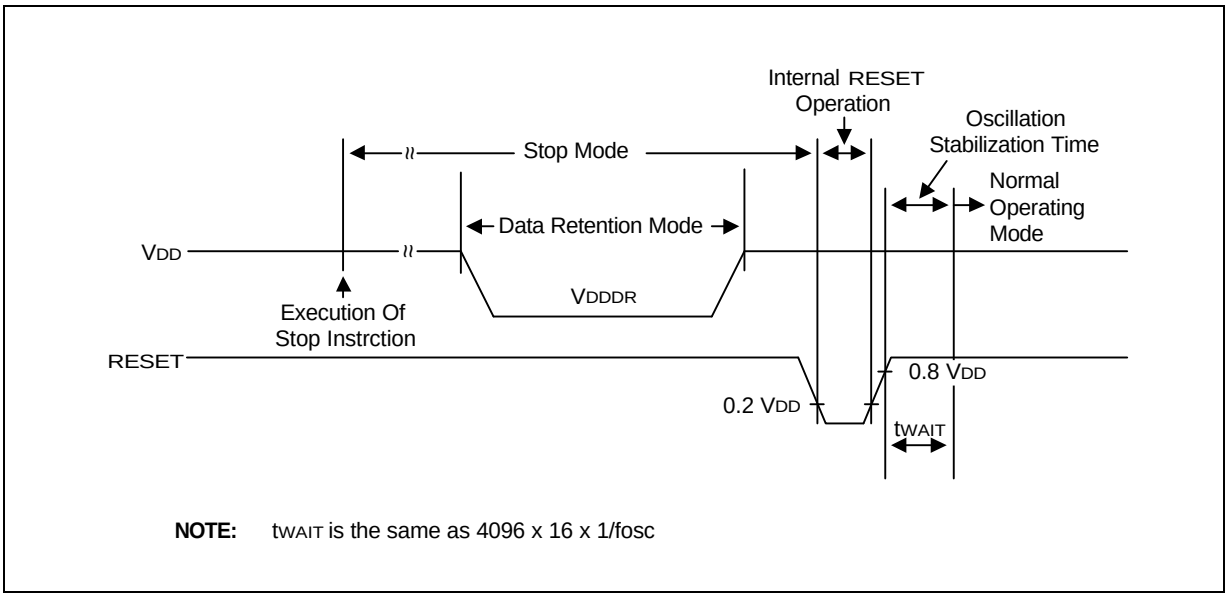


Figure 16-4. Stop Mode Release Timing When Initiated by a RESET

Table 16-9. Power-on RESET Circuit Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 3.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power-on reset voltage high	V_{DDH}		3.0	–	5.5	V
Power-on reset voltage low	V_{DDL}		0	2.6	3.0	V
Power supply voltage rise time	t_r		10		(1)	us
Power supply voltage off time	t_{off}		0.5			s
Power-on reset circuit cunsumption current (2)	I_{DDPR}	V_{DD} = 5 V ± 10%		65	100	µA
		V_{DD} = 3.3 V		45	80	

NOTES:

1. 216/fx (= 6.55 ms at fx = 10 MHz)
2. Current consumed when power-on reset circuit is provided internally.

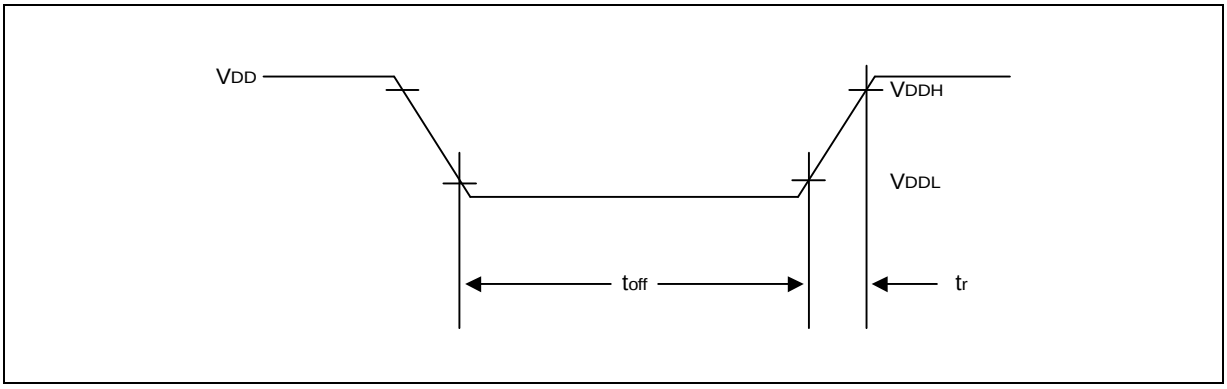


Figure16-5. Power-on RESET Timing

Table 16-10. A/D Converter Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 1.8/3.0 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total accuracy		V_{DD} = 5.12 V CPU clock = 10 MHz AV_{REF} = 5.12 V AV_{SS} = 0 V	–	–	± 3	LSB
Integral linearity error	ILE	"	–	–	± 2	LSB
Differential linearity error	DLE	"	–	–	± 1	
Offset error of top	EOT	"	–	±1	±3	
Offset error of bottom	EOB	"	–	±1	± 2	
Conversion time(1)	t_{CON}	fosc = 10 MHz	20	–	–	µs
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	–	–	MΩ
ADC reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
ADC reference ground	AV_{SS}	–	V_{SS}	–	V_{SS} + 0.3	V
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5 V	–	–	10	µA
ADC block current (2)	I_{ADC}	AV_{REF} = V_{DD} = 5 V	–	1	3	mA
		AV_{REF} = V_{DD} = 3 V		0.5	1.5	
		AV_{REF} = V_{DD} = 5 V Power down mode	–	100	500	nA

NOTES:

1. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is operating current during A/D conversion.

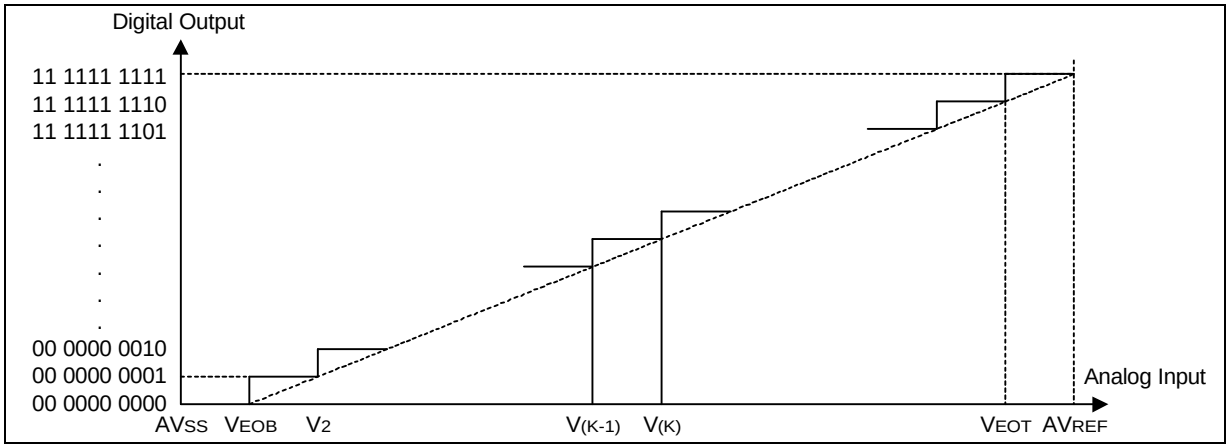


Figure 16-6. Definition of DLE and ILE

Table 16-11. Zero Crossing Detector

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero-crossing detection input voltage	V_{ZC}	AC connection c = 0.1 µF	1.0	–	3.0	Vp-p
Zero-crossing detection accuracy	V_{AZC}	f_{ZC} = 60 Hz (sine wave) V_{DD} = 5 V f_{OSC} = 10 MHz	–	–	± 150	mV
Zero-crossing detection input frequency	f_{ZC}	–	40	–	200	Hz

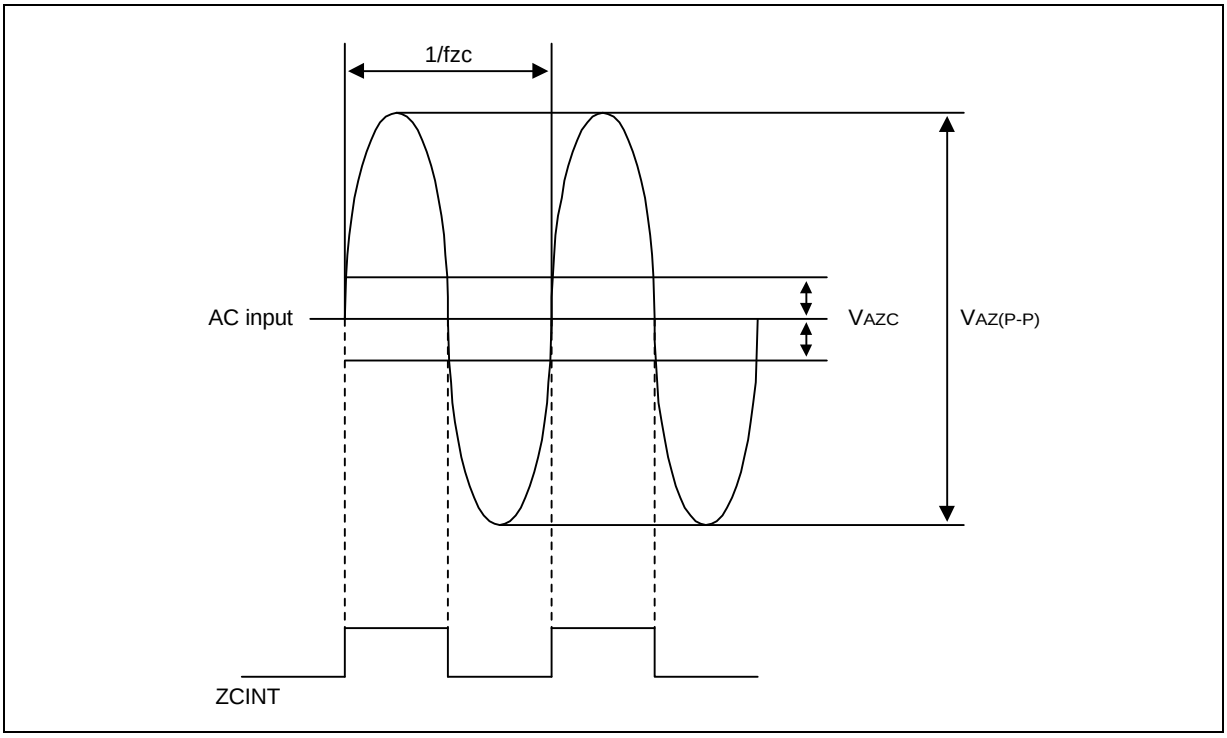
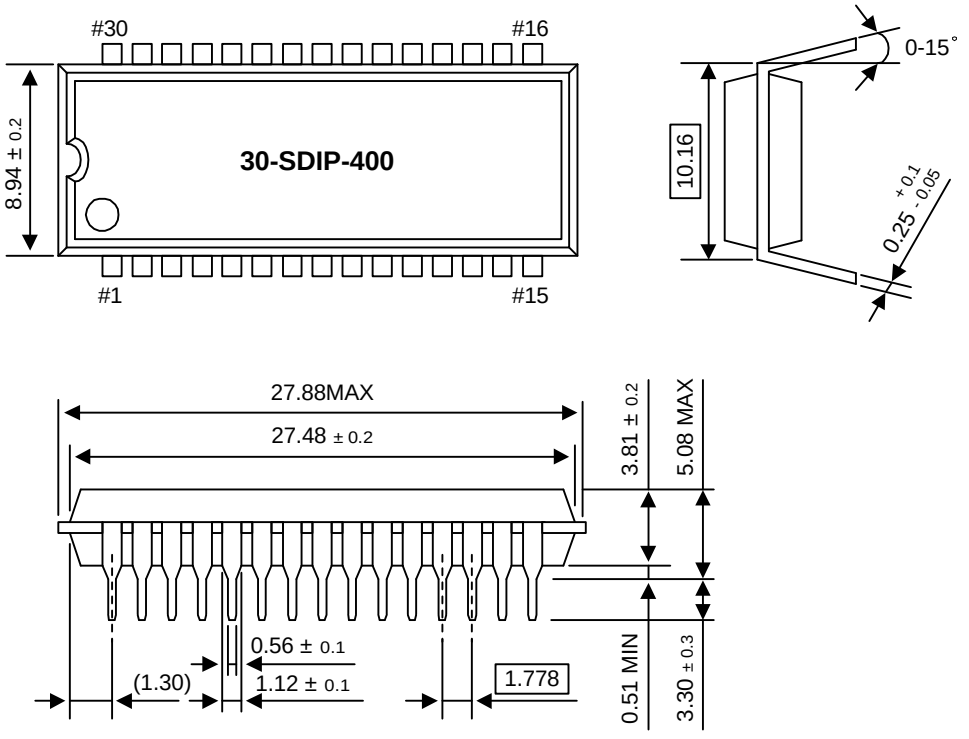


Figure 16-7. Zero Crossing Waveform Diagram

17 MECHANICAL DATA

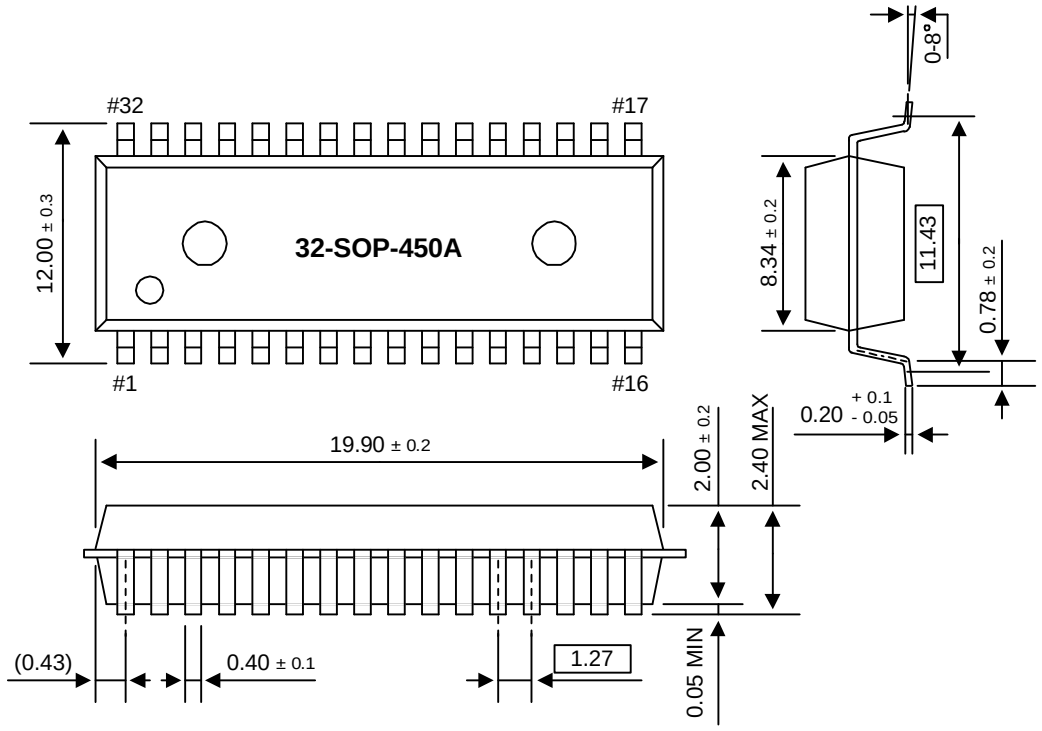
OVERVIEW

The KS86C4204/C4208 is available in a 30-pin SDIP package (Samsung: 30-SDIP-400) and a 32-pin SOP package (32-SOP-450A) and a 28-pin SOP package (28-SOP-375). Package dimensions are shown in Figures 17-1, 17-2, and 17-3



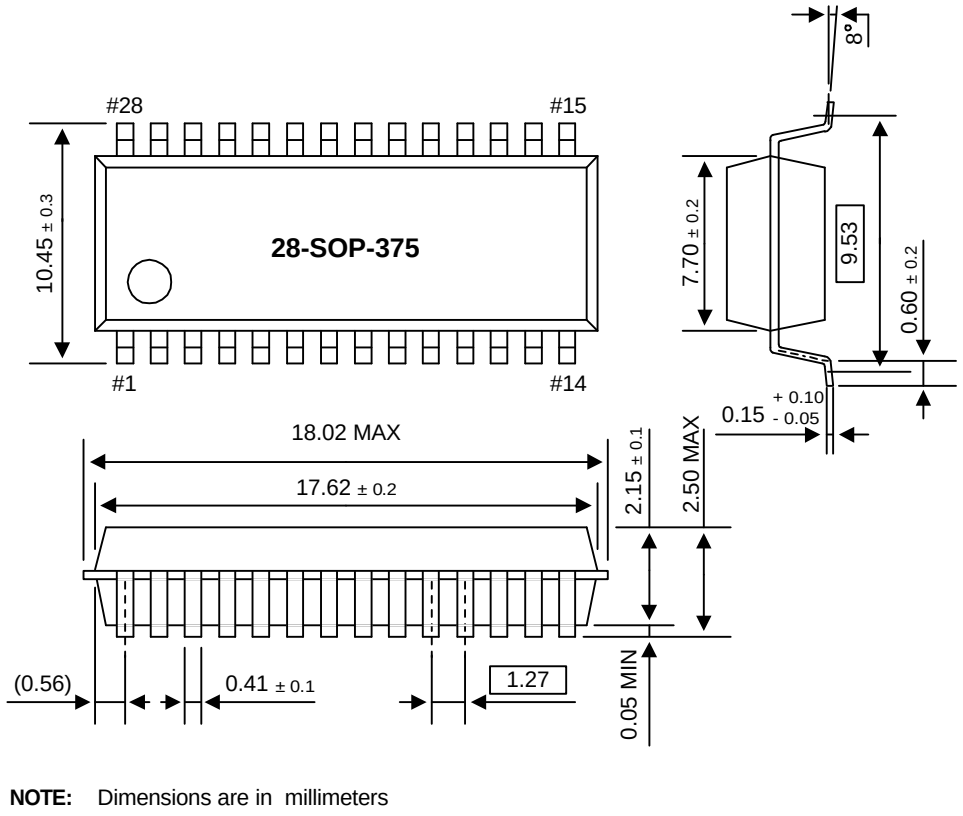
NOTE : Dimensions are in millimeters.

Figure 17-1. 30-Pin SDIP Package Dimensions



NOTE: Dimensions are in millimeters

Figure 17-2. 32-SOP-450A Package Dimensions



NOTE: Dimensions are in millimeters

Figure 17-3. 28-SOP-375 Package Dimensions

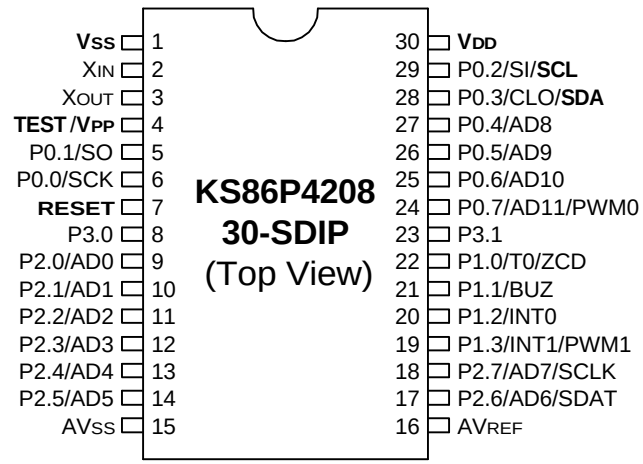
NOTES

18 KS86P4208 OTP

OVERVIEW

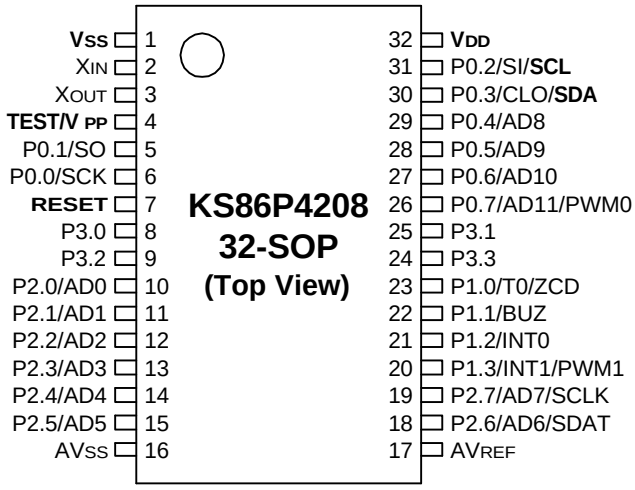
The KS86P4208 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS86C4204/C4208 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS86P4208 is fully compatible with the KS86C4204/C4208, both in function and in pin configuration. Because of its simple programming requirements, the KS86P4208 is ideal for use as an evaluation chip for the KS86C4204/C4208.



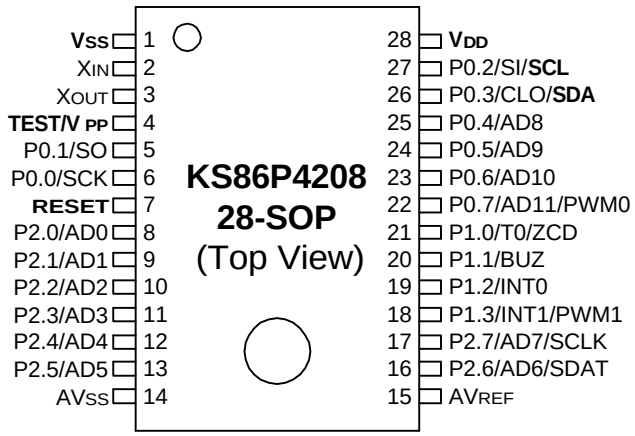
NOTE: The bolds indicate an OTP pin name.

Figure 18-1. Pin Assignment Diagram (30-Pin SDIP Package)



NOTE: The bolds indicate an OTP pin name.

Figure 18-2. Pin Assignment Diagram (32-Pin SOP Package)



NOTE: The bolds indicate an OTP pin name.

Figure 18-3. Pin Assignment Diagram (28-Pin SOP Package)

Table 18-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.3	SDAT	KS86P4208 - 30 SDIP: 28 - 32 SOP: 30	I/O	Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned
P0.2	SCLK	KS86P4208 - 30 SDIP: 29 - 32 SOP: 31	I	Serial clock pin (input only pin)
TEST	V_{PP} (TEST)	4	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	7	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	KS86P4208 - 30 SDIP: 30/1 - 32 SOP: 32/1	I	Logic power supply pin.

Table 18-2. Comparison of KS86P4208 and KS86C4204/C4208 Features

Characteristic	KS86P4208	KS86C4204/C4208
Program Memory	8-Kbyte EPROM	4/8-Kbyte mask ROM
Operating Voltage (V_{DD})	3.0 V to 5.5 V (28 SOP: 1.8 V to 5.5)	3.0 V to 5.5 V (28 SOP: 1.8 V to 5.5)
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	
Pin Configuration	30 SDIP/32 SOP/28SOP	
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the KS86P4208, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 18-3 below.

Table 18-3. Operating Mode Selection Criteria

V_{DD}	V_{pp} (TEST)	REG/MEM	ADDRESS(A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

NOTES