

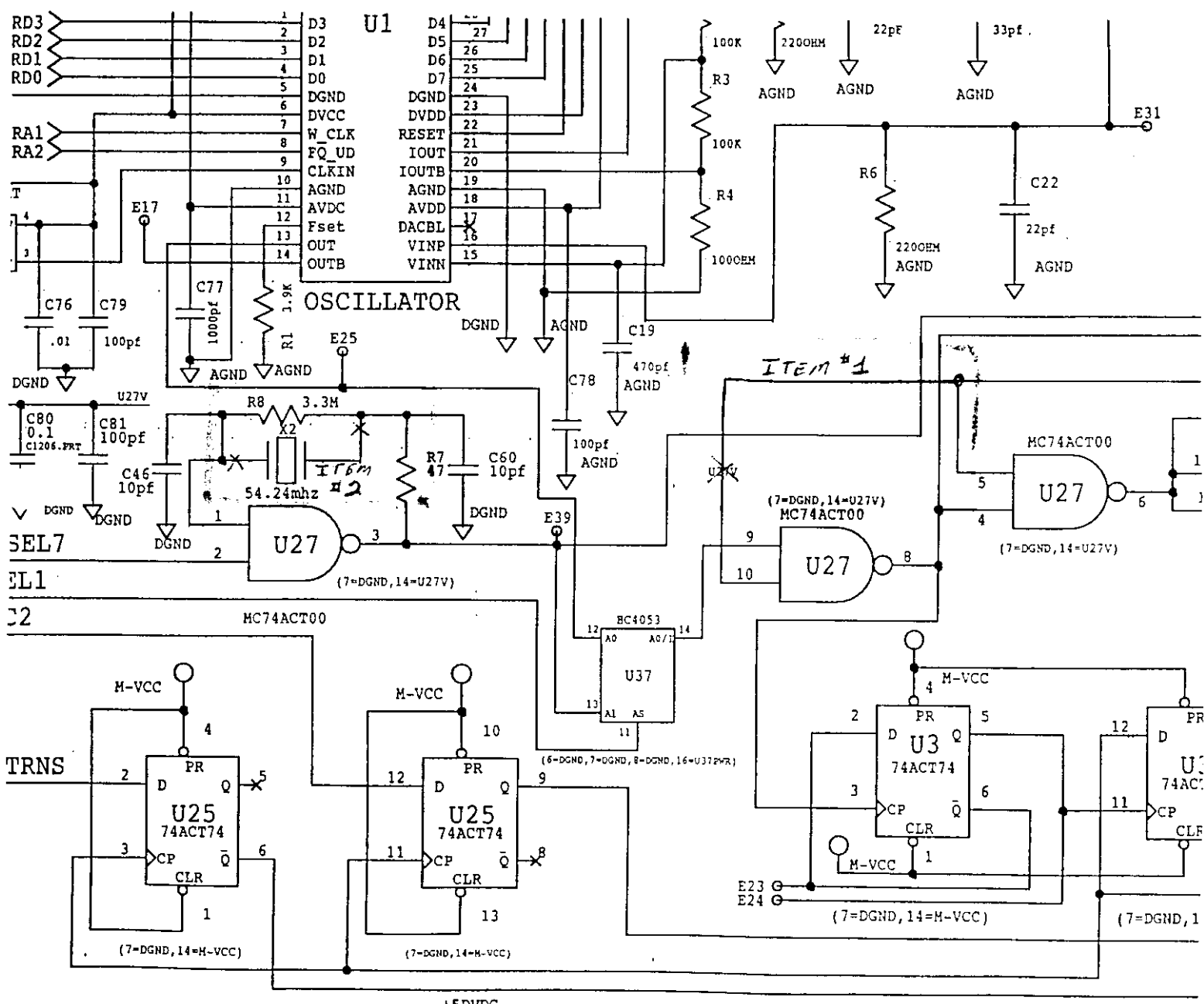
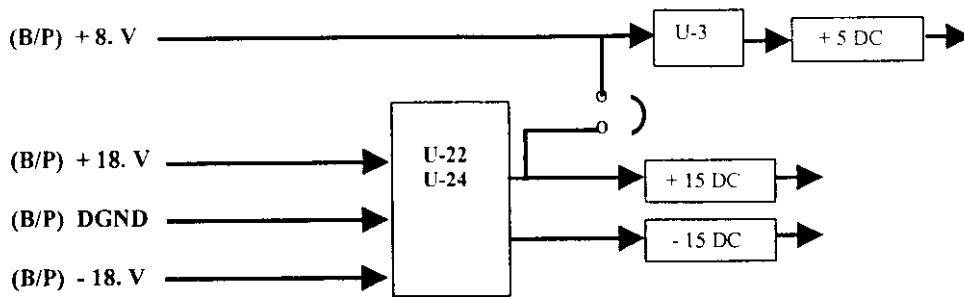


EXHIBIT B.5

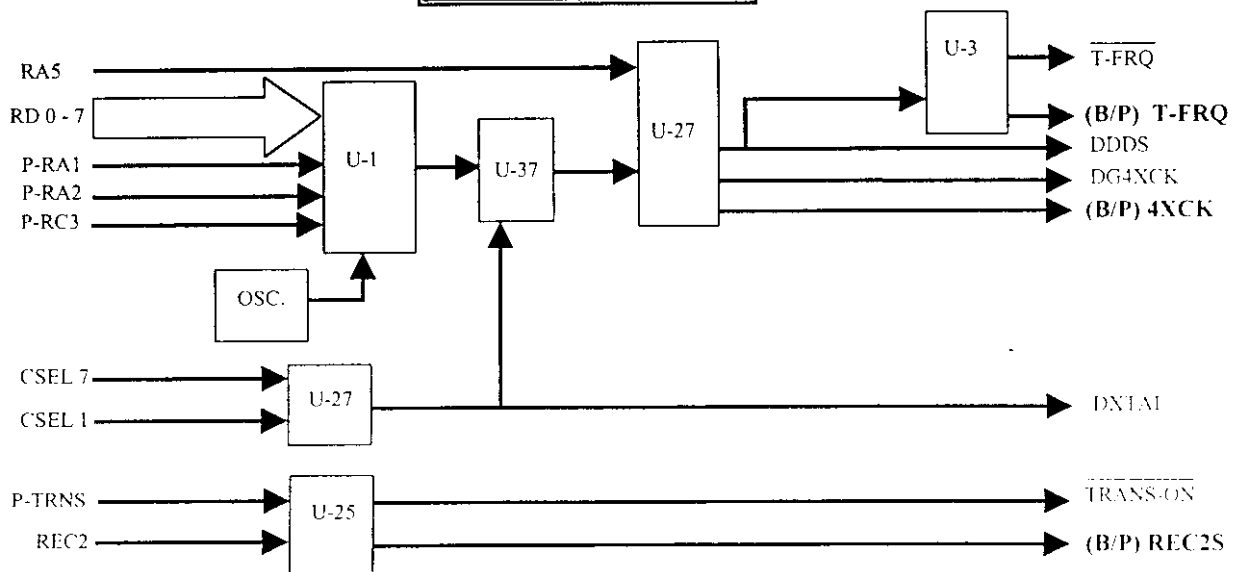
**Block and Schematic Diagrams
Showing Frequency of all Oscillators**

UMS TRANSMITTER CARD

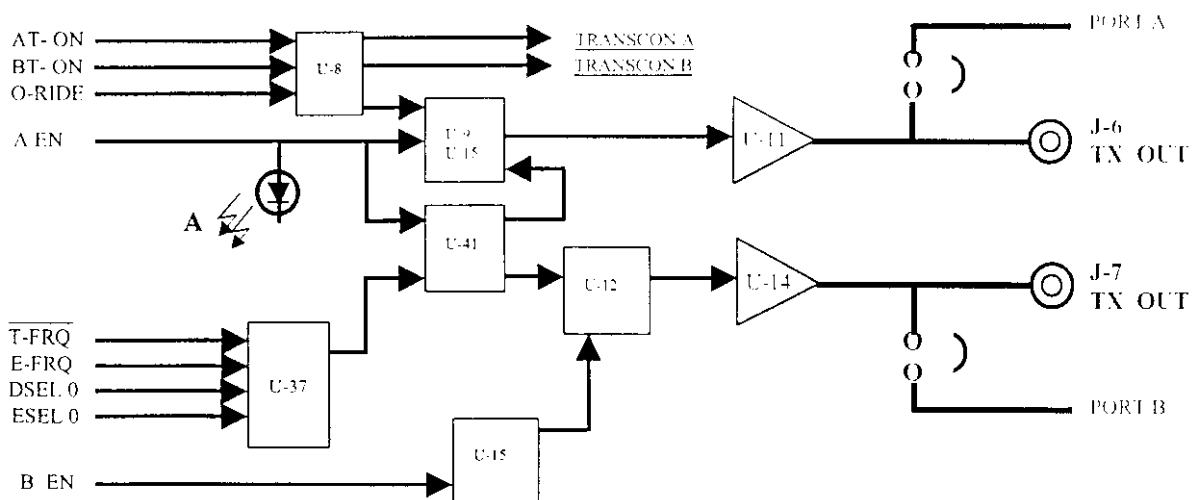
PWR. SUPPLY



DDS OSCILLATOR



FUNCTION GENERATOR

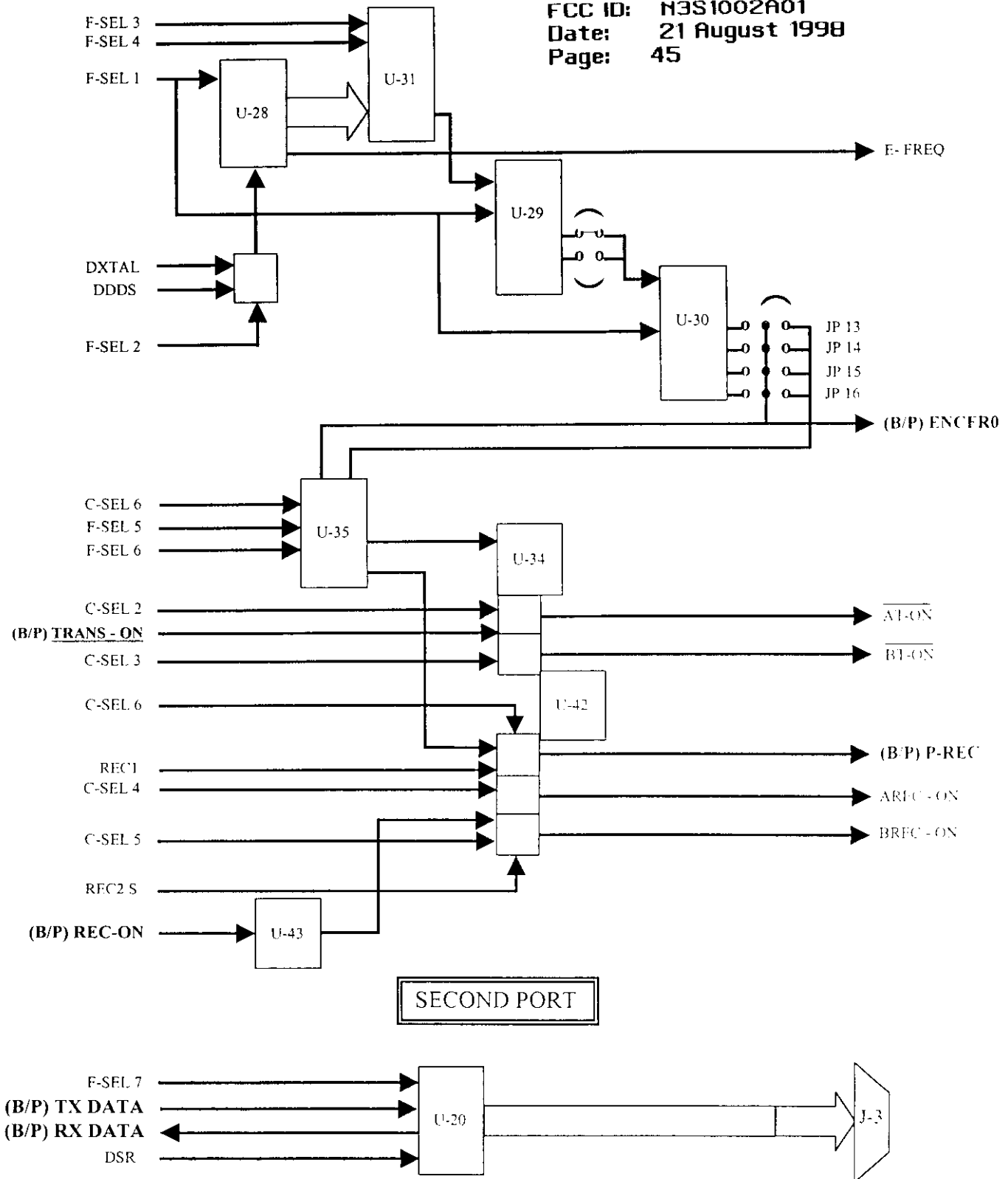


FCC ID: N3S1002A01
Date: 21 August 1998
Page: 44

UMS TRANSMITTER CARD

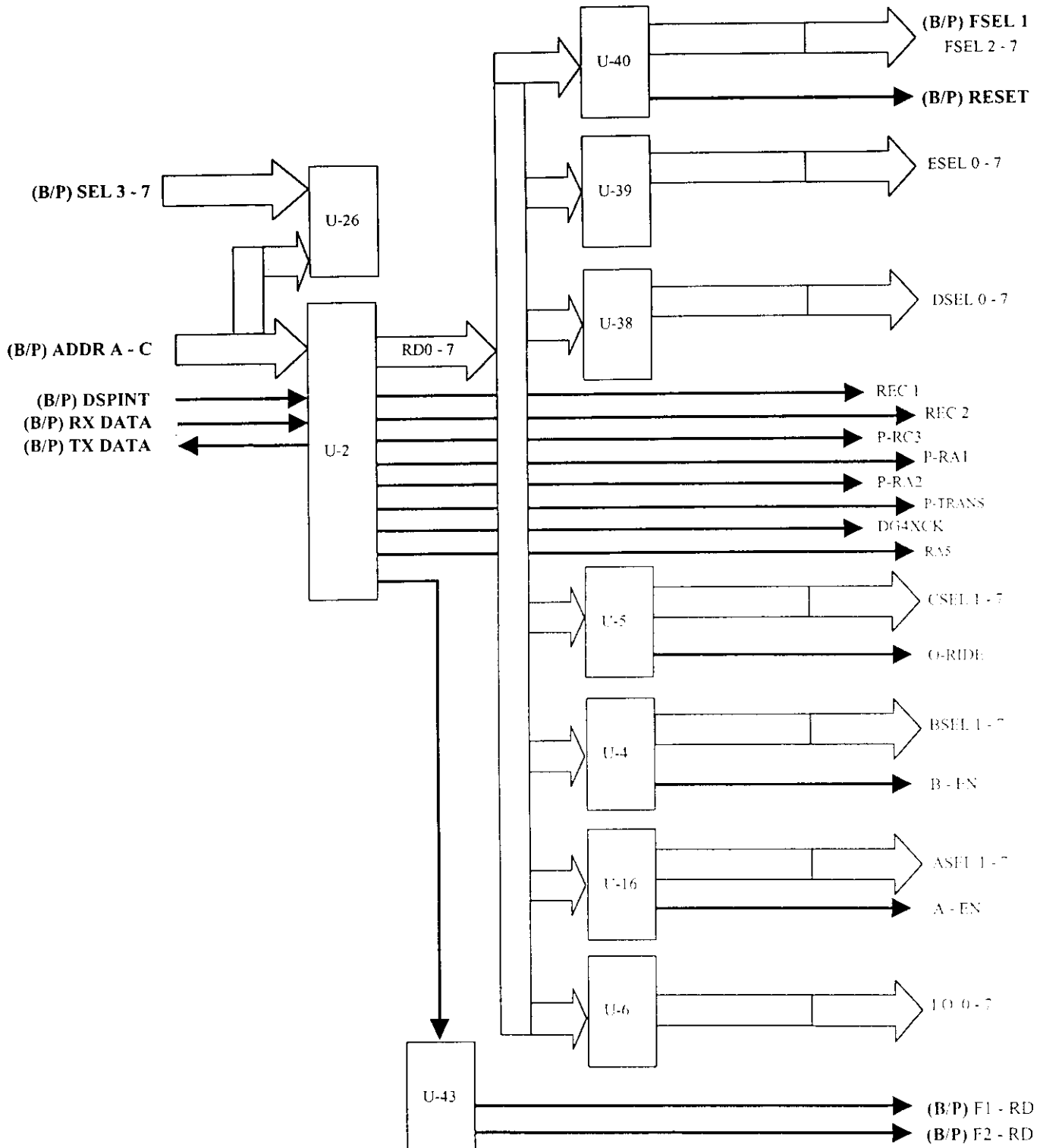
MODE SELECT

FCC ID: N3S1002A01
Date: 21 August 1998
Page: 45



UMS TRANSMITTER CARD

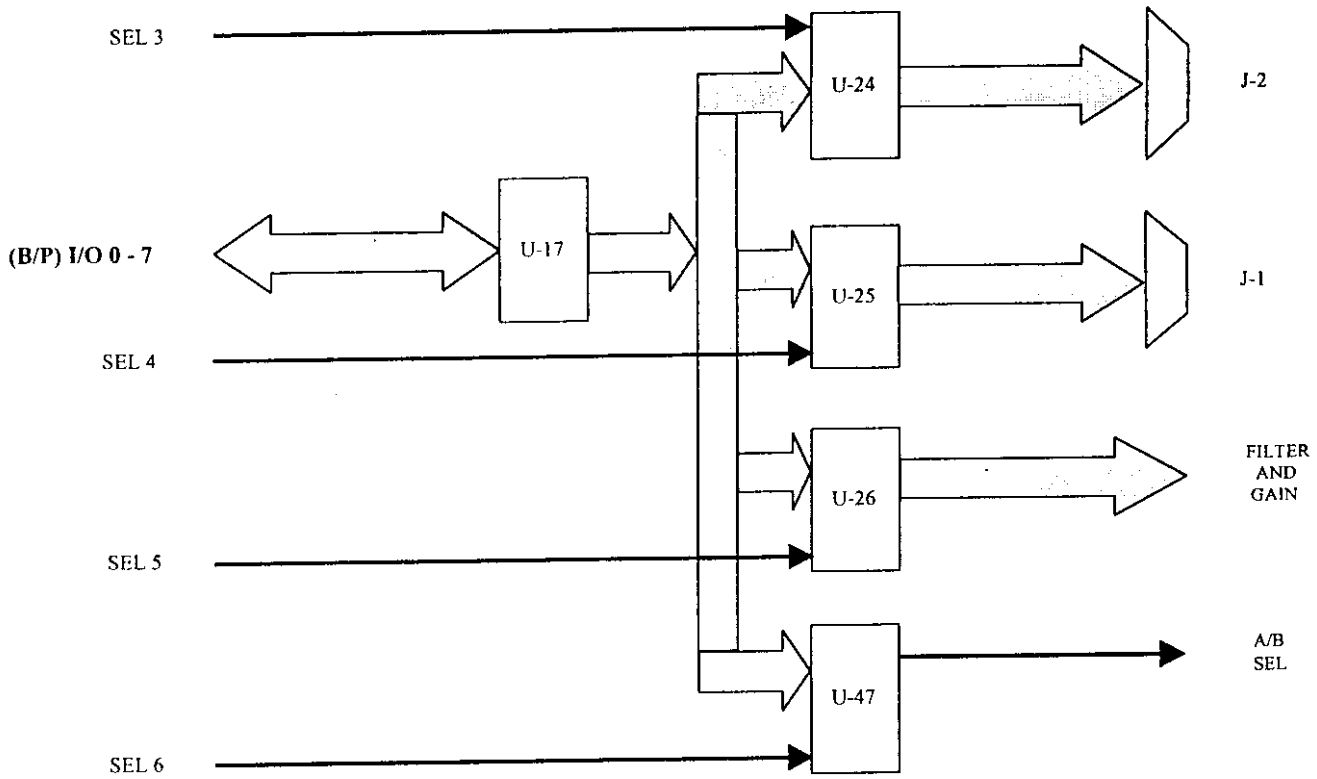
ADDRESS DECODER



UMS RECEIVER CARD

FCC ID: M3S1002A01
Date: 21 August 1998
Page: 46A

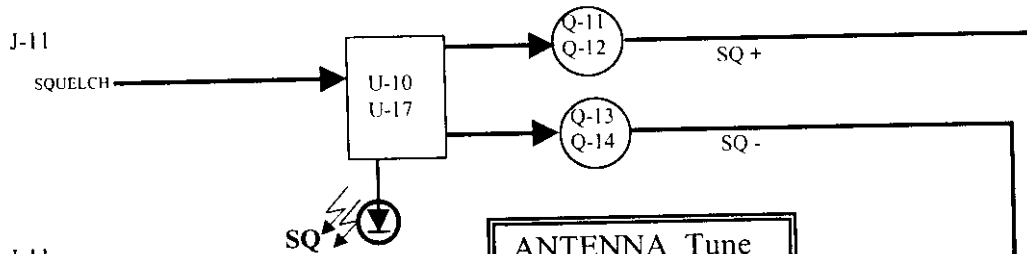
INTERFACE LOGIC



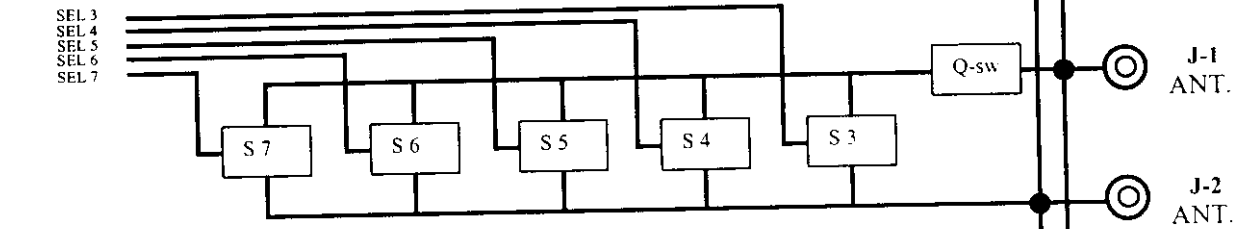
UMS TAP RX/TX CARD

FCC ID: N3S1002A01
Date: 21 August 1998
Page: 74

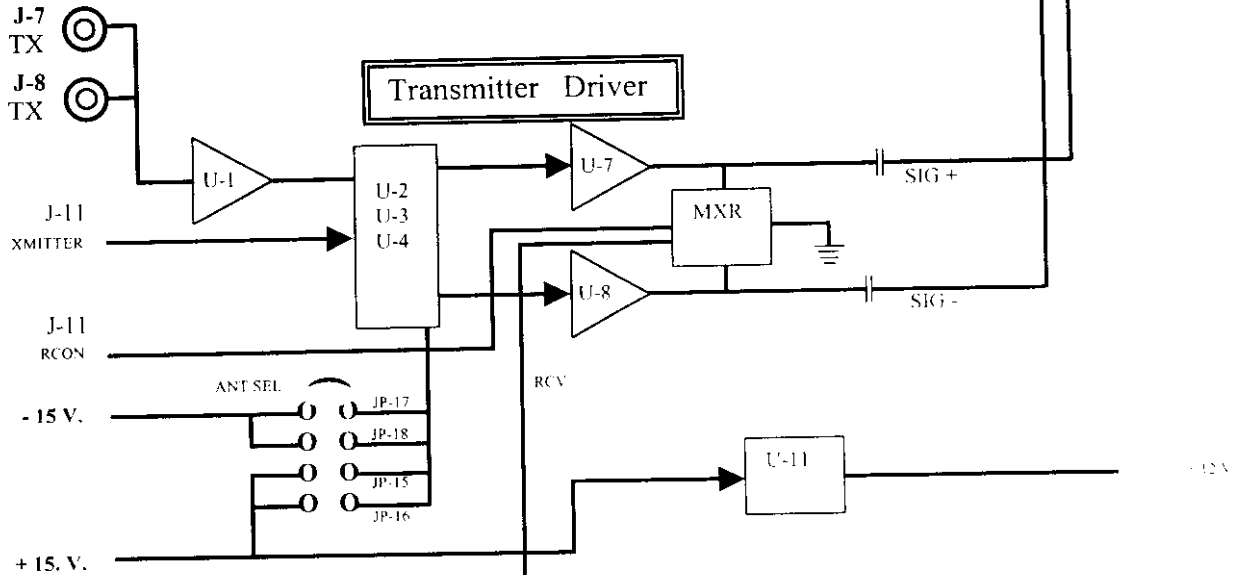
ANTENNA Squelch



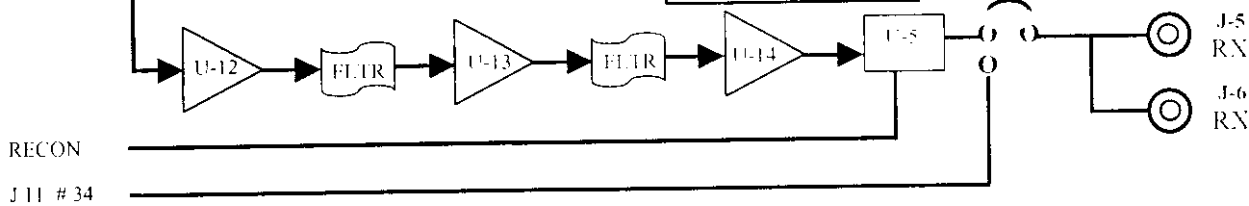
ANTENNA Tune



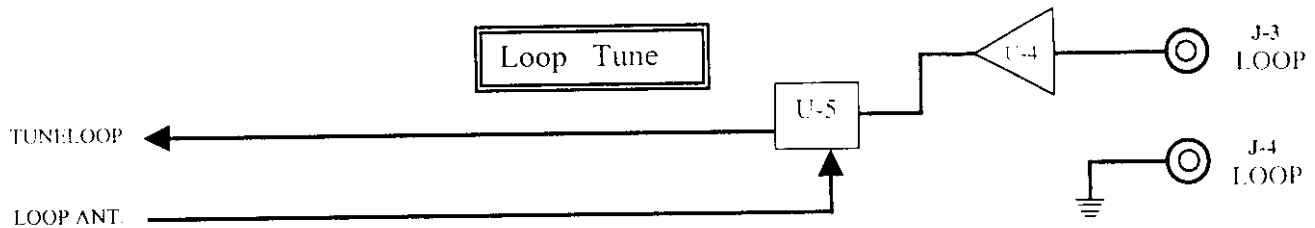
Transmitter Driver



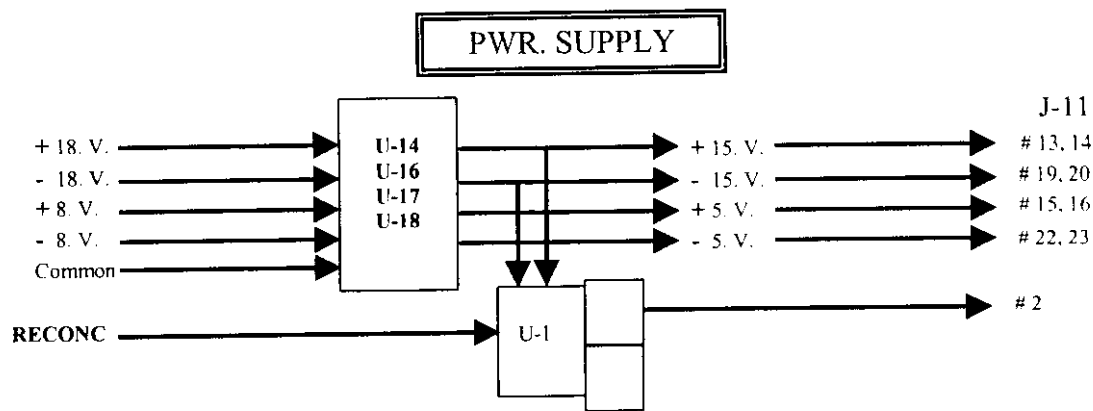
Receiver Path



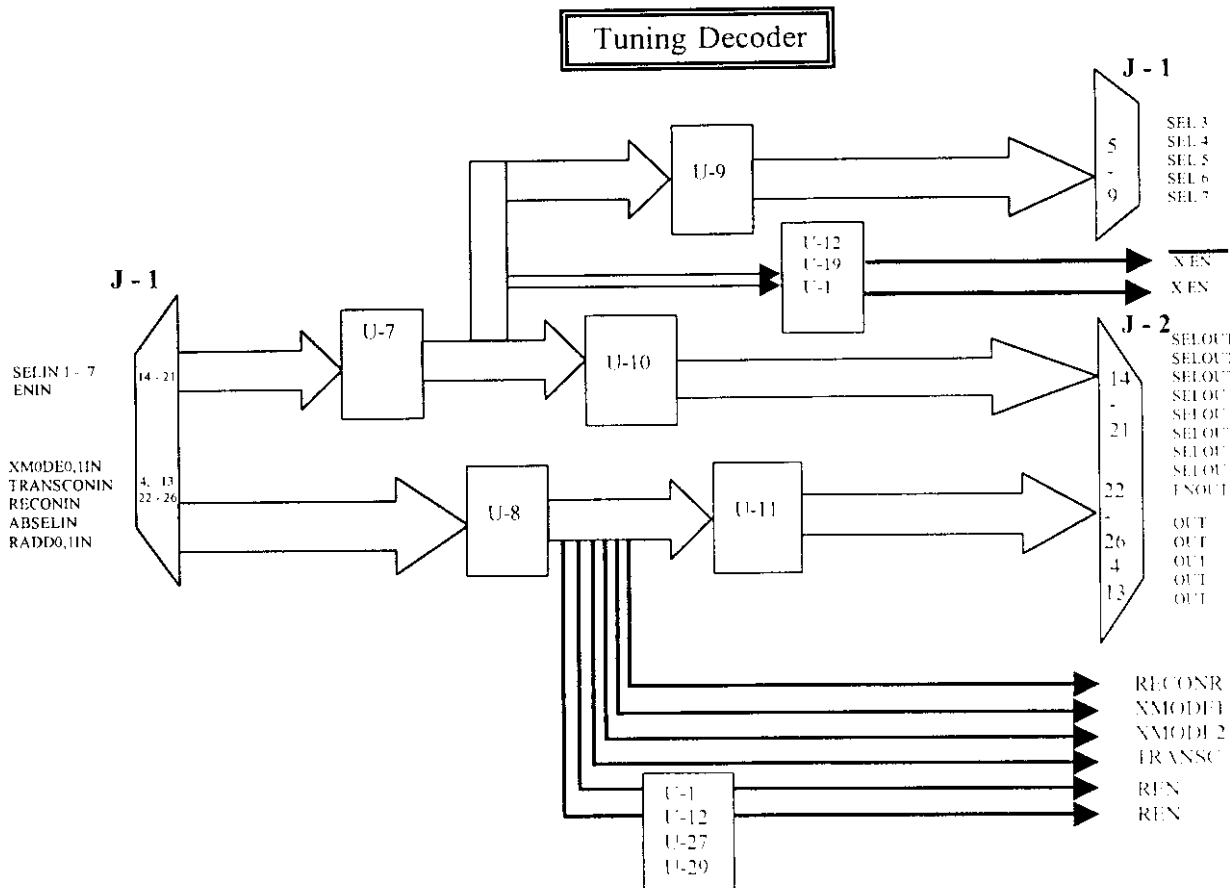
Loop Tune



UMS TAP CONTROLLER CARD



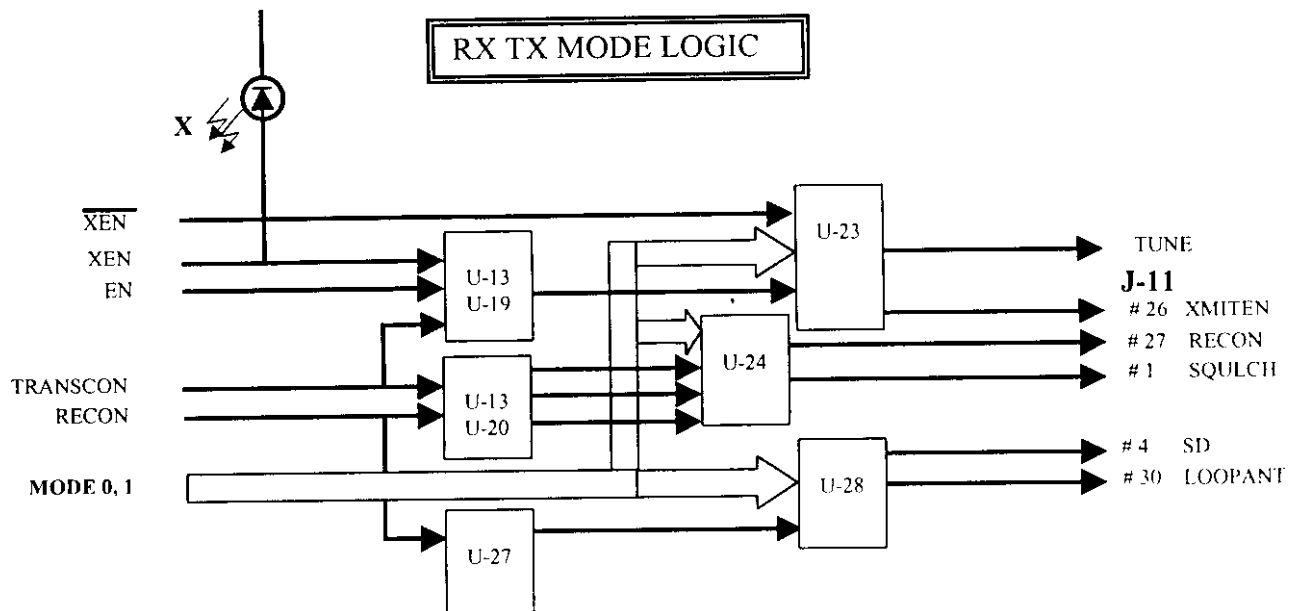
FCC ID: N3S1002A01
 Date: 21 August 1998
 Page: 79



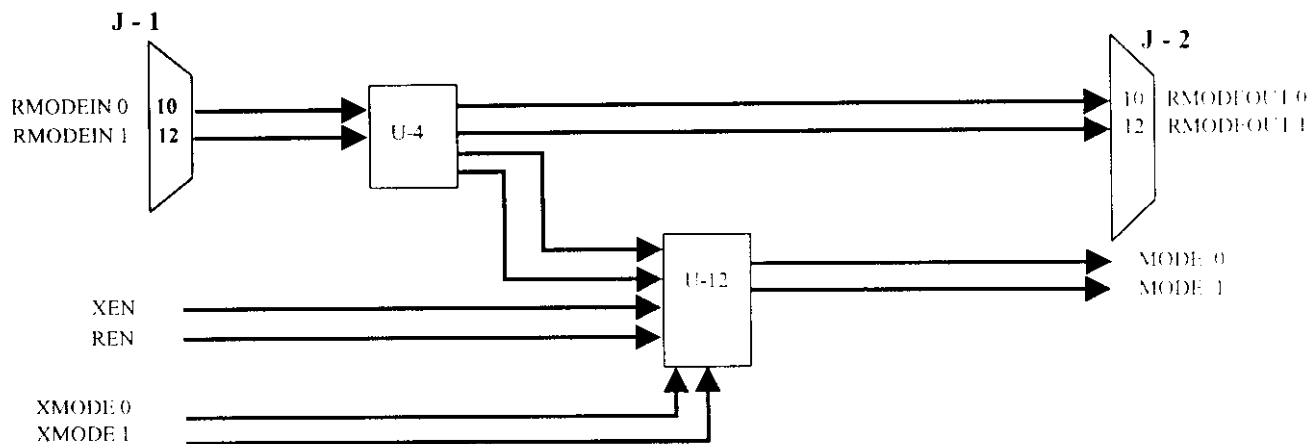
UMS TAP CONTROLLER CARD

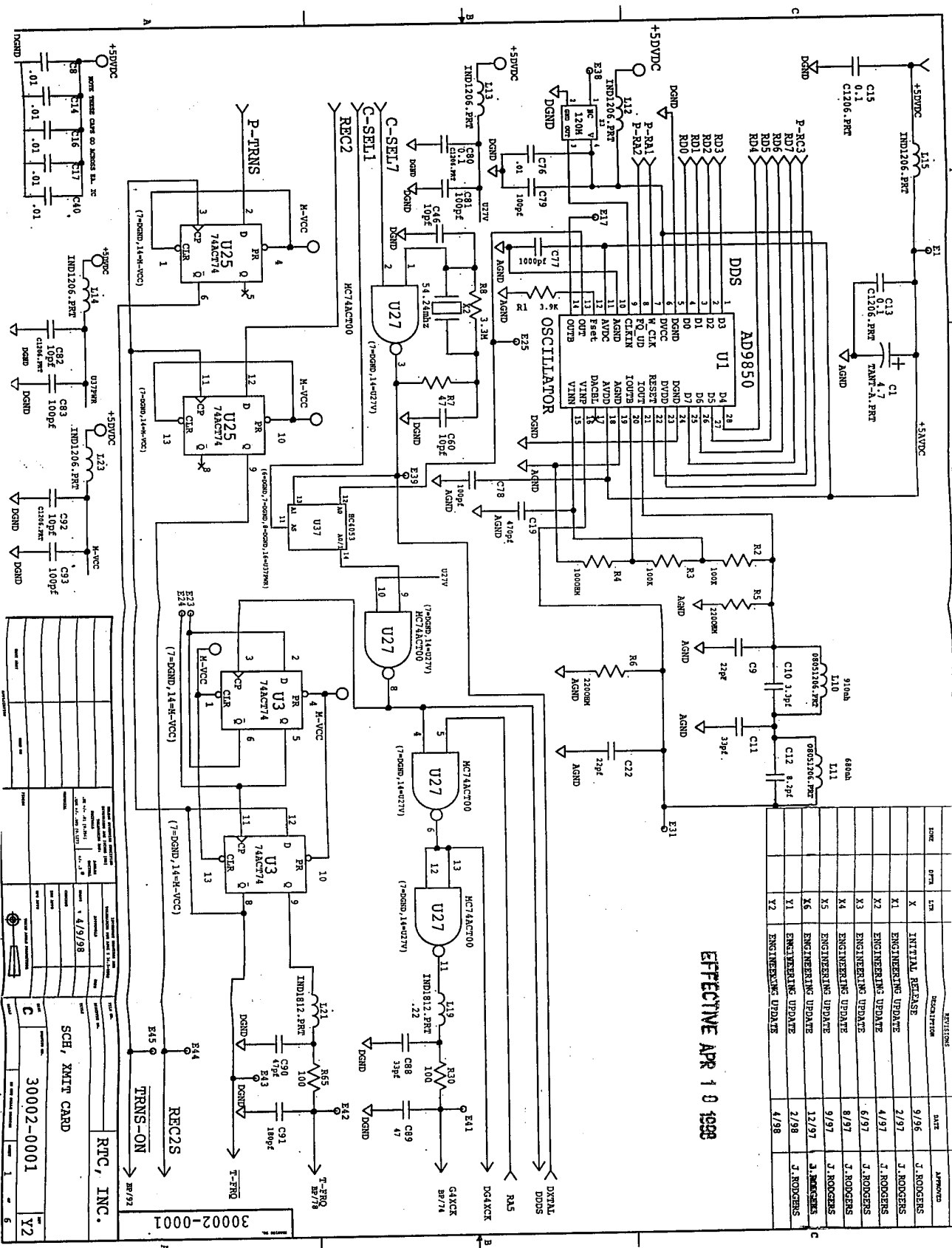
FIG. 10: NGSD002R01
Date: 21 August 1990
Page: 00

RX TX MODE LOGIC



MODE DECODE





EFFECTIVE APR 10 1998

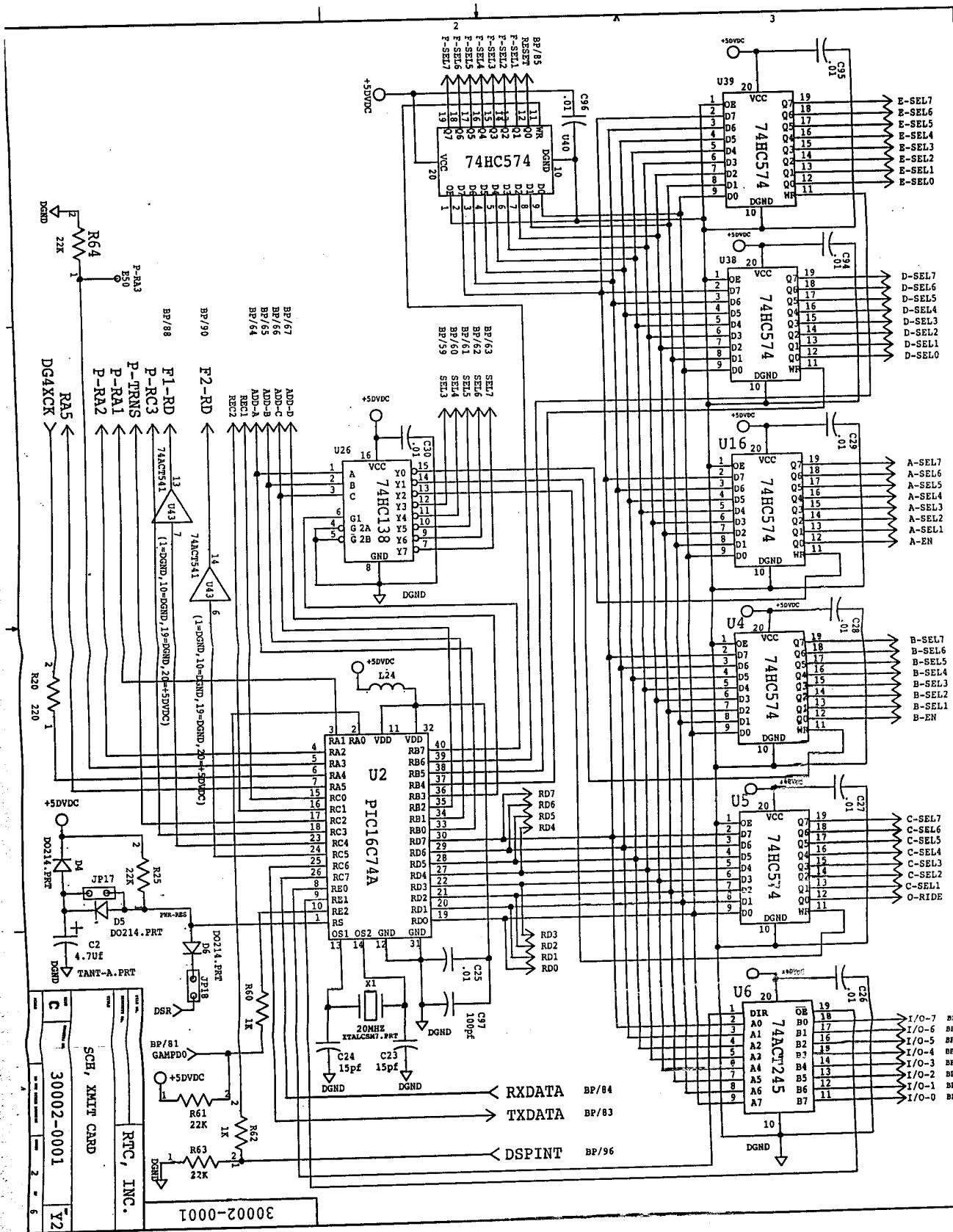
30002-0001

SCH, XMIT CARD

30002-0001

Y2

RECEIVED



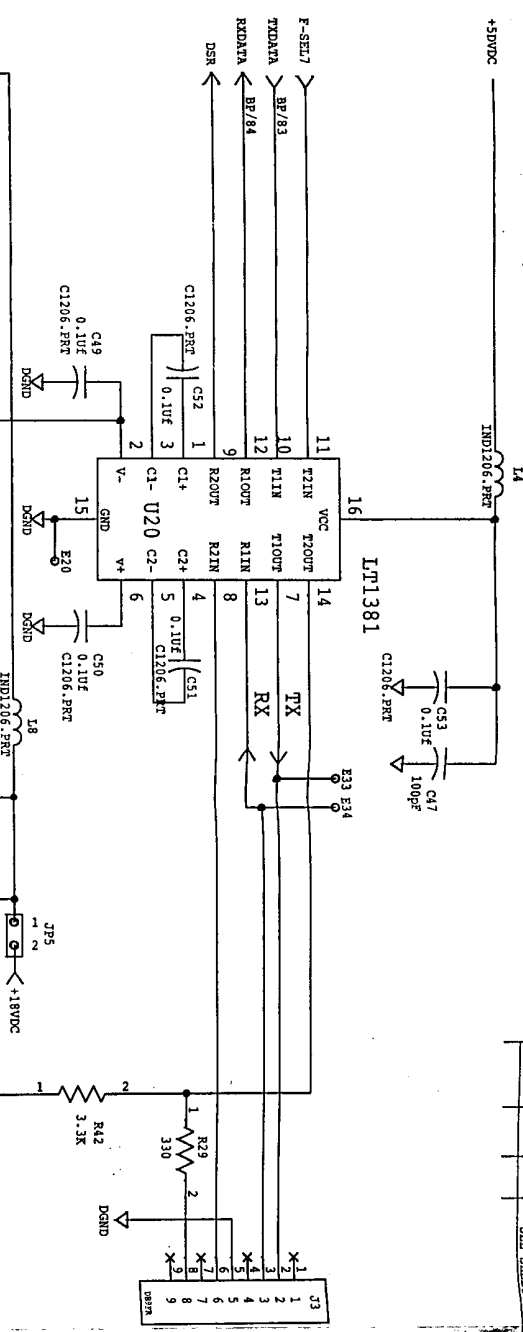
COPY

EFFECTIVE 4-10-1992

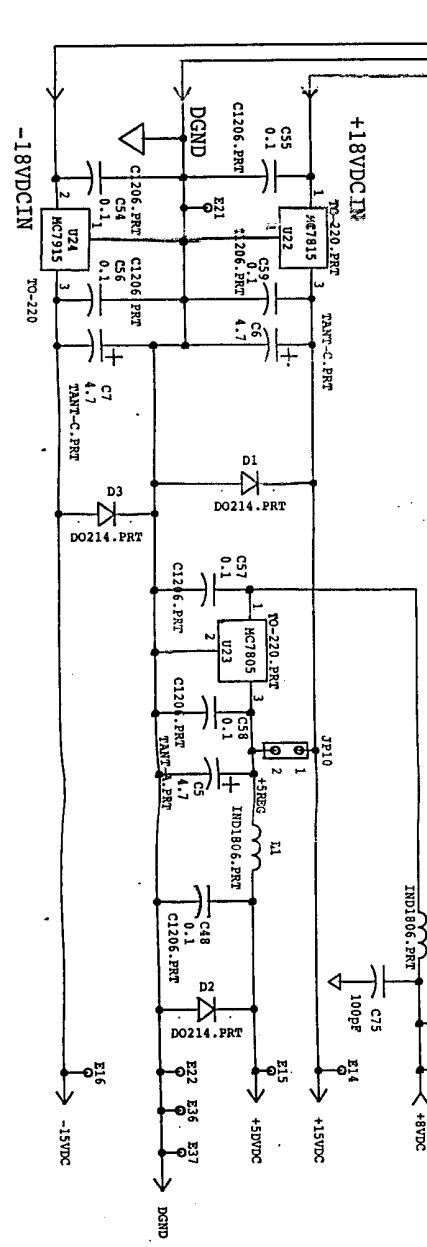
FCC ID: N3S1002A01
Date: 21 August 1992
Page: 48

REV	DATE	APPROVED
1		
2		
3		
4		

SERIAL PORT



POWER REGULATORS



30002-0001	Y2
SCE, XMIT CARD	
RTC, INC.	

ORIGINAL
EFFECTIVE APR 10 1998

100

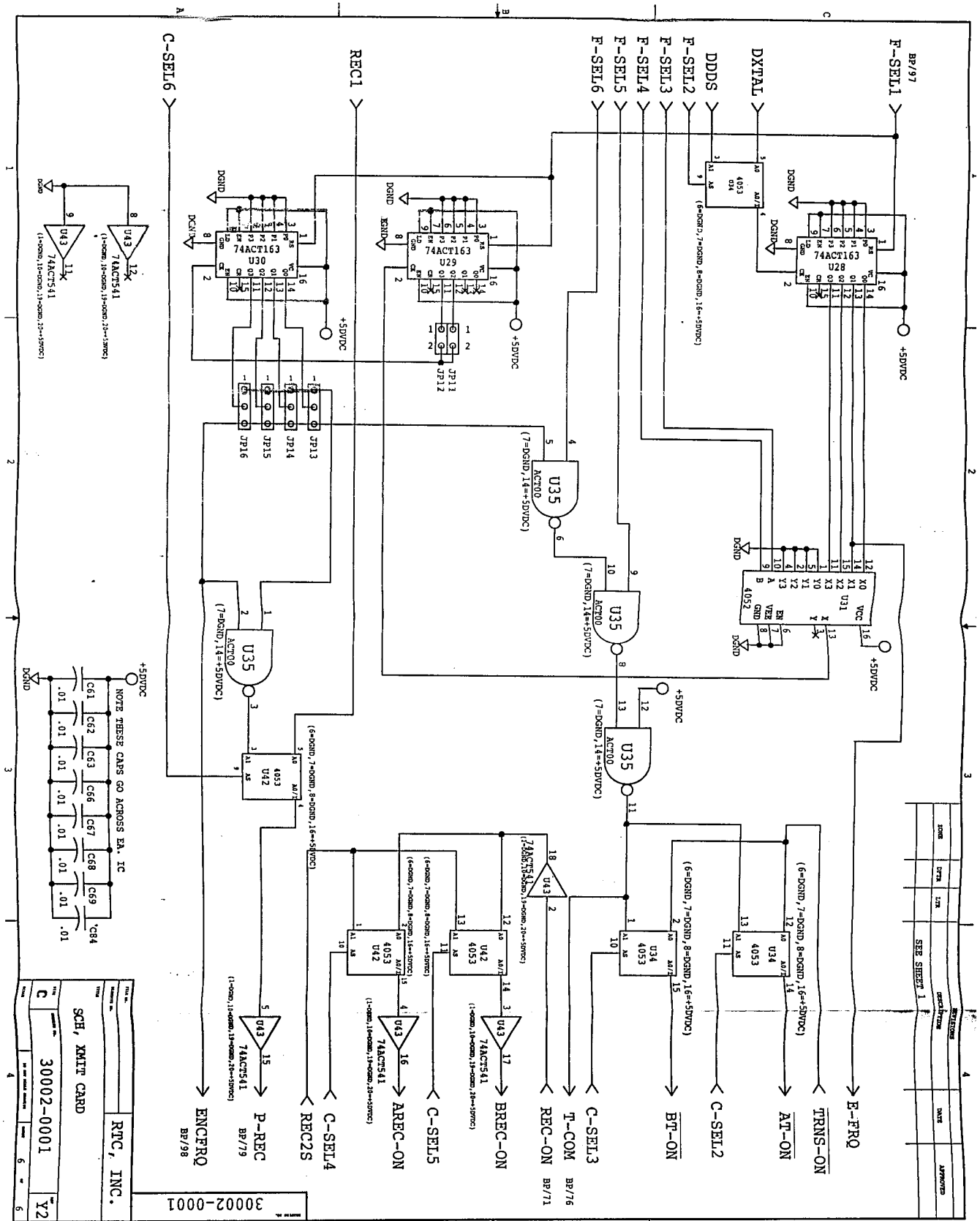
1	SGND
2	D-GND
3	+18VDC
4	TRNSCONA
5	+18VDC
6	D-GND
7	D-GND
8	PORT-A
9	-18VDC
10	D-SEL4
11	D-GND
12	D-SEL5
13	D-SEL7
14	A-SEL7
15	A-SEL6
16	A-SEL5
17	A-SEL4
18	A-SEL3
19	B-SEL2
20	B-SEL1
21	B-SEL
22	E-SEL3
23	E-SEL2
24	E-SEL1
25	REC-ON
26	E-SEL7

1	SGND
2	D-GND
3	+18VDC
4	TRNSCONA
5	+18VDC
6	D-GND
7	D-GND
8	PORT-A
9	-18VDC
10	D-SEL4
11	D-GND
12	D-SEL5
13	D-SEL7
14	A-SEL7
15	A-SEL6
16	A-SEL5
17	A-SEL4
18	A-SEL3
19	B-SEL2
20	B-SEL1
21	B-SEL
22	E-SEL3
23	E-SEL2
24	E-SEL1
25	REC-ON
26	E-SEL7

[illegible][illegible]

RTC, INC.	
TITLE NO. ORDERING NO. PART NO.	SCF, KMIT CARD 30002-0001 YZ

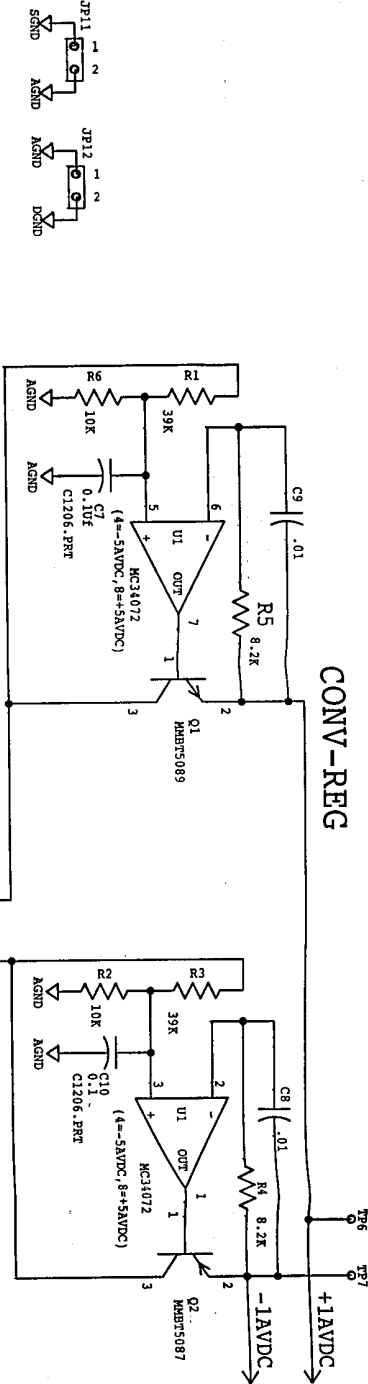
ORIGINAL COPY
EFFECTIVE APR 10 1999



COPY

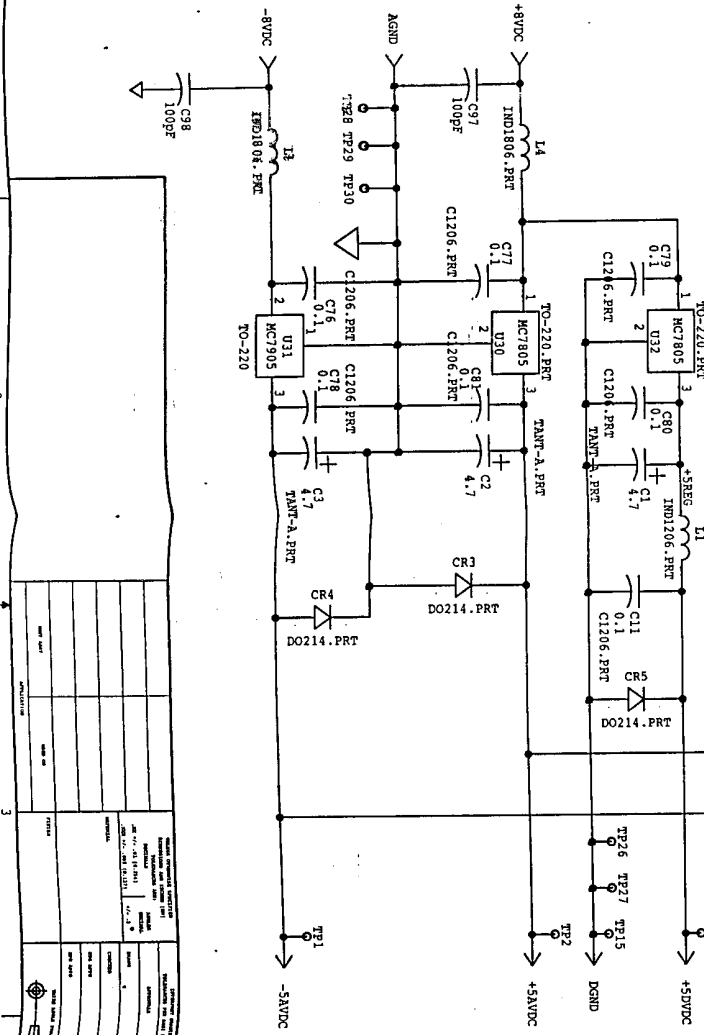
EFFECTIVE APR 10

DATE	APPROVED	REVISION	DESCRIPTION
9/96	J. RODGERS	X	INITIAL RELEASE
2/97	J. RODGERS	X1	ENGINEERING UPDATE
5/97	J. RODGERS	X2	ENGINEERING UPDATE
9/97	J. RODGERS	X3	ENGINEERING UPDATE
1/98	J. RODGERS	X4	ENGINEERING UPDATE
4/98	J. RODGERS	Y2	ENGINEERING UPDATE



*STAR CONNECTION OF
18GND (BP4)
D8ND PLANE AND
U32-2 GND PIN.

*STAR CONNECTION OF
8GND (BP8)
D8ND PLANE AND
U30-2 GND PIN.
U31-1 GND PIN.



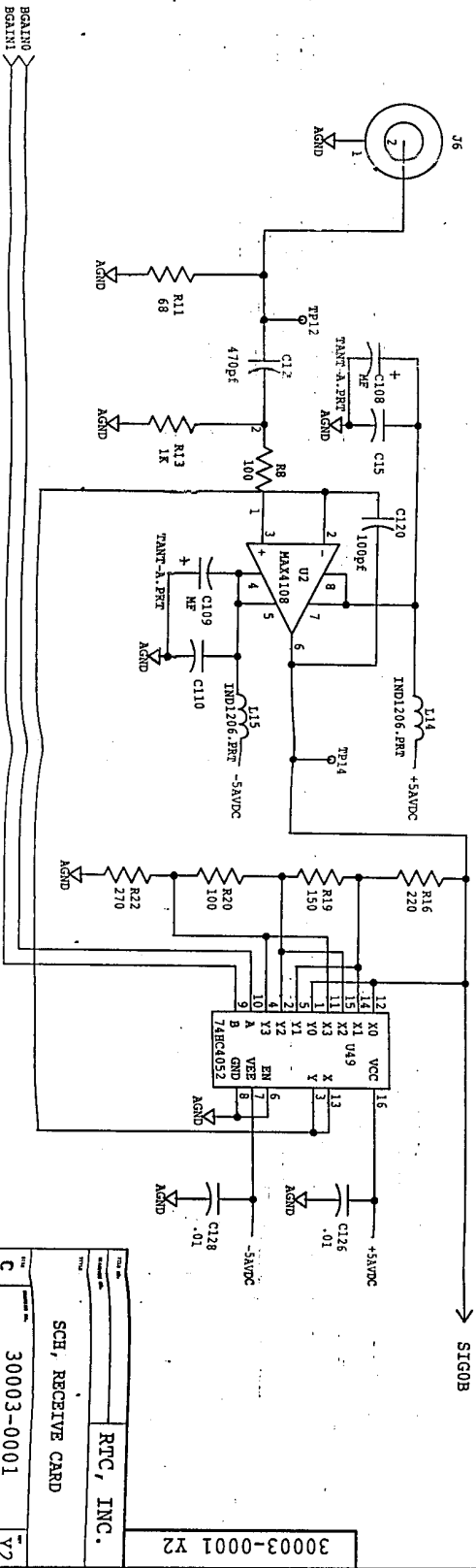
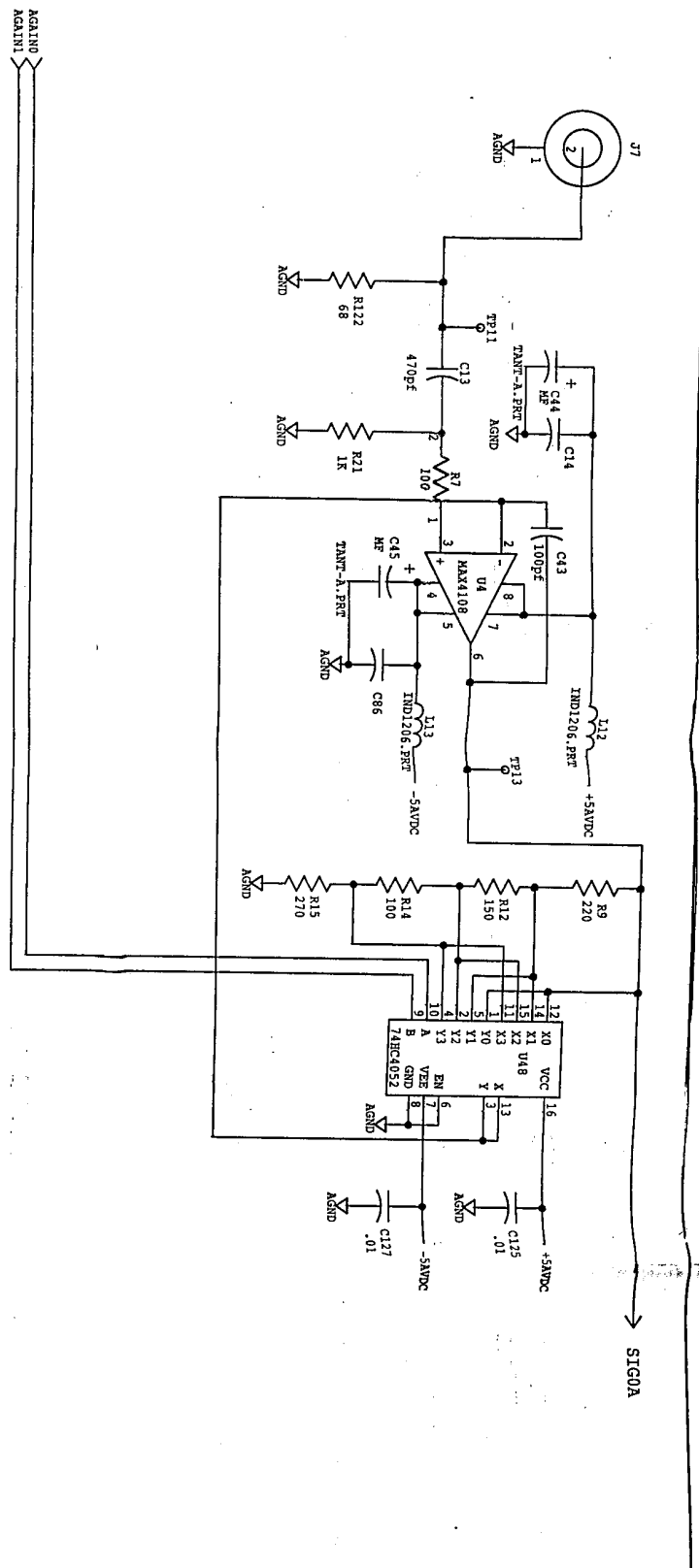
30003-0001 Y2

SCH, RECEIVE CARD

30003-0001

Y2

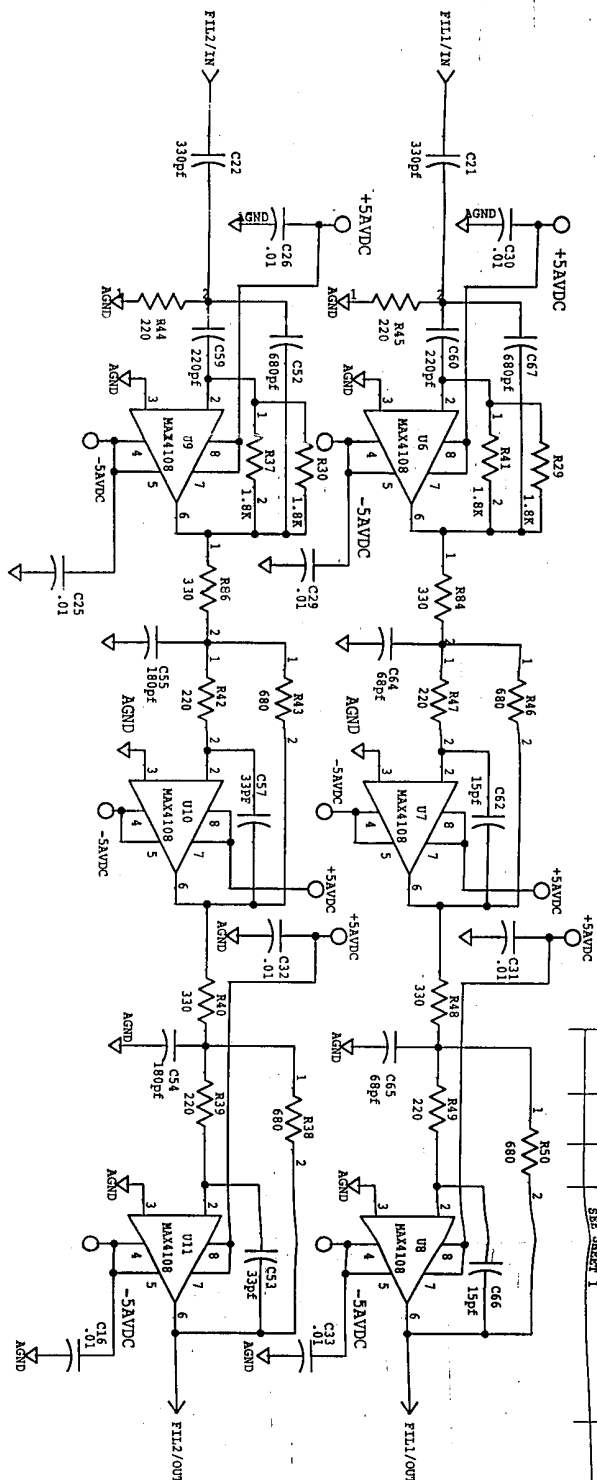
RTC, INC.



30003-0001 Y2	
RTC, INC.	
SCH, RECEIVE CARD	
C	30003-0001
Y2	

DATE	DATE	DATE	DATE	DATE
DATE	DATE	DATE	DATE	DATE
DATE	DATE	DATE	DATE	DATE
DATE	DATE	DATE	DATE	DATE
DATE	DATE	DATE	DATE	DATE

SEE SHEET 1



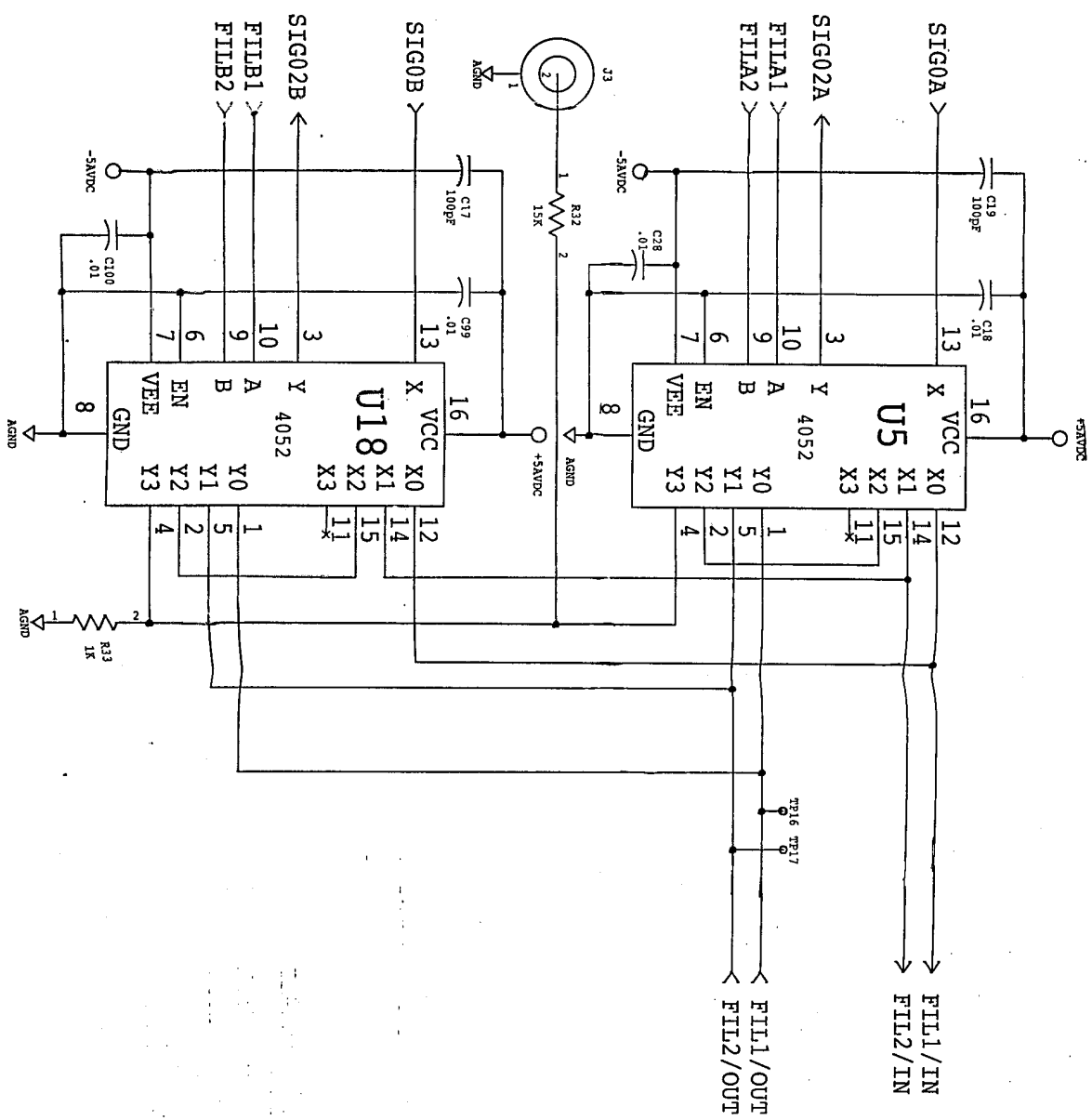
SCH, RECEIVE CARD		RTC, INC.	
30003-0001		Y2	

EFFECTIVE A

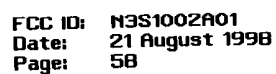
FCC ID: N3S1002A01
Date: 21 August 1998
Page: 56

REV	DATE	APPROVED
1		
2		
3		
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5		
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7		
8		
9		
10		

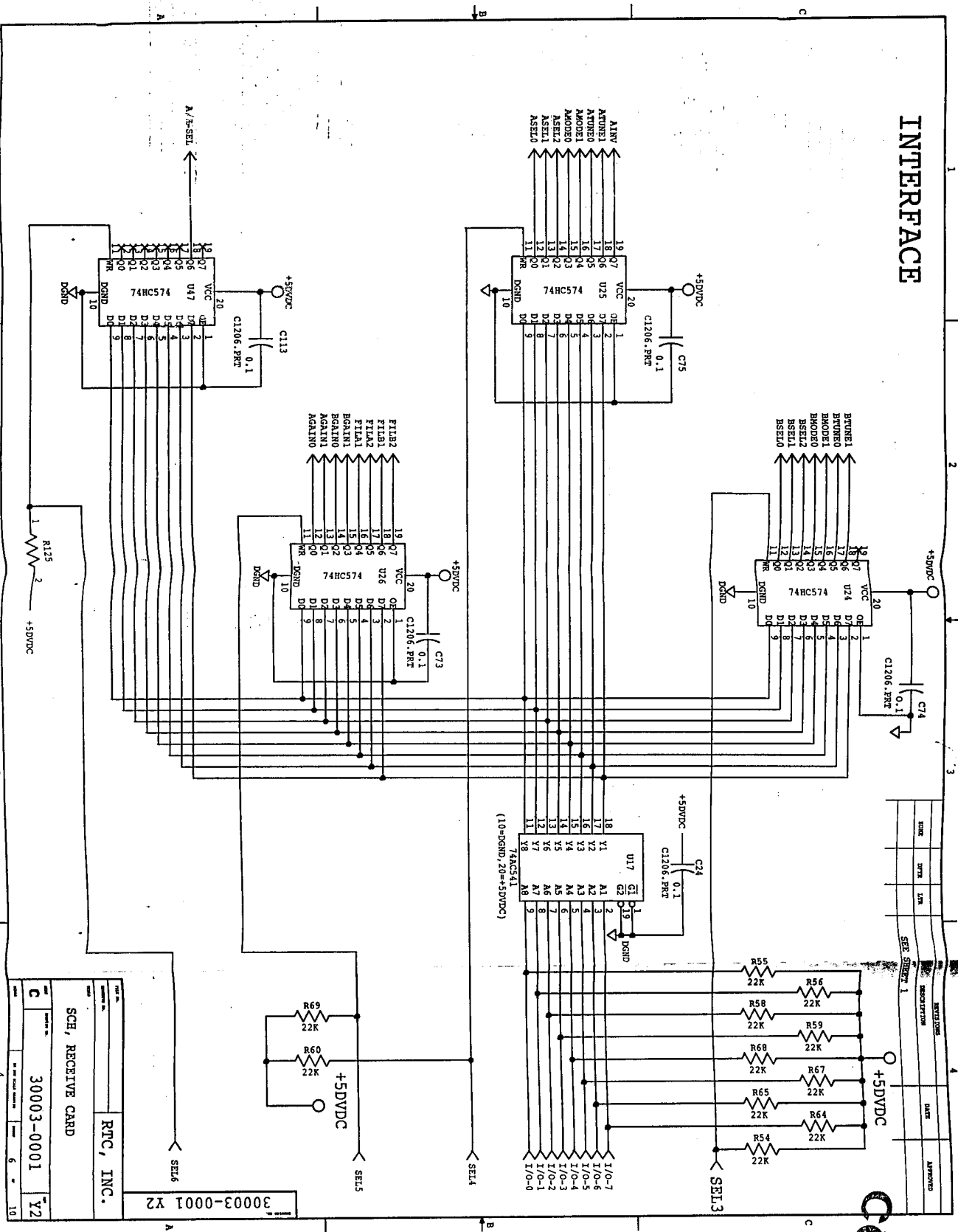
SEE SHEET 1



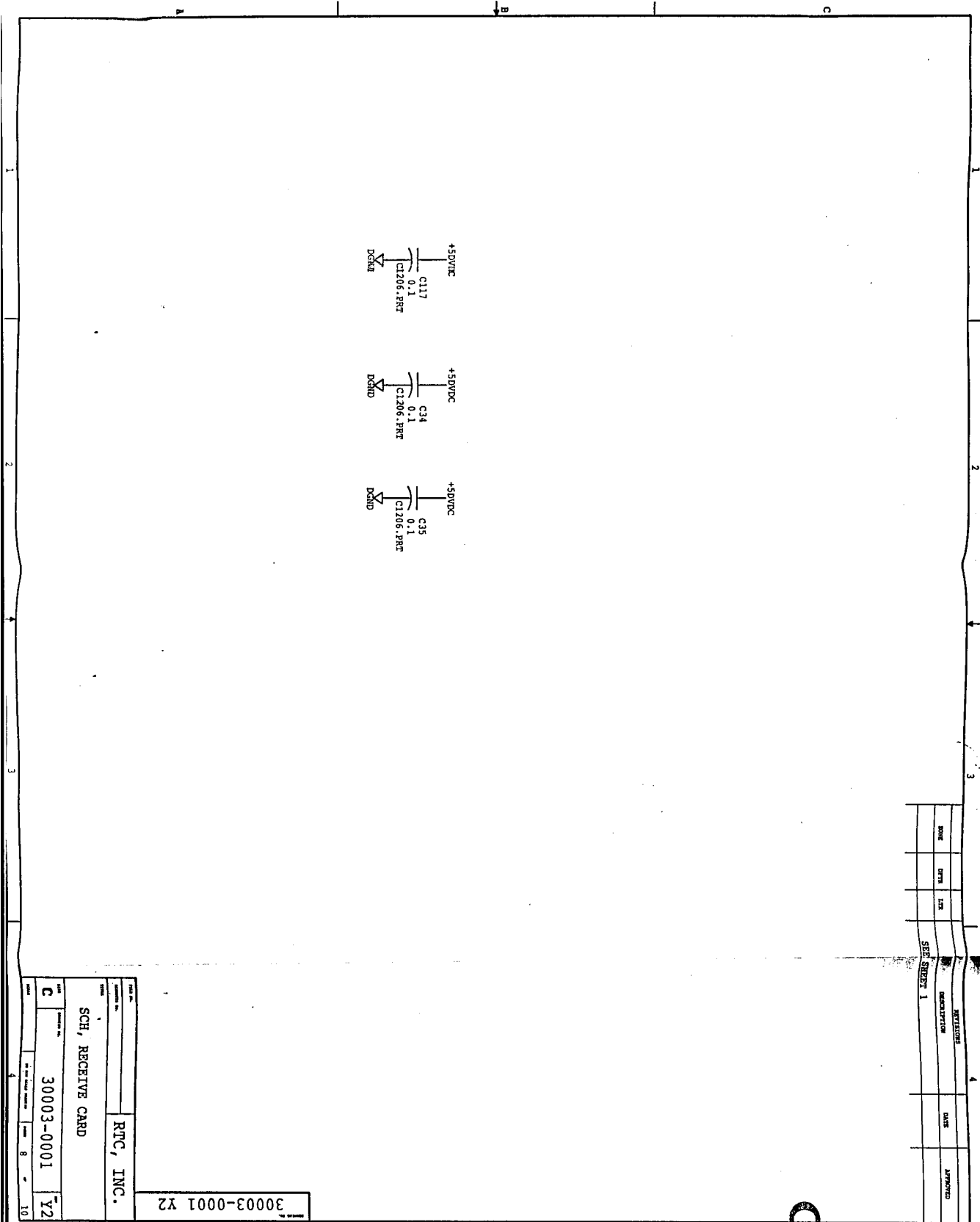
30003-0001 Y2	
SCH. RECEIVE CARD	
30003-0001	Y2



INTERFACE

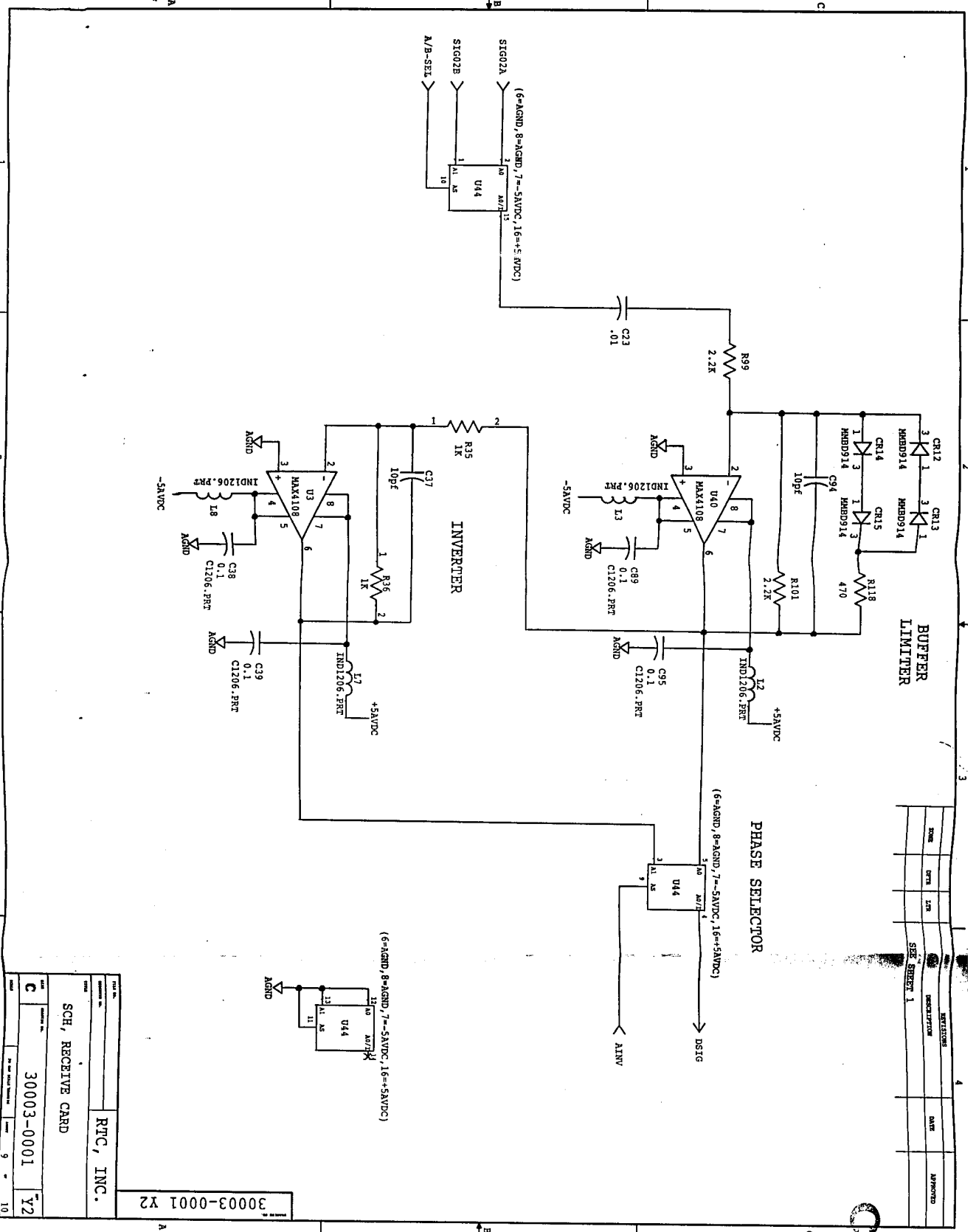


PART NO.		RTC, INC.	
QUANTITY			
DATE			
SCH, RECEIVE CARD			
PART NO.		30003-0001	
C		YZ	
QUANTITY		7	
DATE		10	



DATE	BY	REV	DESCRIPTION	DATE	APPROVED
			SEE SHEET 1		

DATE: 30003-0001 Y2	
SCH, RECEIVE CARD	
C	Y2
30003-0001	Y2
8	10



SCH, RECEIVE CARD	
30003-0001	Y2
RTC, INC.	

30003-0001 Y2

SECTION	DATE	APPROVED
SECTION 1		
SECTION 2		
SECTION 3		
SECTION 4		

LINE	DATA	LINE	DATA	LINE	DATA	LINE	DATA
1	SGND	1	Q	2	Q	2	Q
2	SGND	3	Q	3	Q	3	Q
3	SGND	4	Q	4	Q	4	Q
4	SGND	5	Q	5	Q	5	Q
5	SGND	6	Q	6	Q	6	Q
6	SGND	7	Q	7	Q	7	Q
7	SGND	8	Q	8	Q	8	Q
8	SGND	9	Q	9	Q	9	Q
9	SGND	10	Q	10	Q	10	Q
10	SGND	11	Q	11	Q	11	Q
11	SGND	12	Q	12	Q	12	Q
12	SGND	13	Q	13	Q	13	Q
13	SGND	14	Q	14	Q	14	Q
14	SGND	15	Q	15	Q	15	Q
15	SGND	16	Q	16	Q	16	Q
16	SGND	17	Q	17	Q	17	Q
17	SGND	18	Q	18	Q	18	Q
18	SGND	19	Q	19	Q	19	Q
19	SGND	20	Q	20	Q	20	Q
20	SGND	21	Q	21	Q	21	Q
21	SGND	22	Q	22	Q	22	Q
22	SGND	23	Q	23	Q	23	Q
23	SGND	24	Q	24	Q	24	Q
24	SGND	25	Q	25	Q	25	Q
25	SGND	26	Q	26	Q	26	Q
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40	SGND	41	Q	41	Q	41	Q
41	SGND	42	Q	42	Q	42	Q
42	SGND	43	Q	43	Q	43	Q
43	SGND	44	Q	44	Q	44	Q
44	SGND	45	Q	45	Q	45	Q
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46	SGND	47	Q	47	Q	47	Q
47	SGND	48	Q	48	Q	48	Q
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49	SGND	50	Q	50	Q	50	Q
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51	SGND	52	Q	52	Q	52	Q
52	SGND	53	Q	53	Q	53	Q
53	SGND	54	Q	54	Q	54	Q
54	SGND	55	Q	55	Q	55	Q
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95	SGND	96	Q	96	Q	96	Q
96	SGND	97	Q	97	Q	97	Q
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30003-0001 Y2

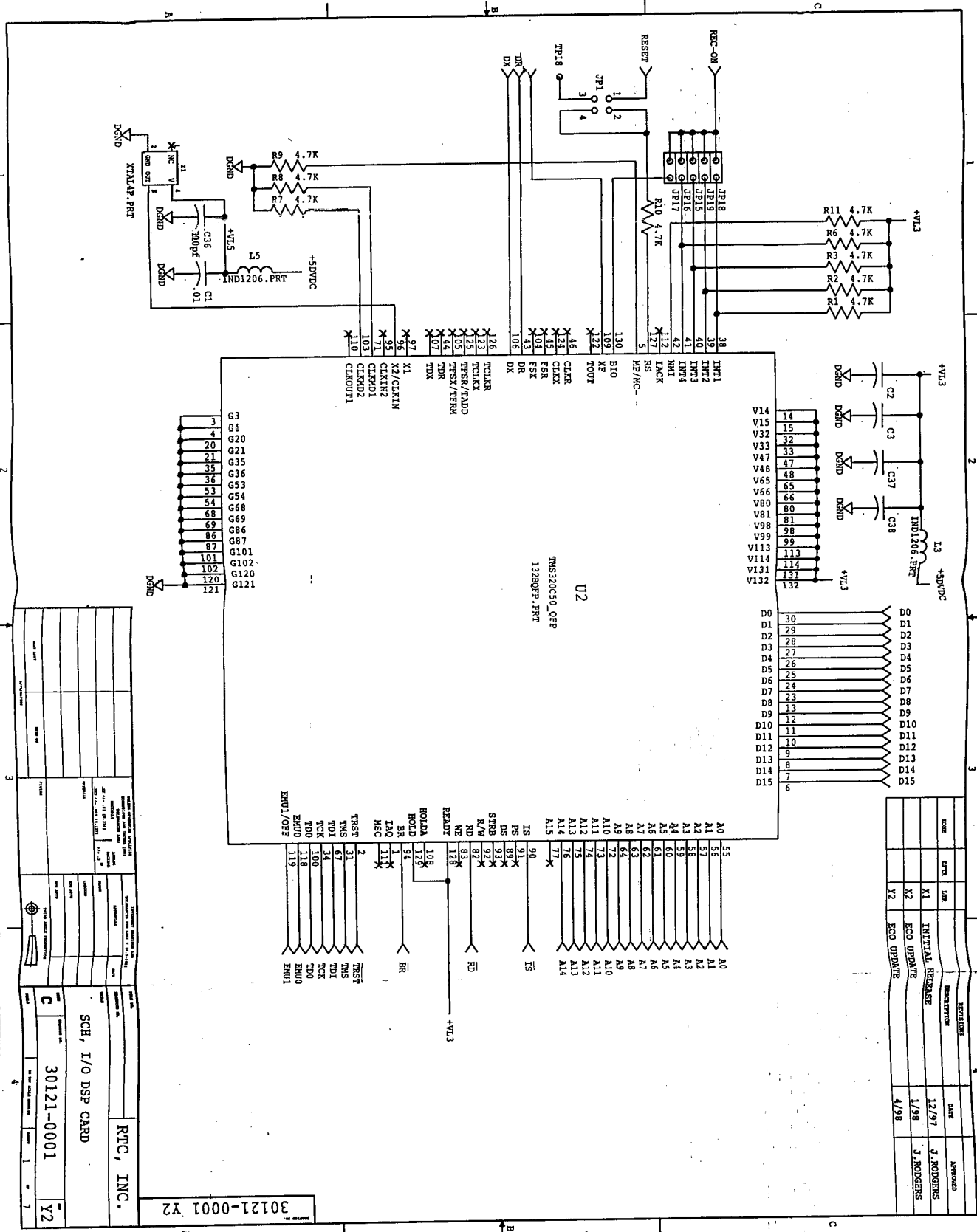
SCH, RECEIVE CARD

30003-0001

Y2

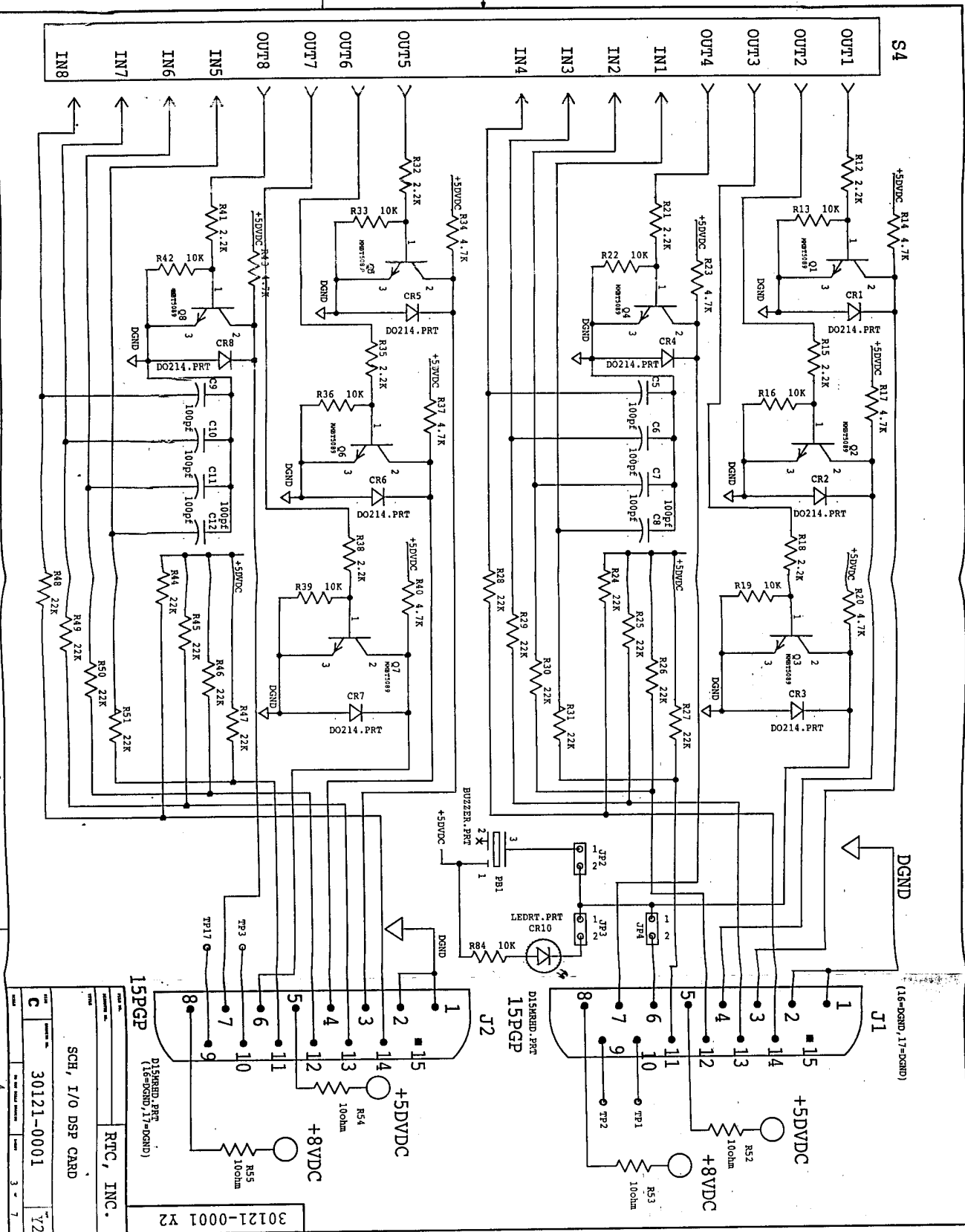
RTC, INC.

DATE	INITIALS	REVISION	DATE	APPROVED
12/97	J. RODRIGUEZ	INITIAL RELEASE	1/98	J. RODRIGUEZ
4/98		ECO UPDATE		

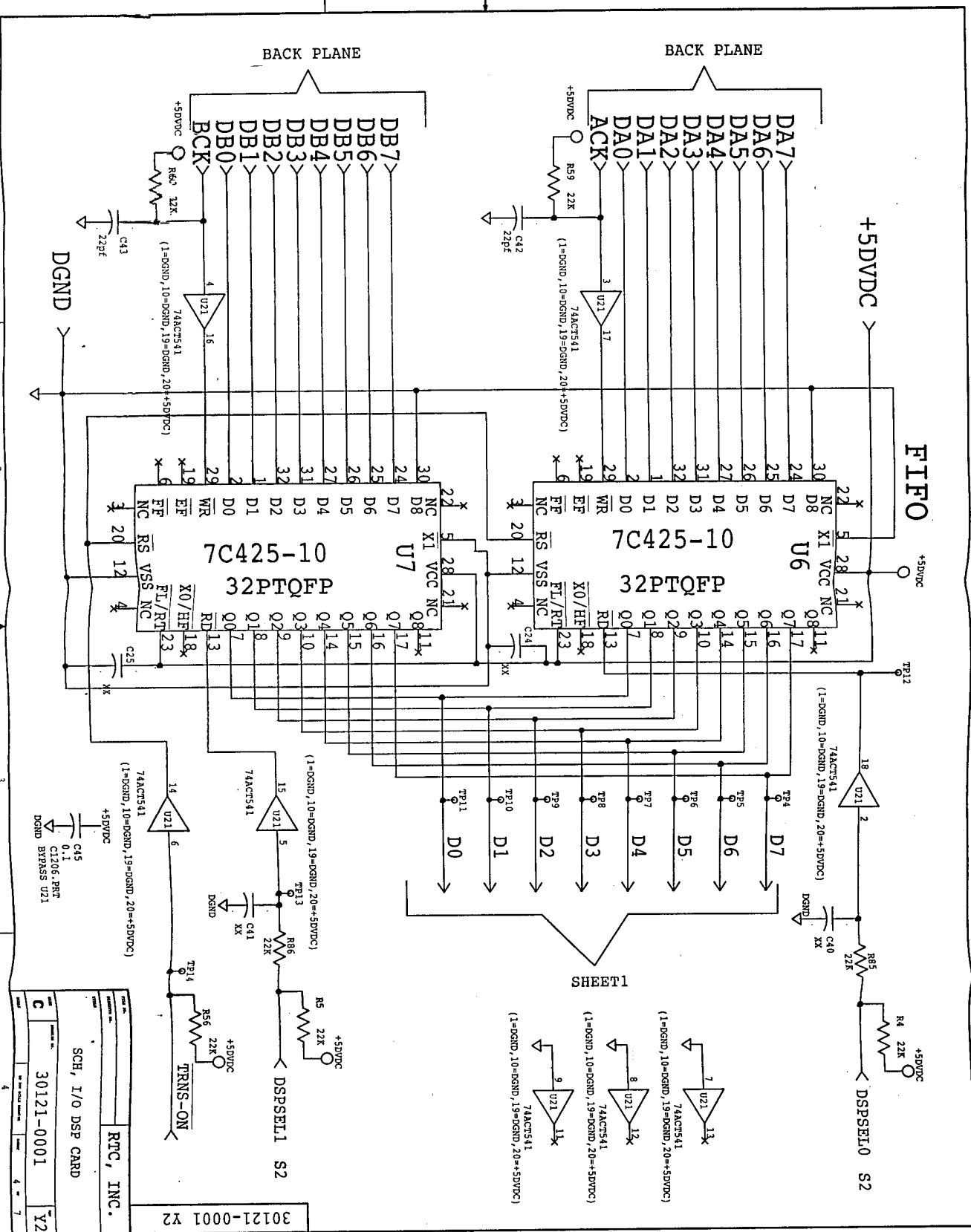


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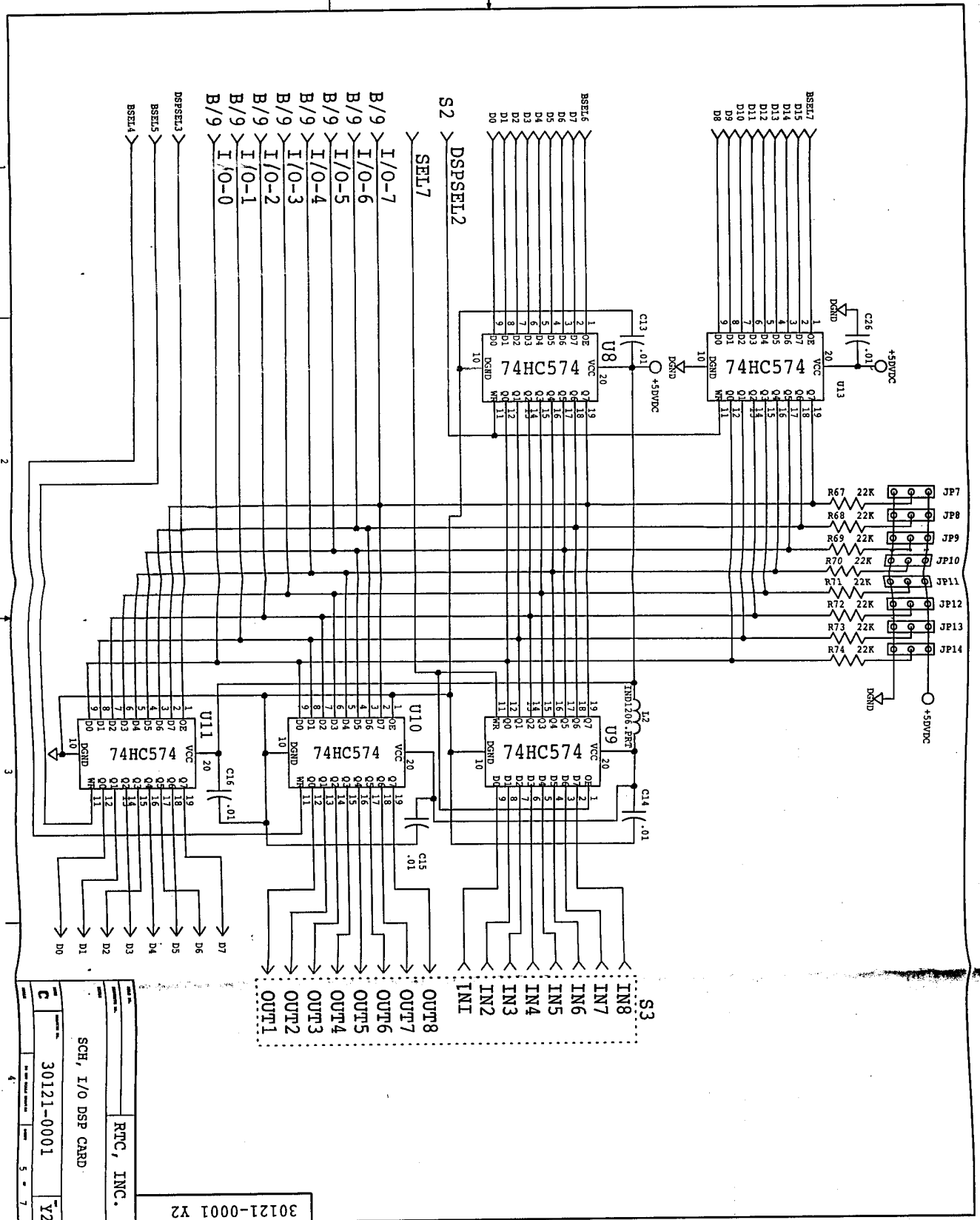
COPY



SCH, I/O DSP CARD		RTC, INC.	
30121-0001		Y2	

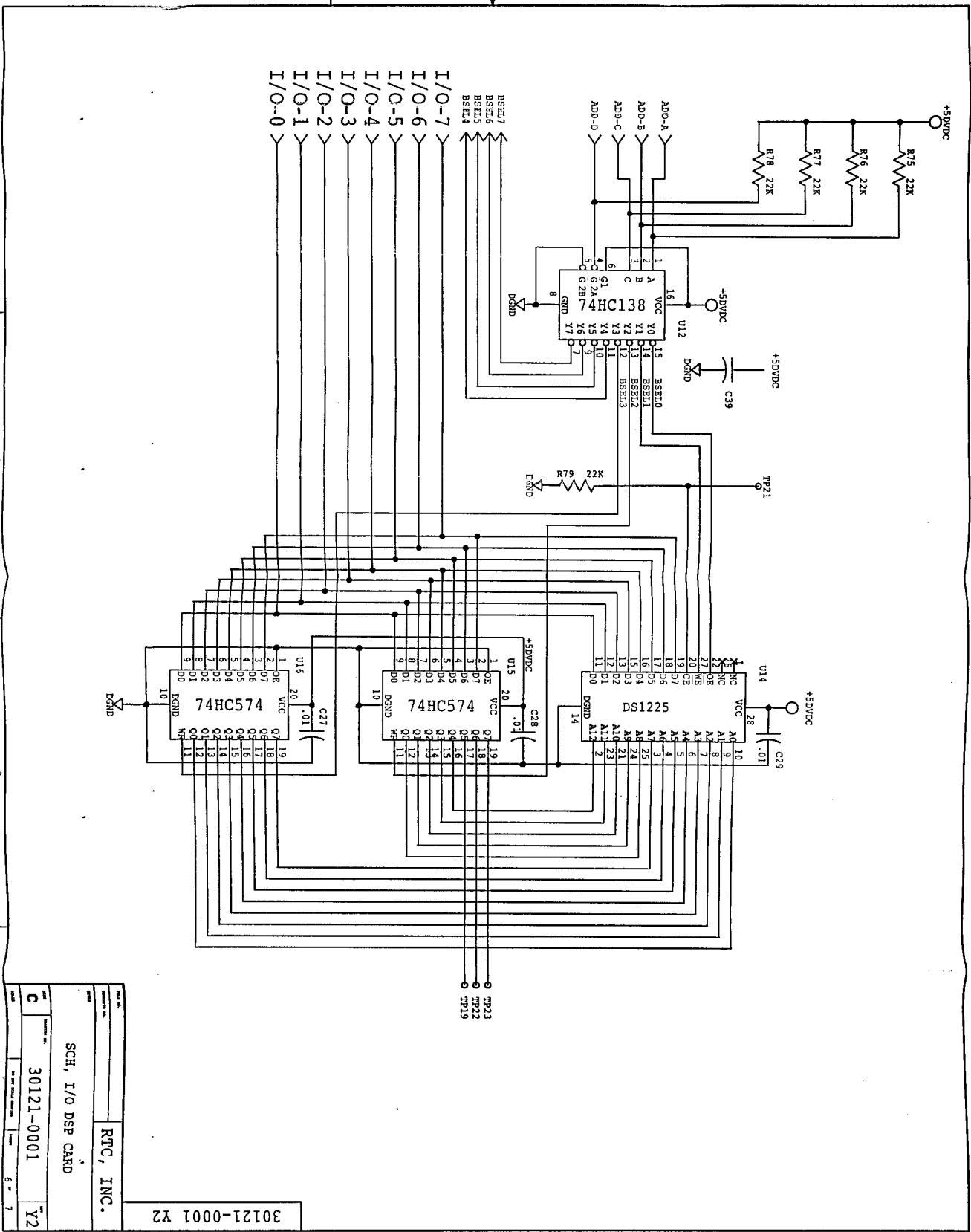
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EFFECTIVE APR 10



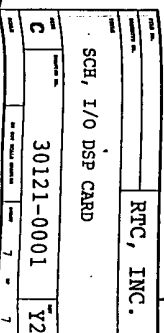
COPY

RECEIVED APR 16



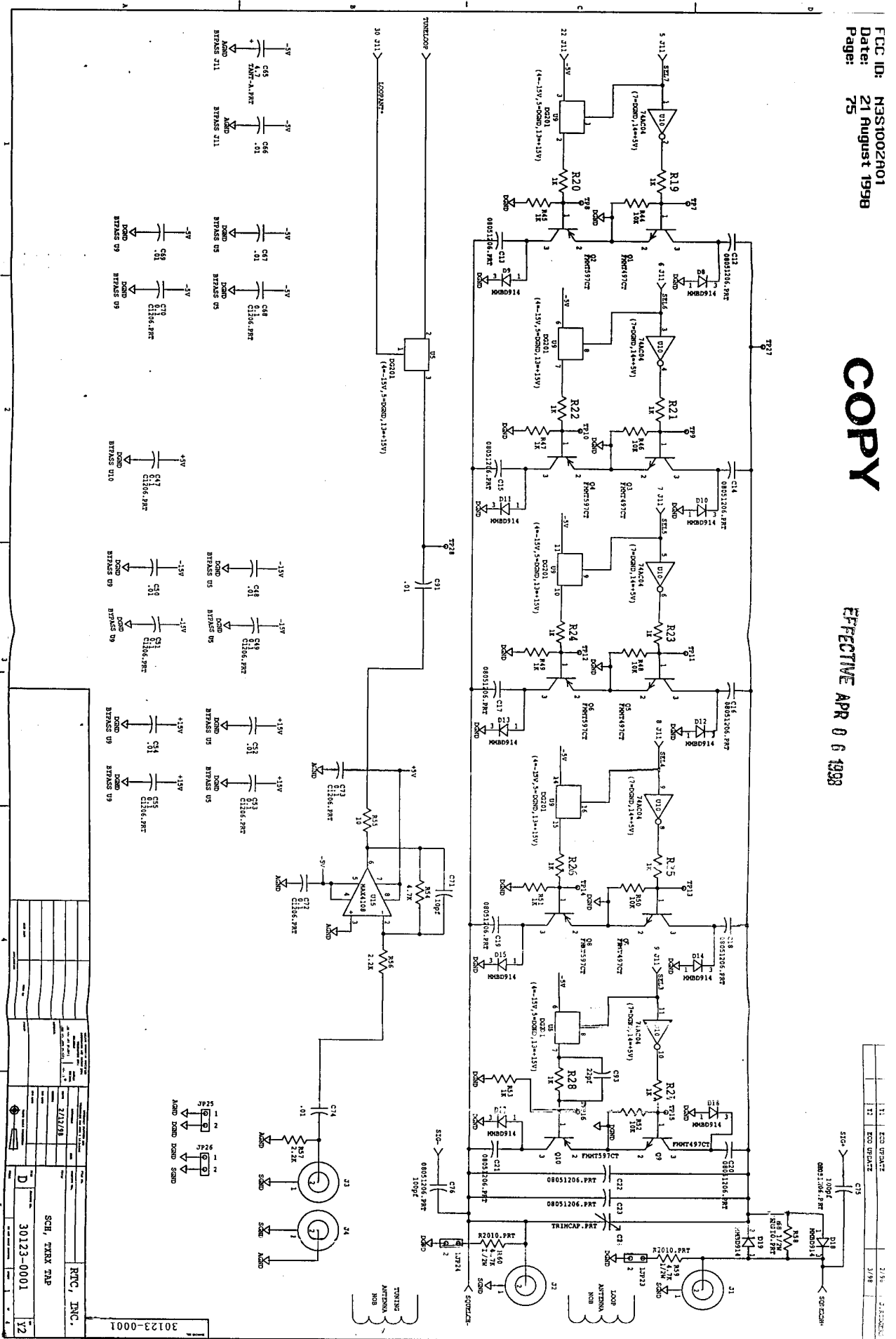
30121-0001 Y2	
RTC, INC.	
SCH, I/O DSP CARD	
C	30121-0001
Y2	

Z4A		Z4B	
1	2	1	2
1	DEND	1	DEND (1BOND)
3	+1BVC	3	DEND
5	-1BVC	5	DEND (1BOND)
7	+8BVC	7	DEND
9	-8BVC	9	DEND
11	+DVC11 (+9BVC)	11	DEND
13		13	DEND
15	+15VVC	15	DEND
17	-15VVC	17	DEND
19	DND	19	DND
21	DND	21	DND
23	DND	23	DND
25	DND	25	DND
27	DND	27	DND
29	DND	29	DND
31	DND	31	DND
33	DND	33	DND
35	DND	35	DND
37	DND	37	DND
39	DND	39	DND
41	DND	41	DND
43	DND	43	DND
45	DND	45	DND
47	DND	47	DND
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79	DND	79	DND
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89	DND	89	DND
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97	DND	97	DND
99	DND	99	DND



COPY

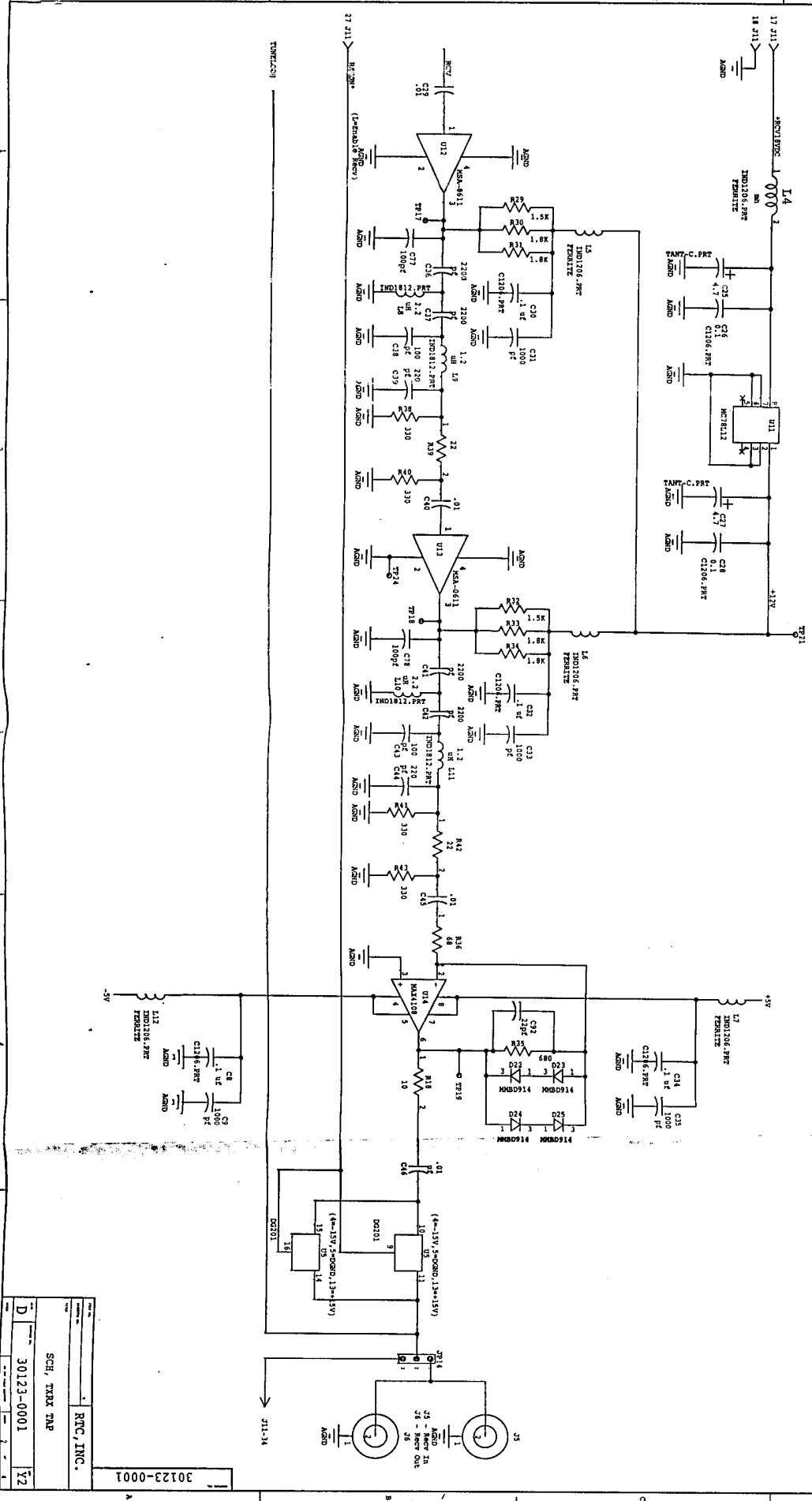
EFFECTIVE APR 6 1998



COPY

EFFECTIVE APR 0 0 1998

FCC ID: N351002601
Date: 21 August 1998
Page: 76



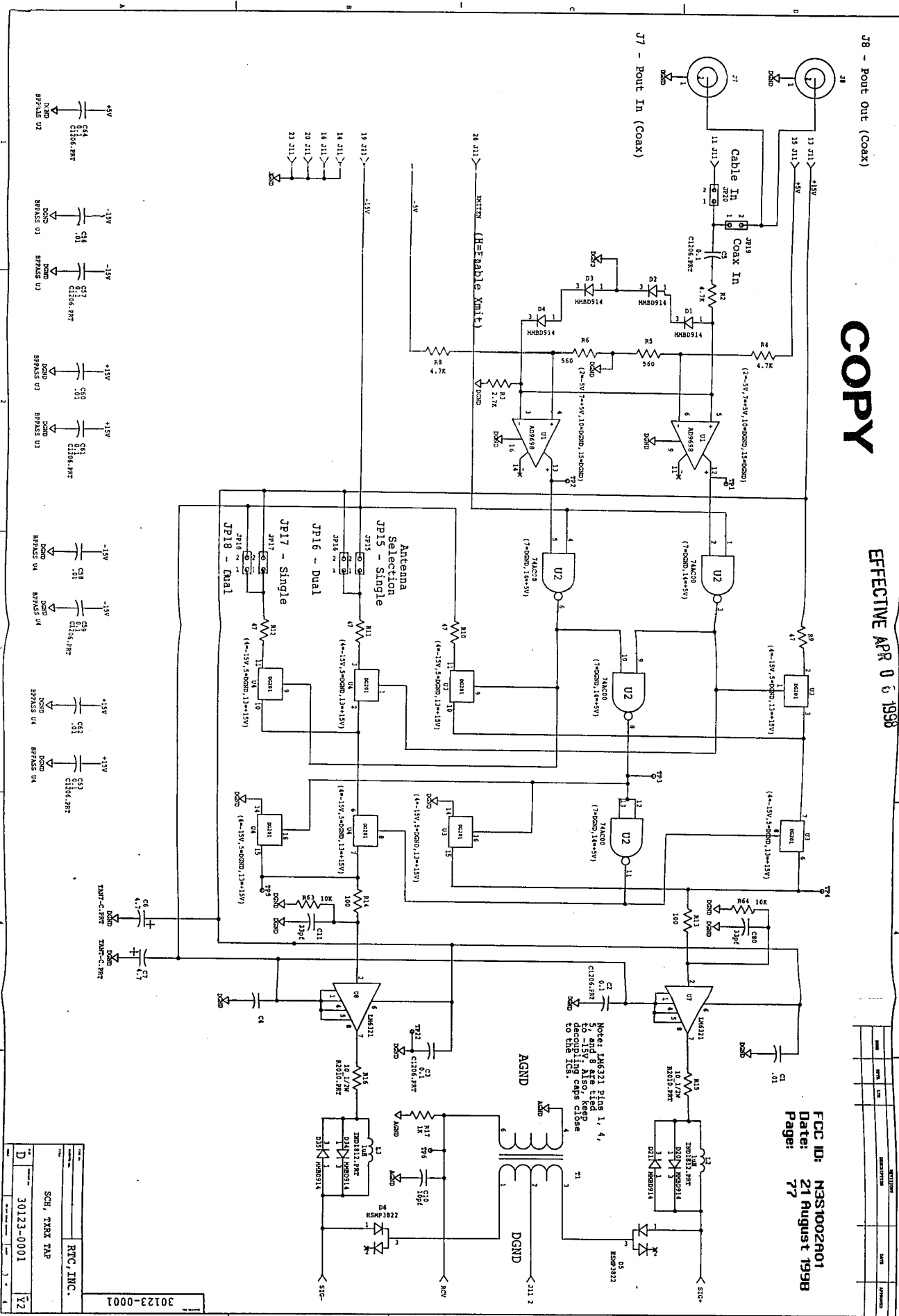
SCH. TXRX TAP	
D	30123-0001
Y2	

30123-0001

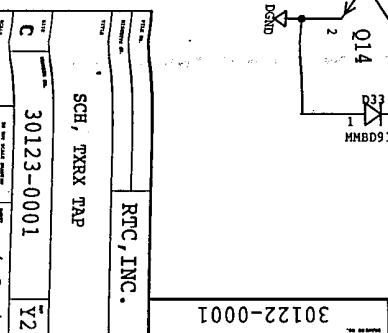
RTC, INC.

EFFECTIVE APR 6 1998

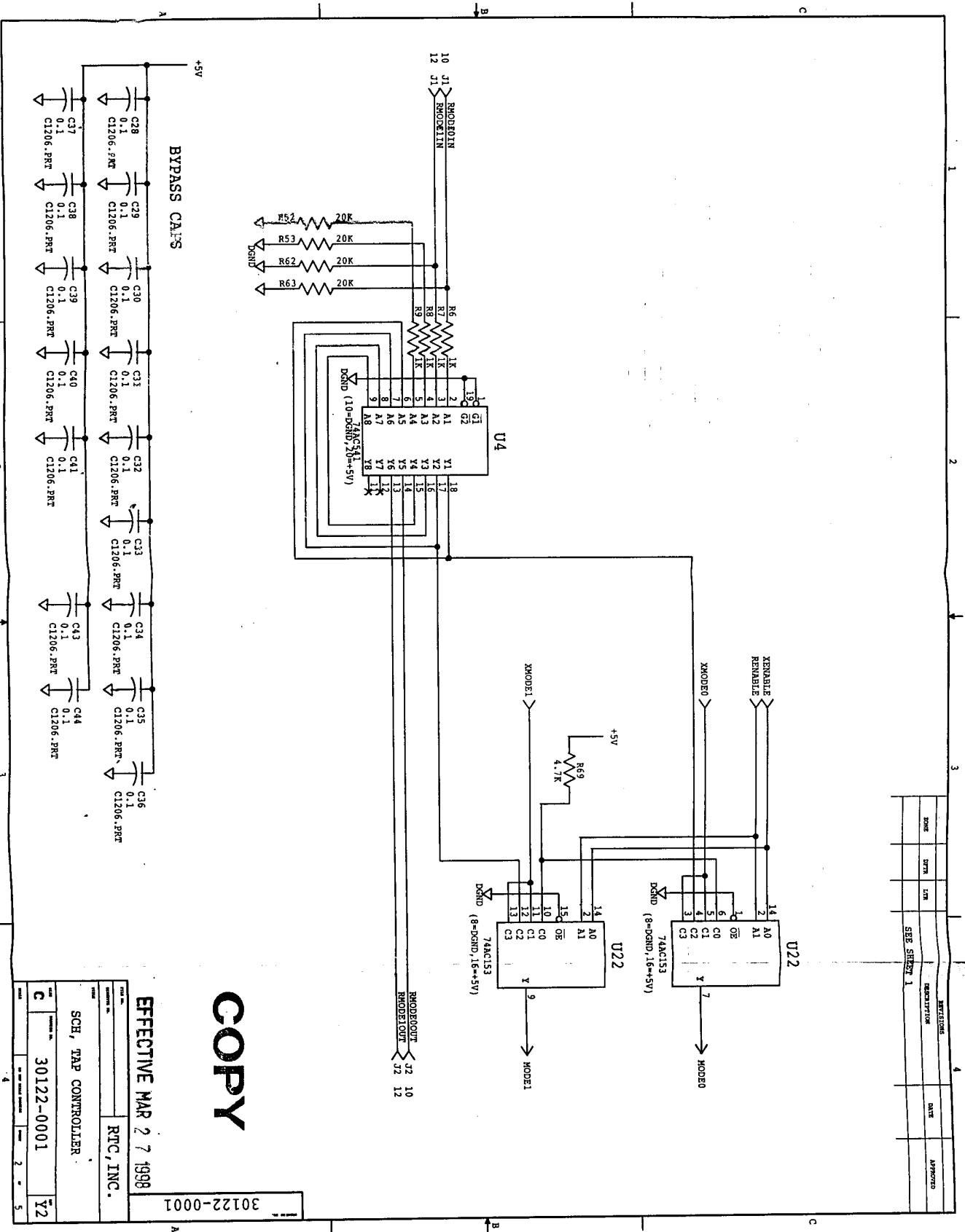
RTG, INC.	
SCH, TXRX TAP	
D	30123-0001
Y2	



COPY



DATE	APPROVED
30122-0001	Y2



COPY

EFFECTIVE MAR 27 1998

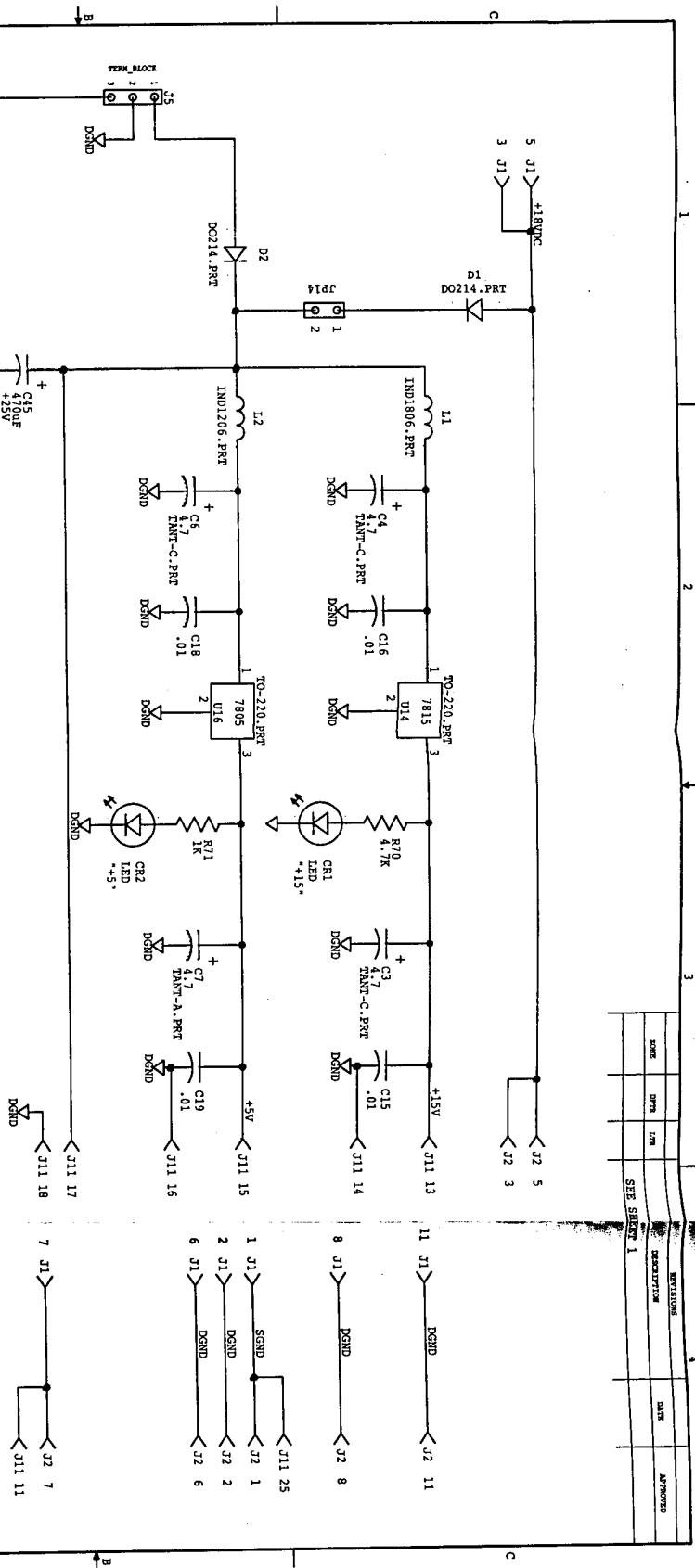
RTC, INC.

SCH, TAP CONTROLLER

30122-0001

DATE	APPROVED
30122-0001	Y2

REV	DESCRIPTION	DATE	APPROVED
1	SEE SHEET 1		

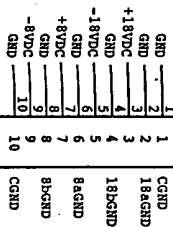


EFFECTIVE MAR 27 1998

SCH, TAP CONTROLLER

30122-0001





30007

TAP
SCH, POWER SUPPLY

RTC, INC.

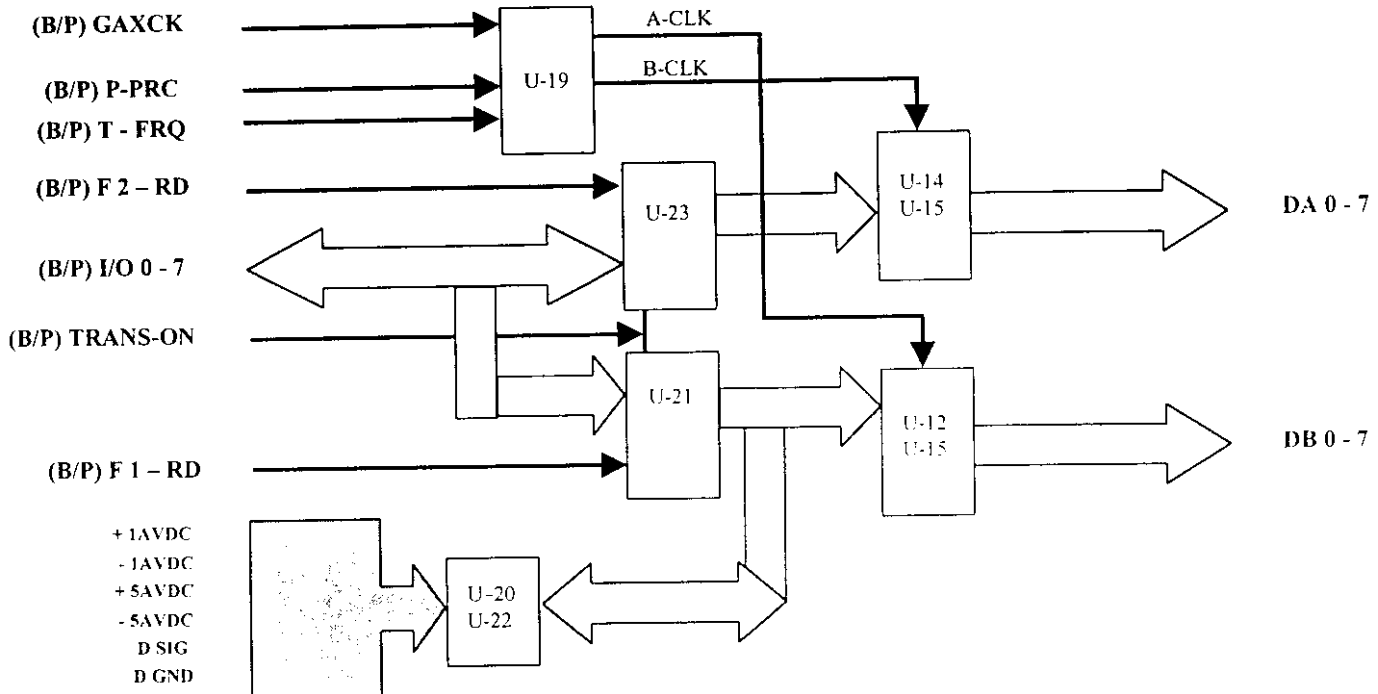
UMS RECEIVER CARD

FCC ID: N3S1002A01
Date: 21 August 1998
Page: 53

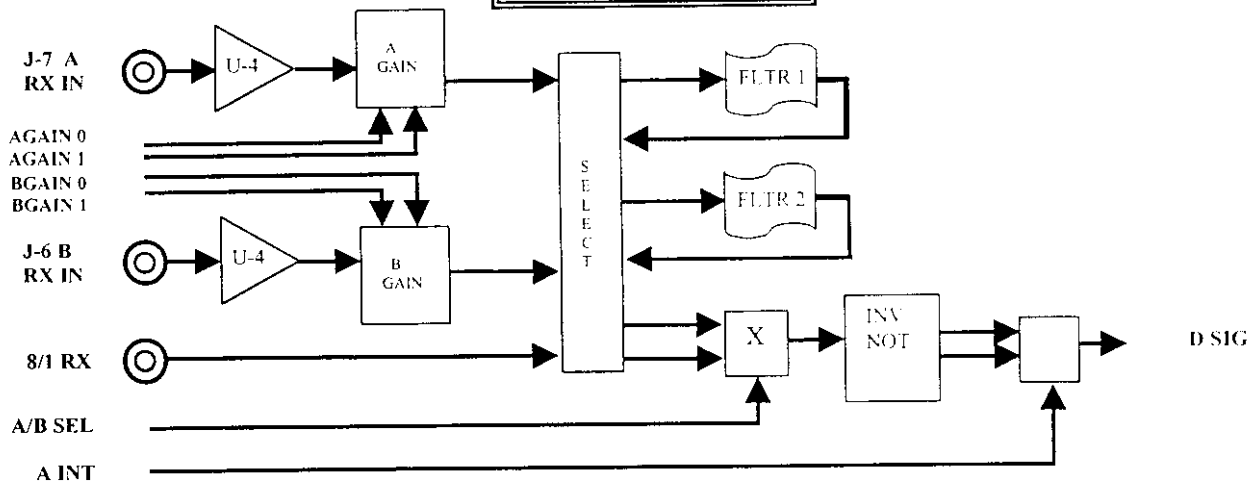
PWR. SUPPLY



FLASH CONVERTER



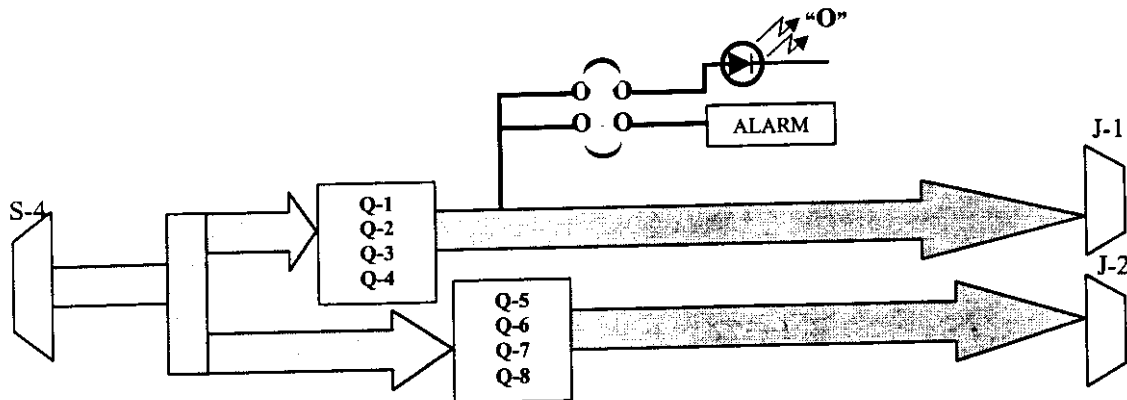
RX INPUT PATH



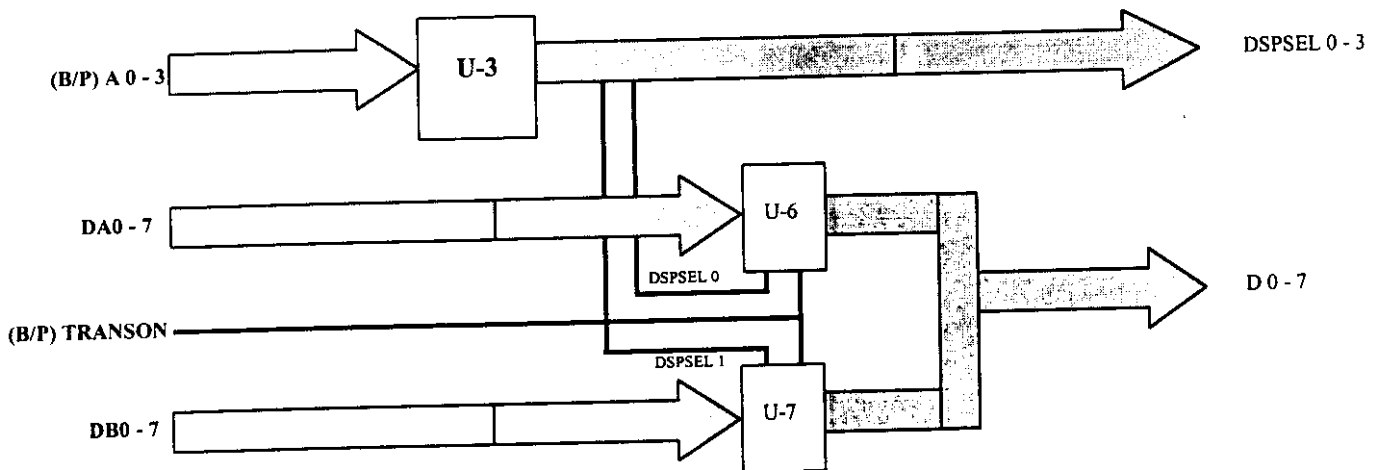
UMS DSP I/O CARD

FCC ID: H3S1002A01
Date: 21 August 1998
Page: 64

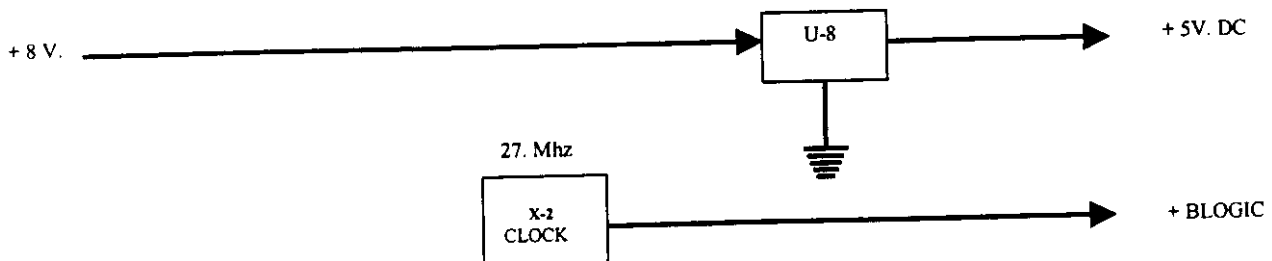
OUTPUT DRIVERS



FIFO LOGIC



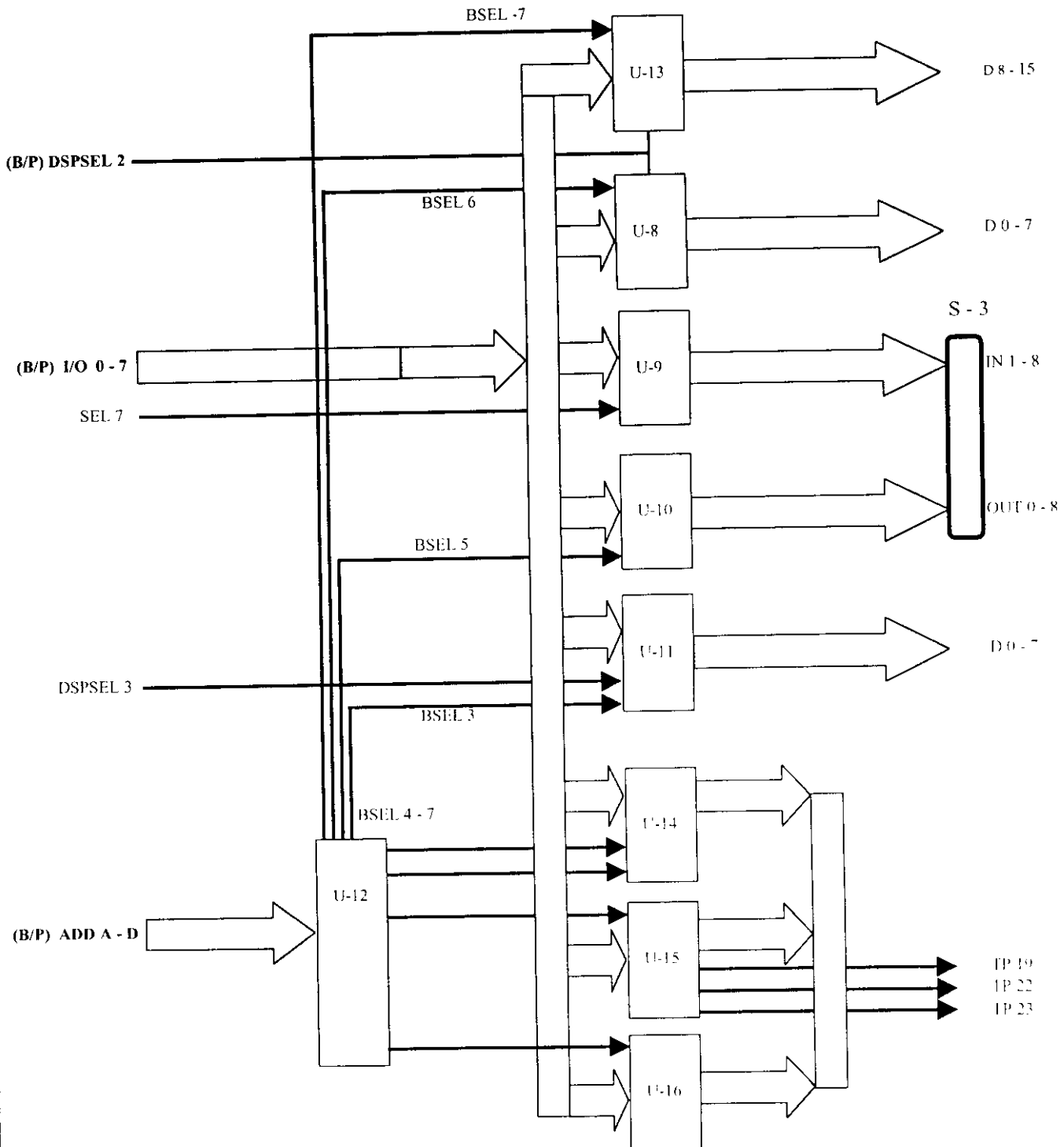
POWER and CLOCK



UMS DSP I/O CARD

FCC ID: N3S1002A01
Date: 21 August 1998
Page: 65

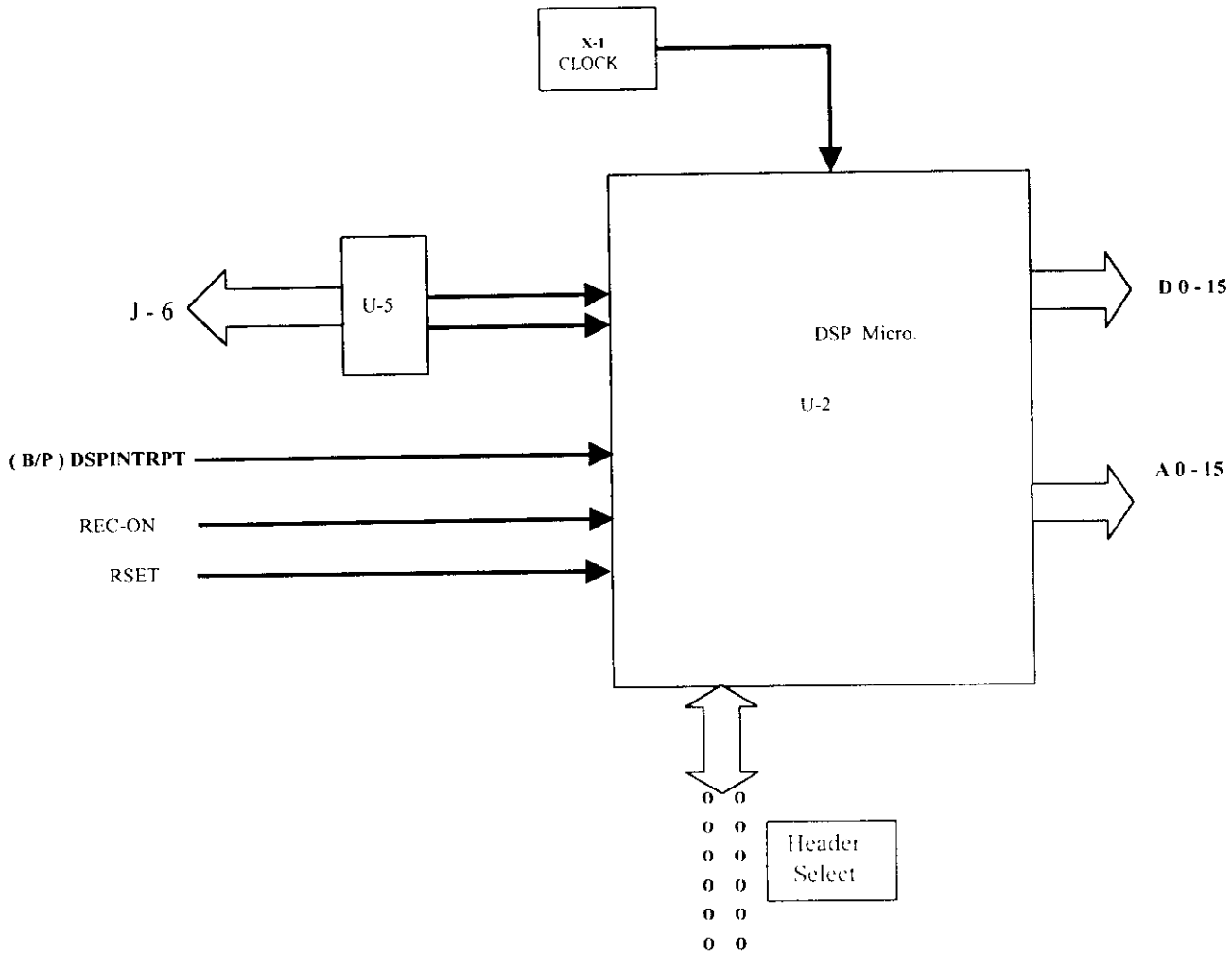
PATH DECODER



UMS DSP I/O CARD

DSP Microprocessor

FCC ID: N3S1002A01
Date: 21 August 1998
Page: 66



MIN DIN PORT

