THEORY OF OPERATION

3.1 POWER SUPPLY

The Power Supply is a switching regulator type and is capable of converting either a 14 or 28 VDC battery bus to the internal voltages (+5 and -27 VDC) required by the logic circuitry. Control and regulation of the Power Supply is established through connections to A3U1 which provides a voltage reference, a voltage comparator, and output circuit.

When the +5 VDC line is below the voltage reference at A3U1 pin 5, the current is provided to A3Q2 through A3Q3 from A3U1 pin 11, holding A3Q2 in the saturated ON condition. When A3C4, A3C5, and A3C17 (in C-722A/C-962A only) charge above the reference voltage level, current from A3U1 pin 11, is switched off, turning A3Q2 off. Current in A3T1, due to energy storage, continues to flow now finding its path through clamp diode A3CR8. The cycle is repeated when the output voltage falls below the reference voltage. Hysteresis on the switching points is provided by current through A3R14. Fuse A3F1 protects the switching circuit from shorts on the output bus. Diode A3CR9 serves as a crowbar to blow A3F1 and protect the logic and memory circuits from over-voltage.

The square wave voltage in the secondary of A3T1, due to the oscillation in the primary circuit, is rectified and zener regulated to provide the -27 VDC required for the memory integrated circuits.

3.2 FREQUENCY DISPLAY BRILLIANCE CONTROL

The light output from the frequency display is one of two levels, as determined by the voltage level on the instrument dimmer bus. For daytime operation, the dimmer bus is off (i.e. low voltage) and A3Q5 is saturated ON by virtue of U2B pin 7, being saturated high driving U2A pin 1 to be saturated low. When the dimmer bus is at a high voltage level, comparator output A3U2A goes low and the collector of A3Q5 becomes a regulated voltage source controlled by the voltage reference on A3U2A pin 3. This voltage source subtracts from the LED loop voltage and reduces element current, therefore, light output drops to a level appropriate to night lighting.

The C-722A and C-962A Control Units have an additional feature that allows their frequency display to normally be OFF unless manually reviewing or programming selected channels. Transistor A3Q6 is a switch that shuts off display return A3Q5 whenever the (DISPLAY ON)' line is open. This line is grounded when the PRESET switch is placed in either the RX or the TX positions, or if A2P2 pin 23, is grounded externally.

3.3 SQUELCH AND XMTR ANNUNCIATOR BRILLIANCE CONTROL (C-722A/C-962A ONLY)

The light output from the SQUELCH and XMTR annunciators is controlled by photo-resistor A1RT1. As the intensity of the light striking the front panel and A1RT1 decreases, the resistance of A1RT1 increases. Resistors A3R33, A3R34, and A1RT1 form a voltage divider that varies the voltage applied to A3Q9 and A3Q10 dependent on the value of A1RT1. Transistors A3Q10 and A3Q7 are arranged to form a variable current source, whose current is dependent upon the voltage applied to the base of A3Q10. As A1RT1 increases in value the current supplied by A3Q7 decreases, thus dimming the MAIN SQUELCH or the XMTR annunciators. Transistors A3Q9 and A3Q8 are in the same circuit arrangement, dimming the GUARD SQUELCH annunciator.

3.4 CHANNEL MEMORY CONTROL

3.4.1 MEMORY DESCRIPTION

Storage of preset channel frequencies and CTCSS tones is accomplished in the C-722/C-722A/C-962/C-962A by the use of a semiconductor memory called an EAROM (Electronically Alterable Read Only Memory). The memory stores information regardless of the operational condition of the Control Unit. Memory storage may be intentionally altered by certain operations, as described in the Installation/Operators Manual section. Two EAROM's are used in each control unit; A5U16 to store frequency codes and A5U17 to store tone codes.

Each EAROM is organized as 32 words containing 16 bits in each word. A five bit binary address defines (locates) each word (frequency or tone code). The EAROM address identities are shown in Table 3.4.1.

The EAROM memory is controlled to the various states (or modes) by three inputs as shown below.

C1	C2	CLOCK	MODE
HI	HI	POS PULSE	READ
HI	HI	--	HOLD
LO	HI	--	ERASE
LO	LO	--	WRITE

This control is directed to only the location that is selected by the binary input address. All other memory locations are unaffected.

	A0	A1	A2	A3	A4
CHANNEL 1	HI	HI	HI	HI	X
CHANNEL 2	LO	HI	HI	HI	X
CHANNEL 3	HI	LO	HI	HI	X
CHANNEL 4	LO	LO	HI	HI	X
CHANNEL 5	HI	HI	LO	HI	X
CHANNEL 6	LO	HI	LO	HI	X
CHANNEL 7	HI	LO	LO	HI	X
CHANNEL 8	LO	LO	LO	HI	X
CHANNEL 9	HI	HI	HI	LO	X
CHANNEL 10	LO	HI	HI	LO	X
CHANNEL 11	HI	LO	HI	LO	X
CHANNEL 12	LO	LO	HI	LO	X
CHANNEL 13	HI	HI	LO	LO	X
CHANNEL 14	LO	HI	LO	LO	X
CHANNEL 15	HI	LO	LO	LO	X
GUARD #1 TRANSMIT	LO	LO	LO	LO	HI
GUARD #2 TRANSMIT	LO	LO	LO	LO	LO

"X" IS HI IN RECEIVE MODE AND LO IN TRANSMIT MODE

LO AND HI REFER TO 0 VDC AND +5 VDC CMOS LOGIC LEVELS RESPECTIVELY

EAROM ADDRESSING CODE
TABLE 3.4.1

3.4 CHANNEL MEMORY CONTROL (cont.)

3.4.2 MEMORY CONTROL LOGIC - READ/HOLD MODES

The normal mode of operation for channel memory A5U16 and A5U17 is the READ/HOLD mode. This mode is established by the high condition set on the Q output of READ/WRITE flip-flop A4U13A. Each positive pulse out of the READ oscillator A4U19D and A4U19E starts a READ cycle by clocking gate flip-flop A4U13B out of the set condition.

This gate enables A4U5, a 14 bit binary counter, and its associated oscillator. After eight oscillator cycles, A4U5 pin 7 goes high. During the last half of the eighth oscillator cycle, gate A4U13B is enabled and a clock pulse is released cuasing a READ cycle in the memory chip. At the end of the clock pulse, flip-flop A4U6B is clocked to disable A4U3B and inhibit any further output. After 16 oscillator cycles, A4U5 pin 5 goes high. This enables gate A4U12B and finishes a READ cycle by setting flip-flop A4U13B. Data is held at the memory outputs until the next READ cycle and clock pulse. EAROM control line C1, coming from A4U11D pin 11 is held high during READ and HOLD modes because A4U13A is in the READ/HOLD mode. Likewise control line C2 is held high by A4U13A through gate A4U14A.

3.4.3 MEMORY CONTROL - LOGIC - ERASE/WRITE CYCLE

A positive pulse from A4U10C will clock A4U13A into the ERASE/WRITE mode condition and clock A4U13B out of the set condition. This action sets control line C1, the output of A4U11D, to a low condition where it will remain for the duration of the ERASE/WRITE cycle; control line C2 is initially high because A4U6A is in the reset condition. Thus the memory control is set up for the ERASE condition. It will remain so for 8,192 cycles of the oscillator in A4U5. When A4U5 counter reaches this count, pin 3 will go high clocking A4U6A and letting control line C2 go low, thus beginning a WRITE interval. At the end of another 8,192 oscillator cycles, A4U5 pin 3 will go low enabling gates A4U7B and A4U9B and setting of A4U13A and A4U13B, ending an ERASE/WRITE cycle. This stored data is changed at the addressed location in memory.

3.4 CHANNEL MEMORY CONTROL (cont.)

3.4.4 MEMORY ADDRESS LOGIC CIRCUIT

The location in memory under control, or ADDRESSED at a given time, is determined by the CHANNEL SELECTOR switch, the PTT control line, the GUARD/MAIN switch, and G1/G2 switch acting through tri-state inverters A4U1 and A4U2.

The channel selector and the PTT line in the receive condition act together at the inputs of A4U1A through A4U1F to generate binary address inputs 31 to 17 (see Table 3.4.1), locating the preset channel receive frequencies and tone in the memory. Should the PTT line be switched to the TRANSMIT condition, with the GUARD/MAIN switch in the MAIN position, the input to A4U1F will become a high condition, and by operating the channel selector through the preset channel positions, binary address inputs 15 through 1 are generated, locating the preset main channel transmit frequencies in the memory.

With TX-GUARD/MAIN switch in the GUARD position, when the PTT line is grounded the output from A4U12D goes low. This low level enables A4U2 and, through A4U12B, disables A4U1. In this manner, depending upon the position of the G1/G2 switch, the guard memory address input is selected (either binary 16 or 0) to locate one or the other of the guard transmit frequencies in the memory.

3.4.5 MEMORY LOAD LOGIC

The memory can be altered (loaded) only when A4S1B or A4S1A and A4S1B are set to the load enable position. With these switches set, loading may be done on demand by first operating A2S14 to either the LOAD RX or LOAD TX position and then pushing LOAD/TEST button A2S1. The RX and TX load commands, from A2S14, are or'd together by A4U14C and then and'd together with the load pulse. The load, generated by A4C5 when A2S1 is closed, passes through A4U20A and A4U18B to the input of A4U15C. The output of A4U15C clocks load memory A4U16B. The output of A4U16B pin 13 is a command to start an ERASE/WRITE cycle; however, it is delayed in A4U10C (by A4U9C and A4U13B outputs) until any previous memory operational cycle has been completed. When the cycle in process is completed, then the output of A4U10C is free to go high, starting the next cycle; in this case an ERASE/WRITE cycle. During the loading operation, the effect of the PTT line on the control unit is disabled by A4U9A.

3.4 CHANNEL MEMORY CONTROL (cont.)

3.4.5 MEMORY LOAD LOGIC (cont.)

Once a LOAD TX cycle has begun, A4U13A is fed back to the LOAD TX switch input through A4U20B and A4U9C to insure that the memory address is maintained in the transmit condition during the entire ERASE/WRITE cycle, regardless of the action on the LOAD TX switch.

Logic is provided by A4S1A and A2S13 inputs to A4U4E, A4U4F, A4U17A, A4U17B, A4U17C, and A4U12D so that when it is desired to load a guard frequency, main channel frequencies may not be altered, and vice versa, for the loading of main channel frequencies.

3.4.6 PUSH-TO-TALK LINE PROCESSING LOGIC

The push-to-talk line, (PTT)', is processed first by A4U18C and A4U19F in a debounce circuit to secure a single leading edge when the PUSH-TO-TALK switch is operated. The switching action is then held up in a QUEUING circuit formed by A4U16A, A4U10A, and A4U10B. A change on the PTT line will normally cause an immediate command (positive pulse from A4U14D) for a new READ/HOLD cycle. This output will be held up if any memory operational cycle is in process at the time of a change on the PTT line by the high output from A4U13B pin 12 connected to A4U10A and A4U10B. When A4U13B pin 12 goes low, then the change being held at the inputs to A4U10A and A4U10B propagates through A4U14D and A4U20C to clock A4U13B.

A change is recognized by comparing the new condition of the PTT and (PTT)' lines with the past condition of flip-flop A4U16A on gates A4U10A and A4U10B. The Q outputs from A4U16A is the processed replica of the input PUSH-TO-TALK line and is high during transmit. This output is used at A4U1F to direct the memory address between receive and transmit halves of the memory and to direct the memory selection between A5U16 and A5U17 or the thumbwheels during transmit in the GUARD mode when channel selector A2S12 is in the manual position.

3.4 CHANNEL MEMORY CONTROL (cont.)

3.4.7 CHIP SELECT LOGIC

Memory chips A5U16 and A5U17 are disabled when the CHIP SELECT (CS) line is in a logic low condition. The memory chips are normally disabled when the CHANNEL SELECTOR switch is in the manual channel position, except when transmitting on one of the preset GUARD channels. In this case, the memories must be selected and the thumbwheels de-selected. With the channel selector set to any of the 15 preset channels the select line is high. This switching is done through A4U3A and A4U12A to A4U8A.

3.4.8 THUMBWHEEL SELECT LOGIC

The thumbwheel frequency and tone selectors are buffered through tri-state inverters A5U10, A5U11, A5U12, and A5U13. These inverters are controlled by the Gth line. A high level on this line causes their outputs to go to a high impedance condition (thumbwheels de-selected). The thumbwheels are selected in the manual mode (except when transmitting on a guard frequency) and during the WRITE mode when data is being transferred from the thumbwheels to memory A5U16 and A5U17. When THUMBWHEEL ENABLE switch A4S1C is opened, the thumbwheels and, therefore, the manual mode (M) are disabled.

3.5 LED DISPLAY, DISPLAY DRIVERS, AND INTERFACE

Seven segment displays A5DS1 through A5DS7 are driven by BCD to seven segment converters A5U1 through A5U6 from the frequency and tone selection data bus lines. Binary adder A5U15 is interposed between the tone data lines to add 1 (one) to the tone BCD code causing the display to show the proper designation numbers (1 through 8, rather than BCD values 0 through 7) actually used to control the remote transceiver.

The frequency and tone bus lines are interfaced to the remote transceiver through open collector logic inverters A5U7, A5U8, A5U9, and A5U14.

The functions of the added tone control switch (A2S15) in the C-722A and C-962A are provided for by portions of A5U9, A5U14, and A5U18. Tone display blanking in the MANUAL TONE mode is provided by A5U14F, A5U18B, A5U18A, and A5U14D. Receiver tone de-activation when in the TONE OFF mode is provided for by A5U18C, A5U18D, A5U9D, and A5U9F.

3.6 THUMBWHEEL BACKLIGHTING

The FREQUENCY and TONE selectors are normally lit whenever the control unit is operating. Power to these lamps are supplied by the internally generated + 5 VDC supply. In the C-722A and C-962A only, these lamps may be shut off. In the C-722A/C-962A the return line for these lamps are routed through A2Q1. Transistor A2Q1 is normally biased on via A2R2. By grounding pin 24 of A2P2, A2Q1 is biased off and the return for the thumbwheel lamps is open.