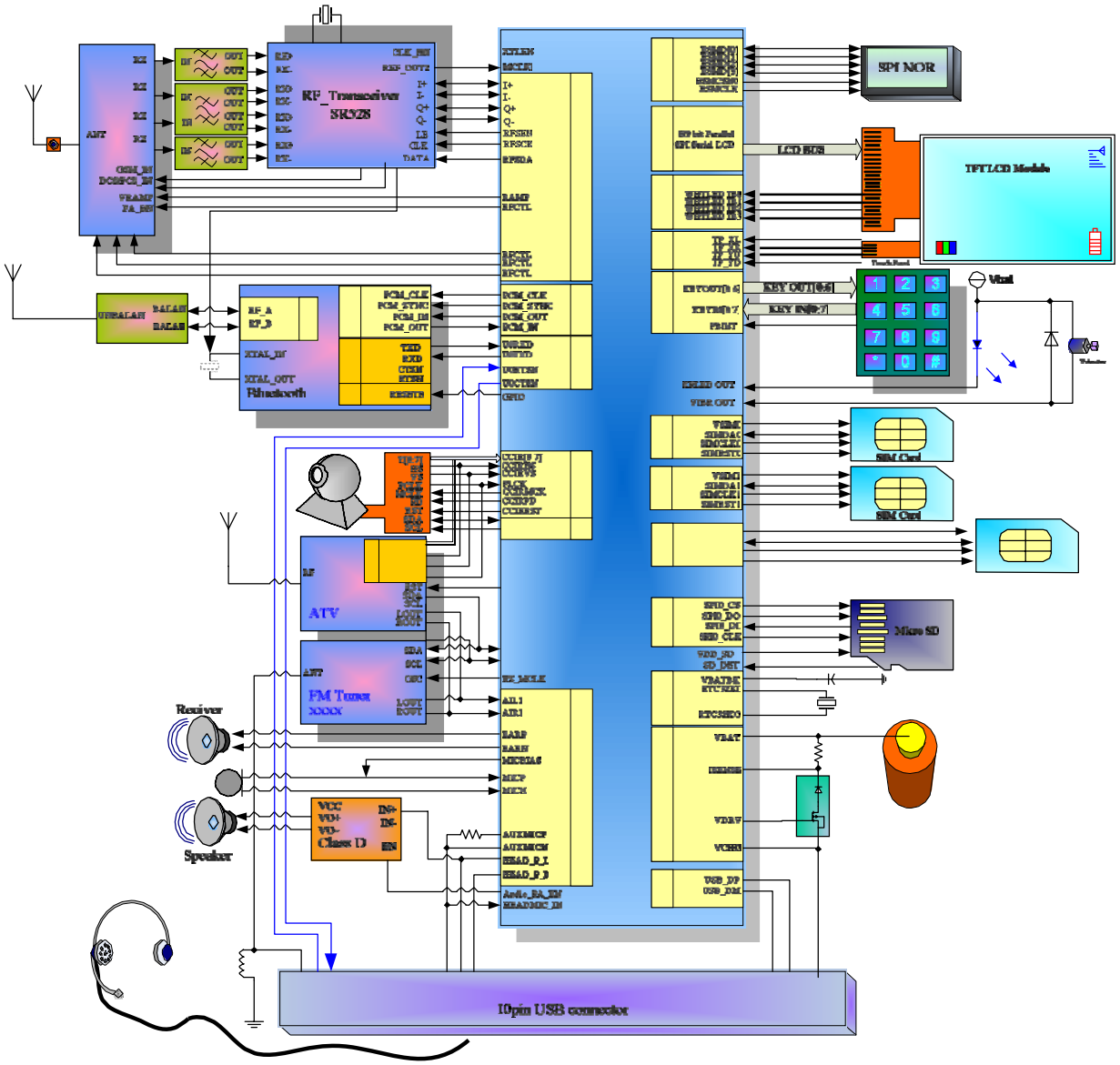
1. Electronic schematic description

1.1 General block introduction



Scheme 3-1 A typical Application Diagram of SC6620

1.2 Baseband main blocks

1.2.1 Baseband chipset

SC6620 is a highly integrated mixed signal baseband processor for GSM/GPRS applications, Which is designed to provide a cost-effective, low-power and

high-performance solution for mobile phones. It consists of an embedded 32-bit microcontroller and an embedded 16-bit DSP core and integrates many GSM/GPRS-specific hardware accelerators and analog functions, such as power management unit, analog baseband, audio DAC and ADC, and many drivers, even some resistors to simplify the system design and minimize the total number of system components. Further more, embedded PSRAM is supported in SC6620 for the purpose of decreasing the system complexity.

The embedded MCU runs a real-time operation system (RTOS), performs the system control functions according to the GSM/GPRS protocol stack, and serves all peripheral components including man-machine interface.

The embedded DSP provides data processing for many GSM/GPRS-specific physical layer signal.

To reduce the total system cost and enhance overall functionality, SC6620 integrated digital still camera processor, MPEG4/H.263/JPEG codec engines and a rich set of peripherals for functionality extensions, such as SPI, IrDA, UART, IIS, PCM, I2C, keypad, SIM card, 4-port external memory interface, LCM and USB. To enhance system performance, a cache controller is added with 8k bytes ram space.

The embedded PSRAM simplifys the design complexity of PCB and reduce the system cost.

Proprietary architectures and algorithms are developed for low power ASIC design and advanced power management for SC6620. Unique techniques are utilized for noise/offset calibration and cancellation at the same time. Therefore, SC6620 is particularly suitable for cost-sensitive and power-sensitive applications.

SC6620 Platform features：

(1) GENERAL Features

- Low power and high-performance device of mixed signal CMOS technology
- External supply voltages: battery 3.6 V (typical), optional backup battery 3.0 V (typical)
- Internal supply voltages: analog 3.0 V or 3.3 V, digital I/O 3.0 V or 1.8 V (typical), digital core 1.8 V (typical) and RTC power supply 1.8 V (typical)
- Integrated power management; voice band, audio band, and base band analog front ends; keypad LED driver, vibrator motor driver, and LCD backlight driver; aux ADC and some resistors
- Embedded PSRAM, ADMUX, 32 M is supported
- Serial flash controller is integrated to support external serial flash memory
- LFBGA , 9mm x 9 mm, 200-ball, 0.5 ball pitch package

(2) MCU

- ARM7TDMI-S , 32-bit RISC processor
- High performance ARM AMBA bus
- Dedicated DMA bus
- High performance CACHE controller
- 22 DMA channels
- 16 KByte on-chip RAM
- 52 KByte on-chip ROM
- Watch dog timer for system crash recovery
- Three sets of general purpose timer
- System timer
- RTC timer
- LCM controller
- Serial flash controller
- Support MCU bus monitor for software debug and ROM code patch
- JTAG port for test and In-Circuit Emulation

(3) Embedded PSRAM Memory

- Supports embedded PSRAM memory with size of 32M bits
- Supports ADM PSRAM of 16-bit data width
- Asynchronous single access
- Synchronous burst access

(4) External serial flash memory

- External serial flash memory supported
- Standard SPI mode, SCLK/SDI/SDO
- Dual SPI mode, SCLK/IO0/IO1
- Quad SPI mode, SCLK/IO0/IO1/IO2/IO3
- QPI mode supported
- up to 78M bus clock frequency supported

(5) Peripherals

- Thriple SIM card interface, support 1.8 V or 3.0 V SIM cards
- 7-row x 8-column keypad controller, support multiple key presses
- Real Time Clock (RTC) and alarm operating at 32.768 kHz with a separate power supply
- General purpose I/Os (GPIO)
- Pulse Width Modulation (PWM) output
- Full-speed USB 1.1 Device controller
- Two sets of UART up to 900K baud rate
- Support IrDA
- Two sets of SPI, support both two-wire and three-wire serial interfaces
- I2S/PCM and DAI interface for audio application
- I2C, for, e.g., camera configuration
- SBI for RF control
- T-card supported with SPI mode

SC6620 Multimedia features：

- Compatible with GSM/GPRS Release 1999, DCS1800 and PCS1900 recommendations
- Dedicated GSM/GPRS signal processing engine for equalization, channel encoding/decoding for all traffic and control channels, GMSK modulation and encryption/decryption (A5/1 and A5/2, GEA 1 and GEA 2 algorithms)
- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A converter for uplink baseband I and Q signals
- 12-bit high resolution A/D converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D converters and D/A converters
- 10-bit D/A converter for Automatic Power Control
- Programmable radio Rx filter
- GSM system timing
  - Low swing 26 MHz master clock input
  - Programmable TDMA timing with 1/4 bit resolution
  - Timing tracking in power saving mode
- Complete in-phase and quadrature (I/Q) component interface between the Digital Signal Processor (DSP) and RF module
- Dedicated RF serial control interface and parallel control signals
- Programmable GSM/GPRS modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- Multi-band support
- Complete voice band codec
  - Audio signal conversion between microphone/earphone and DSP
  - Second set converters for auxiliary microphone/speaker
  - Supports Digital Audio Interface (DAI)
  - Stereo audio output
  - Integrated microphone bias
  - GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - FR error concealment
  - Dial tone generation
  - Voice memo
  - Noise reduction
  - Echo suppression/echo cancellation
  - Advanced side tone oscillation reduction
  - Digital side tone generator with programmable gain
  - Voice power amplifier with programmable gain
  - 2nd order sigma-delta A/D converter for voice uplink path
  - D/A converter for voice downlink path
  - Supports half-duplex hands-free operation
  - Compliant with GSM 03.50
- Five auxiliary analog inputs to a 10-bit analog-to-digital converter (ADC) for measurement purposes

SC6620 Multimedia features：

(1).LCD interface:

- Supports simultaneous connection to up to 2 parallel LCD modules
- Supported formats: RGB332, RGB444, RGB565
- Supports LCD panel maximum resolution up to QCIF at 16 bpp
- Supports hardware accelerated and anti-shaking touch panels

(2).Camra interface:

- Supports CCIR656, CCIR601 and SPI mode interfaces
- Supports up to 2M YUV format sensors

(3).Audio CODEC:

- Wavetable synthesis with up to 64 tones
- Two differential microphone input with a 0~20 dB boost gain stage
- A programmable gain amplifier in front of ADC
- An analog stereo mixer with programmable gains to mix signals coming from DAC and the stereo line inputs (analog bypass path)
- A stereo programmable gain amplifier for headphone outputs
- Programmable sampling frequencies (Fs) for ADC and DAC: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz
- 16-bit linear PCM voice data, programmable DAC/ADC, data buffer sizes from 1 to 160, support DMA
- Both ARM and DSP can control the audio codec

(4).Image CODEC:

- JPEG decoder compliant with JPEG baseline profile, support YUV444, YUV422, YUV420 , YUV411 and Gray formats
- JPEG encoder compliant with JPEG baseline profile, support YUV422 format only
- Supports maximum resolution up to 5M pixel for JPEG decoder and encoder

(5).Video CODEC:

- Supports Motion JPEG recording, up to QVGA 15 fps
- Supports MPEG4 decoding, compliant with ISO/IEC 14496-simple profile, up to QCIF 25 fps.
- Support H263 decoding, compliant with ITU H.263 profile 0, up to QCIF 25 fps.

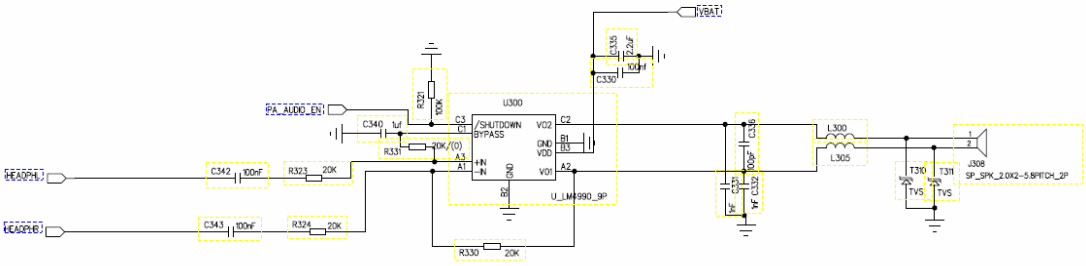
1.2.2 Memory

MCU internal memory controller controls four types of memory in MCU subsystem: MCU internal RAM, MCU internal ROM, MCU-DSP shared RAM and MCU-DSP switched RAM.

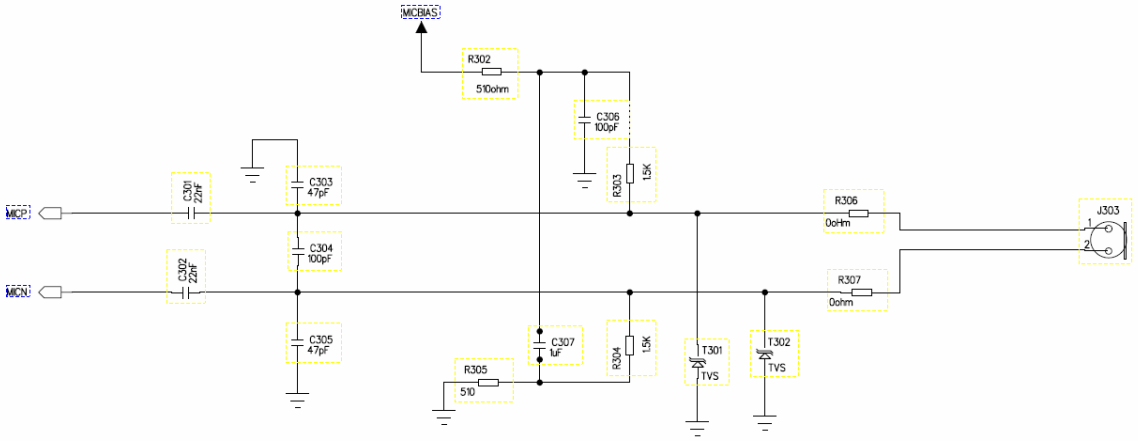
G153 support Nor memory

1.2.3 Audio Block

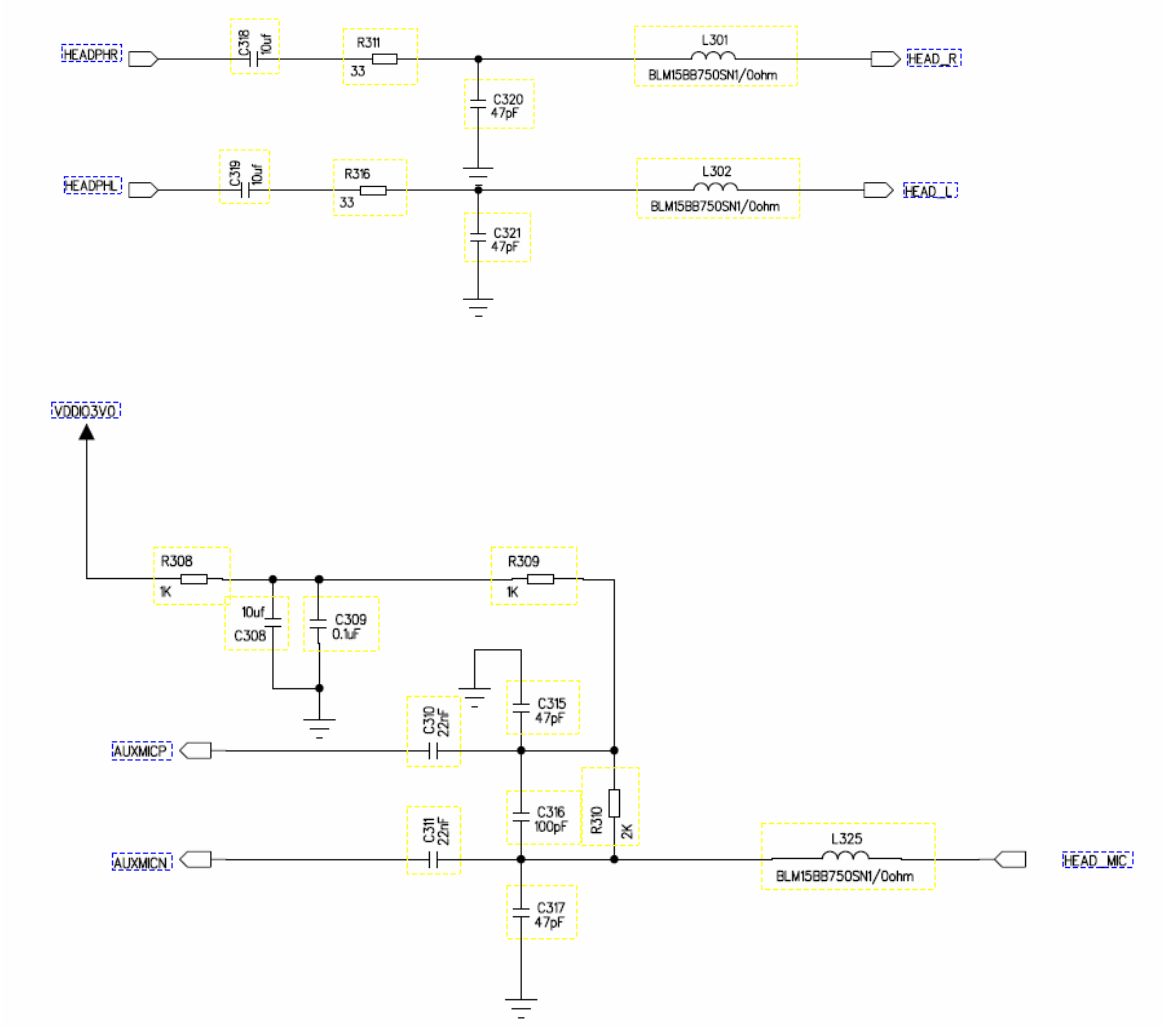
1) Speaker output circuit: SC6620 output AUXSPP and AUXSPN to Audio Power Amplifier, then drive two speaker for playing.



2) MIC Circuit: PCBA mic use differential circuit, the MIC bias voltage MICP /N is provided by SC6620.Mic Circuit support voice memo recording.



3) Headset detect circuit: When headset insert, generate the voltage interupt to SC6620.



1.2.4 LCD Module

G153 support 1.77 inch high-brightness TFT LCD, 65K Color with fulltransparant glass.

Resolution：128*160 Dots

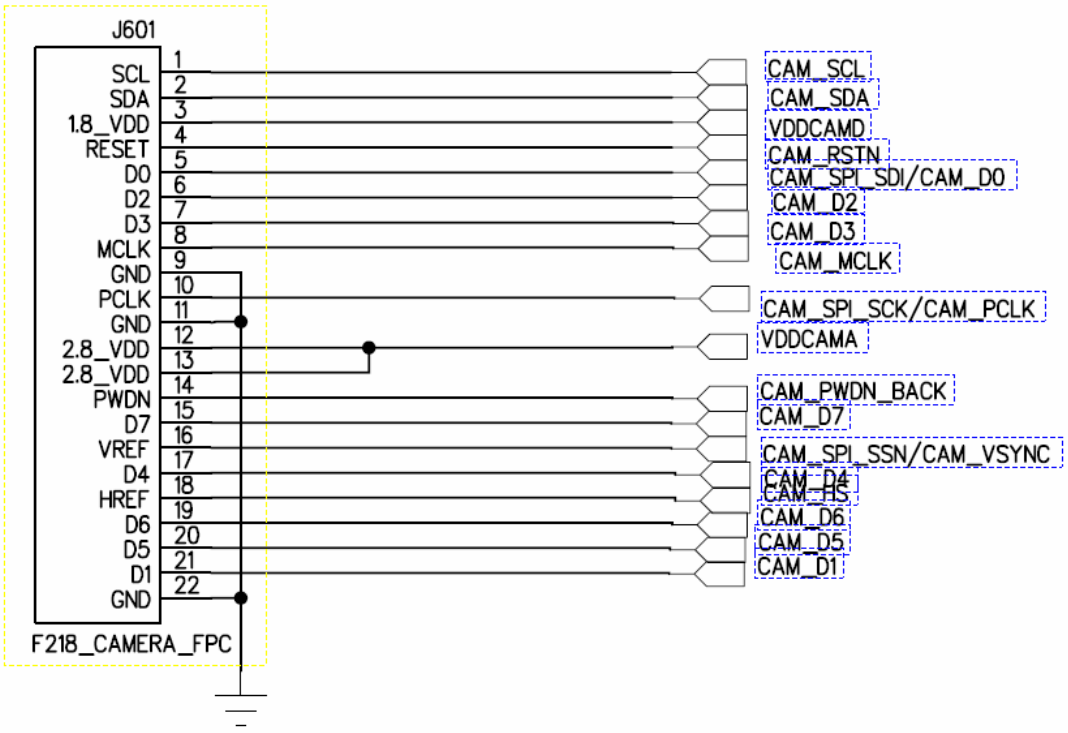
Backlight：White high-brightness LED

AA area：28.03（H）*35.04（V）（mm）

1.2.5 Camera Module

G153 implement JPEG encode/decode with external DSP processor.

Camera could fix the FPC on the connector.



1.2.6 Battery and Charger

1. Battery requirement

G153 use Li-ion battery for power supply. 3pin connector, with VBAT, GND pin. The specific size is count on different mechanical design.

2. Charger requirement

G153 use USB charger or switch on/off charger for charging. PMU charges the battery in three phases: pre-charging, constant current mode charging, and constant voltage mode charging.

1.3 RF Module blocks

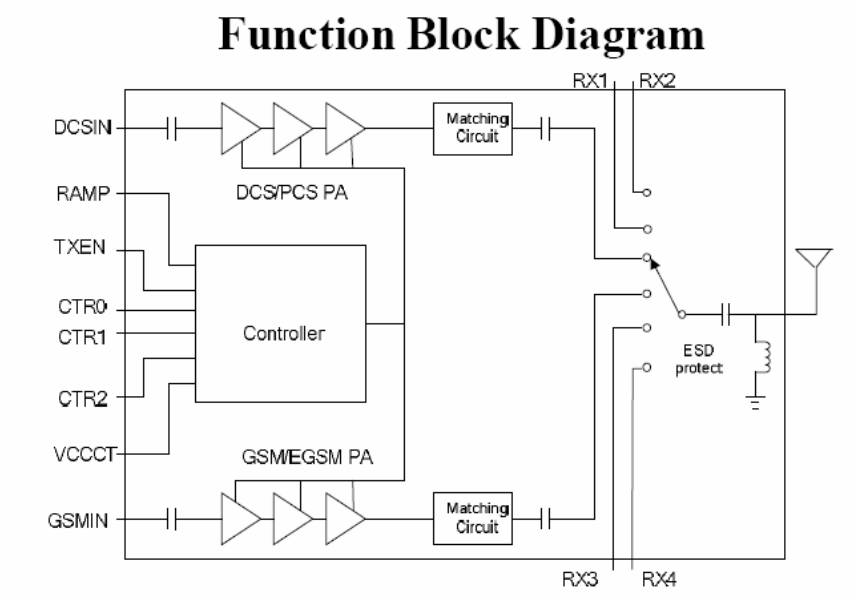
1.3.1 RF Power Amplifier

The RDA6231 is a high-power, high-efficiency dual-band front-end Module. This device is designed for EGSM900 and DCS handheld digital cellular equipment. The module consists of dual band power amplifiers and dual band antenna switch. The power amplifiers, switch and their controller are fabricated with GaAs HBT, GaAs PHEMT and CMOS respectively.

The device package is 6mm×6mm×1.1mm 28-pins LGA. The input and output are realized on-chip matched to 50Ω. The RDA6231 requires few external components, simplifying PCB layout and reducing PCB board space.

Features

- Ultra-Small 6mm×6mm Package
- Dual-Band Power Amplifier with RF switches
- 8KV ESD at Antenna
- Complete Power Control Solution
- High efficiency
- Low supply voltage (3~4.5V)
- Input/Output matched @ 50 Ω
- Advanced HBT/PHEMT/CMOS process



1.3.2 Transceiver

The Spreadtrum SR528 is a single-chip radio transceiver for quad-band GSM/GPRS cellular applications. The SR528 has been implemented in bulk CMOS and the design has been optimized to meet the challenges of integrated handset design.

The receiver part of SR528 supports both Zero-IF(ZIF), and Zear-IF(NZIF) systerm implementations. The performance of the transmit chain requires no additional RF fliters to meet the specification for out-of-band emissions. The SR528 exceeds all ETSI radio design requirements and its enhanced transmit architecture permits the rapid design of stable, high performance handsets only requiring a single radio shield.

Features:

(1).Industry leading receive current 55mA

(2).Available in 5mm×4mm×0.9mm 28L 0.5mm pitch QFN package

(3).Enhanced transmit architecture supports:

- Single radio shield
- Very low phase error
- Faster design cycles

(4).Integrated transceiver radio fully supporting GSM/GPRS receive and transmit for voice and data applications

(5).True Quad-band (USGSM850, EGSM900, DCS1800, and PCS 1900)

(6).ZIF and NZIF receiver architectures supported

(7).Direct down-conversion receiver eliminates image reject and IF fliters

(8).Receiver gain digitally selectable in 1 dB steps

(9).LO Modulation for GMSK

(10). No extra off-chip RF fliters required for transmit

(11). Extensive on-chipautomatic self-calibration

(12). Single integrated and programmable fast-settling multi-band LO synthesizer engine

(13). Temperature sensor built-in

(14). GPRS class 12 compliant

(15). 3-wire serials control interface

(16). 2.7V to 3.3V single supply voltage

(17). Lead-free/RoHS compliant

Applications:

(1).Highly integrated 2.5G quad-band cellular handsets

(2).Entry level and feature level mobile phone

(3).Wireless PDA and cardbus adapters

Transceiver Functions:

(1).Integrated radio transceiver fully supporting GSM, GPRS and receiver EGPRS

(2).GPRS class 12 supported

(3).Direct LO modulator in GMSK mode

General Functions:

(1).Mixed signal interface to a cellular base band

(2).Didital tuning of reference crystal

(3).2.7V to 3.3V single supply range

(4).-40℃ to +85℃ operation