15.0 CUSTOMER USER GUIDE INCLUDING FCC WARNING STATEMENT

Attached.

See page 5 for FCC Warning Statement

USER'S MANUAL

IPC486P8

089-00358-100

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Acknowledgment of Trademarks and Proprietary Names

Emulex:	Emulex Corporation
PC, PC/XT, PC/AT	IBM
Intel:	Intel Corporation
AMD:	Advanced Micro Devices
Zilog:	Zilog Corporation

Important Note:

Throughout this manual, options requiring a link to be fitted are indicated by the bar above the relevant option.

Example 1: **FIX PRIO** (fixed priority dma arbitration), means that if a jumper is fitted across this link, a fixed priority scheme will be used in DMAs arbitration operation (hard wired arbiter). If this jumper is omitted then a rotating priority scheme will be used.

Example 2: **CACHE DIS** (cache disable), means that if a jumper is fitted across this link, the CPU on-chip cache will be disabled. If this jumper is omitted then the CPU on-chip cache is enabled.

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MANUFACTURER'S NOTE

All material in this manual has been tried and tested and is believed to be correct at the time of printing.

No responsibility can be assumed for any omissions, inaccuracies, or mis-statement of facts, though where these exist, the manufacturer would be pleased to hear of them for future editions of this manual.

The material contained herein is not an exhaustive description of the iPC486P8 board and is intended for guidance only. Timing information where quoted, will have been estimated using data supplied by the appropriate device manufacturers.

We reserve the right to alter without notice, the specification, design, price or conditions of supply of any product or service.

SAFETY

The manufacturer confirms that this product does not present a hazard to health and safety when properly used for the purpose for which it was designed and provided also that the buyer or his/her agent takes reasonable and normal precautions in its use.

Although the iPC486P8 board does not use any voltage above 12V (nominal), attention is drawn to the fact that lethal voltages may be present in any PC enclosure and that proper precautions should be exercised when connecting or adjusting this equipment.

CUSTOMER SERVICE

For sales or technical advice please contact HTEC Ltd. Head office at 303-305 Portswood Road, Southampton SO17 2LD, Telephone 01703- 516000.

CARE OF THE iPC486P8 BOARD

iPC486P8 uses Static Sensitive Devices. The card is supplied in packaging which will protect it whilst in transit. It should only be removed from this packaging and subsequently handled by competent personnel observing Electrostatic Discharge precautions in a static safe environment. It is anticipated that once the card is installed, the target system will provide protection from Electrostatic Discharge.

Please ensure that the power to the PC system is turned Off (and sufficient time allowed for the storage capacitors to discharge), before inserting or removing the card.

PREREQUISITES

It is assumed that the user is familiar with the features of the 80486DX4 processor, Z85230 SCC, 8237A DMA Controller, 8259 Interrupt Controller, 8254 Timer, the PC, and their operation.

SCOPE

The objectives of this manual are as follows:

1- To outline the features of the iPC486P8 PCI board.

2- To give the system integrator sufficient information about the hardware features of the iPC486P8 card to enable it's successful installation in almost any PC system.

3- To provide technical information about programming and the operation of the hardware devices.

1 INTRODUCTION

1.1 OVERVIEW

This manual describes the hardware aspects of the HTEC iPC486P8 intelligent peripheral controller PCI board for servers and personal computers. The manual also includes technical information about the operation and programming of the card. The manual contains two major sections based on operations performed from the point of view of either the Host PC or the local processor. The Host view section describes the functions performed by the Host PC during communication with the iPC486P8 card. It describes parts of memory and interrupts used to monitor and control the board. The local view section describes functions of the local processor and parts that are accessible by the user programs running on the board.

1.2 DESCRIPTION

The iPC486P8 card has full implementation of the PCI 2.1 Compliant Target Bus Interface and is designed with provision of processor upgrade path to 486DX2-66, 486DX4-100 and 486DX5-133. The production version will be fitted with 3.3V 80486DX4-100 CPU. The PCI bus conforms to plug and play standard and is a factor of 30 times faster than ISA bus interface. From local point of view, the card (2 ports or a 4 ports version) is **%100 software compatible** with the Htec iPC486X and the Emulex DCP286i cards. That means, the existing software written for either of these cards, once loaded on to the card, will run with out any modifications

To eliminate the need for a second level cache, the memory system is implemented using fast SRAMs. All processor accesses (data read/write and code fetch) to the system memory will occur with zero wait state, including burst cycles and cache line fill. A minimum of 1 Mb of dual ported memory, expandable to 4 Mb (build option), will be included on-board.

Up to eight serial ports are implemented using the Zilog 85230 SCC communication chips supporting both asynchronous and most synchronous protocols. The ports electrical interface is either RS232 or RS422 (X.21) (via a Daughter Board option). The serial ports will be available via a small form factor (90mm x 100mm maximum) daughter card. The daughter board plugs onto the main board and contains drivers and connectors only. The daughter board feature enables HTEC to provide variety of interfaces without redesigning the Main Board. The Main Board is designed to support

2, 4 and 8 serial channels. For example, 8-channel RS232 card will use a daughter card with RS232 transceivers and 80-pin SCSI-2 connector. An 8-channel RS422 card will be using a daughter board with RS422 transceivers and 100-pin SCSI-2 connector. A 2-channel daughter card is user configurable and will be using both RS232 and RS422 transceivers and two 15-way (DB-15) connectors.

The card has up to sixteen independent channels of DMA on-board for full-duplex DMA operation on all 8 ports.

Other features include a 82C54 timer/counter providing three independently programmable timers, a 82C59 interrupt controller and PAL-based software lock feature.

1.3 Main Features

Processor: 80486DX4 running at 32 Mhz system clock speed (96 Mhz internally) with zero wait states.

Memory: Up to 4M bytes of onboard dual ported fast SRAM.

Cache: 16K bytes, Four Way Set associative buffered write through unified code and data.

Cache Consistency: It is maintained automatically by "bus watching" (snooping) mechanism.

Eight channels of high-speed serial ports onboard using Z85230 SCCs.

Sixteen channels of high-speed DMAs between SCC's and the shared memory allows DMA operation on eight full duplex lines.

Ports may be individually configured as either DTE or DCE using jumpers.

Three uncommitted timer/counters for user software with maskable interrupt support.

PCI 2.1 compliant 32 bit 33 Mhz Target Bus Interface to the Host PC.

Optional GAL based software lock feature.

MTBF greater than 70,000 hours (calculated from the British Telecom Handbook of Reliability Data HRD4).

Low power consumption, 2.5 Amp from 5V supply rail.

1.4 Product Specification

1.4.1 Functional Specification

CPU	80486DX4-100
Clock Speed	32 Mhz
Data Size	32 bits
Address Size	22 bits, 4M bytes address range
Memory	1M and 4M bytes SRAM Shared.
PC Bus Interface	PCI 2.1 compliant Target Interface
Serial Ports	Z85230 enhanced SCCs 8 channels
DMAs	16 channels using 8237A DMA controllers

1.4.2 Power Consumption

+5V : +/- 5% at 2.8 A Maximum 80486-DX2 66 Mhz CPU
+5V : " at 2.4 A " CPU at Reset.
+5V : " at 2.0 a " CPU Halted.

+12V: +/- 5% at 0.1 A "
-12V: +/- 5% at 0.1 A "

1.4.3 Physical Characteristics

Height 106 mm (PCI size)
Depth 312 mm (full size)
Width One PC slot.

1.4.4 Environmental

Storage temperature	40 to 75 degree Celsius.
Operating temperature	0 to 50 degree Celsius with force cooling (80486DX2-66).
Minimum Air Flow	200ft/min (80486DX2-66).
Humidity	0 to 90% non-condensing.

1.4.5 Approvals

The card complies with requirements of European and American EMC specifications as follows when installed in a compliant PC:

UL 1950
CSA C22.2 - 950 - M89
EN550022 Class B
FCC 15J Class B
EN55101 (when ratified)
EN50082-1 1992

1.5 FCC NOTICE

Notice: This equipment has been tested and found to comply with the limits for a Class B digital, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, these is no guarantee that interference will not occur in a particular installation . If this equipment does cause harmful interference to radio or television reception, which can be determined by switching the equipment Off and On, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult HTEC of HTEC representative for help.

Properly shielded and grounded cables and connectors must be used in order to meet FCC emission limits. Proper cables and connectors are available for HTEC. Htec is not responsible for any radio or television interference caused by using other than recommended cables and connections or by unauthorised changes or modifications to this equipment. Unauthorised changes or modifications could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subjected to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may caused undesired operation.

2. PC HOST VIEW

2.1 Introduction

This section describes how the Host PC communicates with the iPC486P8 card by controlling and monitoring the iPC486P8 operation. Included are descriptions of PCI bus architecture, dual ported memory, interrupts, Host Accessible Register (HAR) and PCI configuration space.

2.2 Bus Architecture

The card has a full implementation of a 32 bit 33 MHz PCI 2.1 Compliant Target Bus Interface to the Host PC. The Host can communicate with the card at speeds approaching 64 Mbytes/s data throughput. This is about 30 times faster than ISA bus data throughput. The card is fully compatible with Plug and Play Standard. The PCI bus interface provides for totally software driven initialisation and configuration via a separate Configuration Address Space including interrupt binding. iPC486P8 card provides 256 bytes of configuration registers for this purpose.

2.2.1 Configuration Space Organisation

This section defines the organisation of Configuration Space registers. It also lists the functions that is supported by the card via its configuration registers. The Configuration Space is intended for configuration, initialisation, and catastrophic error handling functions.

The Configuration Space is divided into a predefined header region and a device dependent region. A predefined header defined for the iPC486P8 card is of Type 00. The layout of this portion is shown in figure 1.

The following five fields deals with device identification. All these registers are read only:

Vendor ID: This field is read only and identifies the manufacturer of the device. Htec Vendor ID is 1507 Hex.

Device ID: This field identifies the particular comms card. At present the following identifiers are allocated by Htec:

2-Channels RS422/423/232/X.21, 4 DMA channels	Device ID = 00C0h
8-Channels RS232 card with 16 DMA channels	Device ID = 0008h
8-Channels RS422 card with 16 DMA channels	Device ID = 0010h

Revision ID: This field is an extension to the Device ID and indicates the card revision number. Valid numbers are 00, 01, 02 .....99 in BCD format.

Header Type: This field returns value 00h when is read and indicates a Type 00 header.

Class Code: This read only field is used to identify the generic function of the card. The register is broken into three byte-size-fields. The upper, middle and the lower bytes (at offset 0Bh, 0Ah and 09h respectively). The Class Code when read, it returns value 0B4000 hex to indicate a co-processor card.

Command Register: This register is located at offsets address 04h and provides coarse control over the iPC486P8 card's ability to respond to PCI cycles. When a value 0 is written to this register, the card is logically disconnected from the PCI bus for all accesses except configuration accesses. The card powers up with all 0's in this register. The description of Command Register bits are as follows:

Bit 0: R/W bit, controls card's response to I/O accesses. A value of 0 disables the card response to I/O accesses. A value 1 allows the card to respond to I/O accesses.

Note: This card is memory mapped only and does not use PCI I/O space.

Bit 1: R/W bit, controls card's response to Memory accesses. A value of 0 disables the card to respond to Memory accesses. A value 1 allows the card to respond to Memory accesses.

Bit 2: R/O bit, hard wired to return value of 0 when read (Target only device).

Bit 3: R/O bit, hard wired to return value of 0 when read (ignores all Special Cycle operations).

Bit 4: R/O bit. Memory Write and Invalidate Command. this bit is not supported. hard wired to return value of 0 when read.

Bit 5: R/O bit, VGA Palette Snoop. This bit not supported. Returns 0 value.

Bit 6: R/W bit, Parity Error Response. A value of 0 indicates that a parity error is ignored and operation continues. A value of 1 indicates that parity checking is enabled.

Bit 7: R/O bit, Wait cycle control. Controls whether or not the device does address/data stepping. This bit is not supported. Returns 0 value.

Bit 8: R/W bit, SERR# Enable. A value of 1 enables the SERR# driver.

Bit 9: R/O bit, Fast Back-to-Back Enable. This bit is not supported and is hard wired to return value of 0 when read.

Bit 10-15: Reserved.

Status Register : This register located at offset address 08h and is used to record status information for PCI bus events. The description of Status Register bits are as follows:

Bit 0-4: Reserved.

Bit 5: R/O bit. This bit will return value of 0 when read to indicate 33 Mhz PCI bus operation.

Bit 6: R/O bit. This bit will return value of 0 when read to indicate that user selectable configuration items are not supported.

Bit 7: R/O bit. This bit return 0 when read indicating that the fast back-to-back transactions are not supported.

Bit 8: This bit is implemented by bus masters. IPC486P8 card is a PCI target (slave) only. Thus this bit is not implemented.

Bit 9-10: These bits encode the timing of DEVSEL#. They are read only and indicate the slowest time that the card asserts DEVSEL#. These bit are read by the host. Upon read and it returns 10h.

Bit 11: The card never terminates a cycle with Target-Abort. Thus, this bit is not implemented.

Bit 12: A PCI master sets this bit on Target-Abort. This bit again is not implemented for a PCI target.

Bit 13: This bit is set by master device on master abort. Thus, it is not implemented for a PCI target card.

Bit 14: This bit is not implemented because the card does not assert SERR# signal.

Bit 15: This bit is not implemented because the card does not check for any parity error on the PCI AD(31:0) bus.

CacheLine Size: This register can be written and read, but the value has no effect on the operation of the card. It is set to 0 value after reset.

Latency Timer: R/O register. This register is not supported.

BIST; 0Fh: PCI Built-In Self Test. This register is R/O, and is not supported. It is set to 0 after reset.

Base Address Register0; 10h: This register is used by the Host (driver software) to map the iPC486P8 shared memory into the host memory 4 Gbytes address space. Bits 0-3 of this register are read only. Bit 0 returns "0" to indicate that this Base Address Register maps into Memory Space. Bit 1 and bit 2 when read return 00 to indicate that the base register is 32 bit wide and mapping can be done anywhere in the 32-bit Memory Space. Bit 4 returns "1" upon read to indicate to the host that the shared memory is prefetchable (i.e. there is no side effects on reads, the card returns all bytes on reads regardless of the byte enables status).

The number of upper bits that the card actually implements depends on how much of the address space the card will respond to. A 1 Mbytes version of the card would use the top 12 bits of the address register and returning zeros the other remaining bits (bits 4 to 19).

Bit 31 Bit 0

XXXX,XXXX,XXXX,0000,0000,0000,0000,1000

Power up software will determine how much address space the card is required by writing a value of all 1's to this register and then reading the value back. A 1M version will return 0's in bit locations 19 to 4 and thus effectively specifying a 1M address space required. Bit 31 to 20 is used by the host to locate the card any where in the 4 Gbytes address space.

Base Address Register1; 14h: IPC486P8 card contains a single 16-bit R/W Host Accessible Register (HAR). This register is used by the host to issue commands such as reset and interrupt to the card. This register is not visible to the local processor. Before Host can access this register, it must map it into its memory address space. The PCI Base Address Register 1 is used by the Host (driver software) for this purpose. The Base Address Register 1 resides at offset 14h in the configuration space and is 32 bit wide with bit 0 hardwired to logic "0". Bits locations 19 to 1 will always return logic "0" when read. Bits 20 to 31 are used by the host to map the 486P8 HAR anywhere within 4 Gbytes of host memory address on a 1M address boundary. See section 2.2.2 for definition of iPC486P8 Host Accessible Register.

Base Address Registers 2, 3, 4, and 5: These registers are not implemented.

Card CIS Pointer; 28h: Card Information Structure Pointer for PCMCIA. Not supported. R/O register and it is set to 0 after Reset.

Subsystem Vendor ID: R/O register. It is set to 0 after Reset.

Subsystem ID: R/O register. It is set to 0 after Reset.

Expansion ROM Base Address: R/O register. This register is not supported. It returns value of 0 when read.

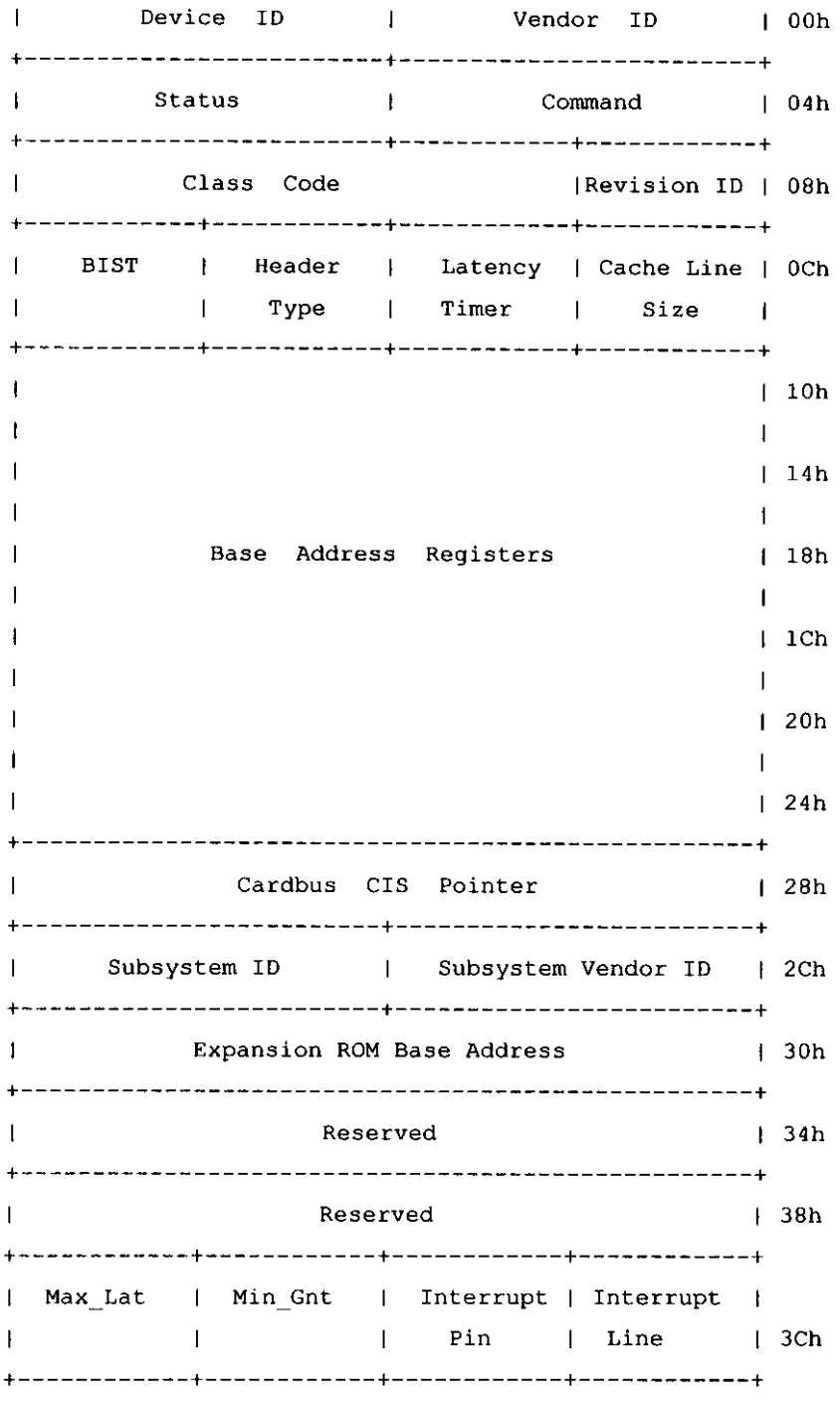
Interrupt Line: This is the PCI Interrupt Line Register which is written to by the Host PC to indicate which IRQ lines (IRQ2, 3, 4, 5, ...IRQ15) the card's interrupt line (INTA#) is connected to. See section xx for more detail.

Interrupt Pin: R/O register. It returns a value of 1 which indicates to the Host that the card uses PCI interrupt line INTA#.

Min_Gnt: This register is not supported. Returns value of 0 when read.

Max_Lat: This register is not supported. Returns value of 0 when read.

Figure 1. Type 00h Configuration Space Header



2.2.2 Host Accessible Register (HAR)

The iPC486P8 contains a single 16 bit wide (2 bytes, low byte and high byte) R/W register that is accessible by the host PC (appear in the PC memory map. It is pointed to by the PCI Base Address Register at offset 14h). This register is used only by the host PC (it is not visible to the iPC486P8 itself).

At PC power on, the local processor is in the reset state, giving control of the card to the host PC processor. All bits in the lower byte (bits 7-0) of HAR register are cleared to zero. This power-up reset operation allows the host PC to start the local processor in an orderly fashion once a program is loaded into the iPC486P8 memory.

The following chart shows the HAR low byte bit assignment. All bits in this register will be reset to zero after power up.

HAR Low Byte Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
CLIP	HIP	N/U	MI	EI	RES2	RES1	NMI
W/O	R/O		W/O	R/W	R/W	R/W	R/W

N/U = not used.

Note: W/O and N/U bits return zero when read.

BIT 0 (NMI= Non-Maskable Interrupt, Read and Write)

When this bit is set to "1" and then reset to "0" by the Host PC, it will generate a non-maskable interrupt to the local processor.

An internally supplied vector value of 2 will be generated by this interrupt. This bit is used by the Host PC to unconditionally get attention of the iPC486P8 card.

BIT 1 and BIT 2 (RES1, RES2= Reset Bits, Read and Write)

The iPC486P8 processor is at reset state after power up and is held in reset until both RES1 and RES2 bits are set to "1" by the Host PC. When local 486 processor is allowed to run, it jumps to memory address F000:FFF0 in real mode.

This power-up reset feature allows the host PC to start the local processor in an orderly fashion once a program is loaded into the iPC486P8 memory.

BIT 3 (EI= Enable Interrupt, Read and Write)

Providing that this bit is set to "1", then IPC486P8 can interrupt the Host PC by writing to local I/O location 3dch (see section xxxx for more detail). This bit is zero on power up.

BIT 4 (MI= Maskable Interrupt, Write Only)

When a bit "1" is written to this location by the Host PC, it generates a maskable vector interrupt to the local processor. This bit is connected to IRQ2 of the primary 8259 Interrupt Controller. This bit do not need to be reset to zero.

BIT 5 Not Used: Returns 0 when read.

BIT 6 (HOSTIP = Host Interrupt Pending Bit, Read Only)

This is an interrupt pending bit and indicates the status of the PCI interrupt pin #INTA. When read as "1" indicates that #INTA is active (active low). This bit must be cleared by the Host PC at the end of its interrupt service routine.

BIT 7 (CLRIP= Clear Interrupt Pending Flag, Write Only)

When a bit "1" is written to this location by the Host PC, it clears the Host interrupt bit . Always returns zero when read.

iPC486P8 card has a hex switch onboard which can be set to 16 positions, 0-9, A-F. This ID switch is read by applications software running on the Host PC via HAR high byte (D15-D8).

The following chart shows the HAR high byte bit assignment.

HAR High Byte Bit Assignments

D15	D14	D13	D12	D11	D10	D9	D8
N/U	N/U	N/U	N/U	SW8	SW4	SW2	SW1

Bits D11-D8 represents the switch setting. For example, if switch is set to hex digit "9" then D11-D8 will read 1001.

2.3 Host Interrupt Handling

The host PC is able both to generate and receive interrupts from the iPC486P8. The following explain how this will be done.

2.3.1 Generating Interrupts to the iPC486P8

The host PC can generate either a maskable or a non-maskable interrupts to the iPC486P8. A maskable interrupt will be generated by writing a "1" to the Host accessible Register (HAR) at bit position D4 (non-latchable). This generates a low going pulse at IRQ2 input of the 82C59 Interrupt Controller. The 82C59 must be initialised correctly in order for local processor to recognise the interrupt.

A non-maskable interrupt is generated by setting, then resetting, bit D0 of HAR Register. This bit is directly connected to the NMI input of the local processor. This interrupt is used to get the attention of the iPC486P8. Acknowledgement of the interrupt may be determined by the host PC reading a specific memory location in the shared memory. This bit is reset to 0 on power-up.

2.3.2 Receiving Interrupts from the iPC486P8

The iPC486P8 can generate interrupts to the host PC by writing to local I/O address 3DCh.

The interrupt will only be sent to the host PC if the Enable Interrupt bit in the HAR Register (bit d3) is set to 1.

A local I/O write to location 3dch will set the PCI interrupt pin #INTA to low level and HOSTIP flag (bit D7 of HAR Register) to logic "1". This interrupt pending flag should be cleared by the Host at the end of its interrupt service routine. Host does this by writing a "1" to bit location D7 of the HAR register. This generates a pulse that clears HOSTIP bit and sets #INTA to high .

3. LOCAL VIEW

3.1 Introduction

This section describes the local processor and all peripherals onboard the iPC486P8 card from the point of view of user program development requirements.

3.2 CPU

The iPC486P8 uses the Intel 80486DX4-100 processor running at a bus clock speed of 32 Mhz. The processor uses speed-multiplying technology and runs internally at 96 Mhz. It has a single clock cycle execution unit and many instructions execute in a single clock (10.4 nsec). Instruction pipelining allows fetching, decoding and execution of instructions to be overlapped within the processor. The 80486DX4 has 16K bytes of internal cache which is used for both data and instructions. Cache hit provides 10.4 nsec access time for data within the cache.

The CPU data and address busses are connected to 32 bit wide fast SRAM memory (12 nsec access time). At 32 Mhz system clock it runs with zero wait states burst and cache fill cycles (2-1-1-1 burst cycle) and zero wait state memory read/write cycles (2-2 cycles).

The 80486 CPU architecture features thirty four general purpose registers and a memory management unit. It has two modes of operations Real Address Mode (Real Mode), and Protected Virtual Address Mode (Protected Mode). In Real Mode it operates as a very fast 8086, but with 32-bit extensions if desired. After reset the 80486 CPU starts executing in Real Mode at the top of physical memory at location 0FFFFF0h.

For a general description of 80486 registers, addressing modes and instructions set, please refer to the Intel 486 Programmer's Reference Manual.

3.3 Memory

A minimum of 1 Mb of dual ported memory, expandable to 4Mb onboard. Use of fast SRAM memory provides a high performance processing engine which runs with zero wait state for processor burst and cache line fill (2-1-1-1 burst cycle) and zero wait state for processor read/write memory accesses.

The memory starts at address 00000h and will be implemented using either 128K x 8 or 512K x 8 SRAM chips. The memory is used by the local processor for program and data storage. The Host PC and the onboard DMA controllers can also access this memory. When a concurrent access to SRAM memory is required by the local processor, Host PC and DMA controllers, the priorities order are as follows:

PC has the highest priority followed by DMA and then local processor.

The Host PC access to the shared memory is implemented via high performance 32 bit PCI bus.

3.4 Serial Ports

Eight serial ports are provided onboard using the enhanced Zilog 85230 SCCs. These can be programmed to be either synchronous or asynchronous channels. All 8 ports can operate in half or full duplex operation with or without DMA support. **Note**: a 2 port version of the card has 2 serial ports and 4 DMA channels.

Currently three versions of the card are in existence, one with 2 channels user configurable RS422/423/232/X.21 interface, the second one with 8 channels of RS-232C interface and the third one with 8 channels of RS-422 interface. Each channel, On all versions, can be configured as either DTE or DCE via jumper links.

There will be four SCC's onboard providing eight serial ports as follows:

Port No.	SCC Channel	Data Register I/O Address	Control Register I/O Address
1	**SCC1 CH-A**	**3E3h**	**3E2h**
2	**SCC1 CH-B**	**3E7h**	**3E0h**
3	SCC2 CH-A	3E7h	3E6h
4	SCC2 CH-B	3E5h	3E4h
5	SCC3 CH-A	7E3h	7E2h
6	SCC3 CH-B	7E1h	7E0h
7	SCC4 CH-A	7E7h	7E6h
8	SCC4 CH-B	7E5h	7E4h

RS232 interface
character length: 5 to 8 bit
stop bits: 1.5 or 2
error checks: parity, overrun, framing error
baud rates: 50 to 38.4 Kbaud.

RS422 interface
Bisync, HDLC, SDLC
Sync: internal or external
error checks: CRC
baud rates up to 4M bits/sec.

The following signals will be supported for each port:

Signal	**RS422 (X.21)**	**RS232C**
Transmit Data	TXD(A)/TXD(B)	TXD

Receive Data	RXD(A)/RXD(B)	RXD
Request to Send	RTS(A)/RTS(B)	RTS
Clear to Send	CTS(A)/CTS(B)	CTS
Signal Ground	GND	GND
Receive Clock	RXC(A)/RXC(B)	RXC
Transmit Clock	TXC(A)/TXC(B)	TXC
Data Carrier Detect		DCD
Data Terminal Ready		DTR
Data Set Ready		DSR

3.4.1 PCLK Source to SCC's

Three PCLK rates will be supported, 7.3728 MHz, 14.7456 MHz and 16.000 MHz. The selection will be via LK1 jumper link. For 14.7456 Mhz SCC PCLK, insert jumper across pin 1-2, for 16 Mhz PCLK, insert jumper across pin 3-4 and for 7.3728 Mhz PCLK, omit jumpers.

3.4.2 SCC's Interrupt

All SCC's interrupt lines are ORed-wired together and connected to the INT input pin of the processor via a hardware interrupt arbiter. During the interrupt acknowledge cycle the highest priority SCC places an interrupt vector on the bus which is read by the processor. The interrupt vector is written in WR2 of either channel of the SCC during the initialisation. The following table shows the condition that will cause the interrupt:

Interrupt Condition	**Bit Modified**		
(If WR9 Bit 4 = "0")	D3	D2	D1
(If WR9 Bit 4 = "1")	D4	D5	D6
Channel B Tx Buffer Empty	0	0	0
Channel B External/Status Change	0	0	1
Channel B Rx Character Available	0	1	0
Channel B Special Receive Condition	0	1	1
Channel A Tx Buffer Empty	1	0	0
Channel A External/Status Change	1	0	1
Channel A Rx Character Available	1	1	0
Channel A Special Receive Condition	1	1	1

3.4.3 SCC Interrupt Priority

The hardware arbiter will normally give SCC interrupts priority over the 82C59 interrupts. The SCC will always receive the first interrupt

acknowledge, but the arbiter will pass the following acknowledge cycle to the 82C59, even if another SCC interrupt request comes in before that acknowledge. This ensures that SCC interrupt cannot monopolise the non-maskable interrupt request and lock out the 82C59 entirely.

Within SCCs individual channels, channel 1 has the highest priority and channel 8 the lowest.

3.5 DMA Support

Four Intel compatible 8237A DMA controllers (total of 16 DMA channels) are provided onboard in order to improve processor performance by allowing direct transfer between SCC's and SRAM memory (no intervention from the local processor). The HTEC proprietary hardware interface between the system bus and DMA controllers is used in order to double the system bus throughput. This novel interface will take only one tenth of the time normally needed for DMA device to complete the transfer on the system bus. Thus, in effect increasing the availability (bandwidth) of the system bus to other masters such as Host PC and the local processor in accessing the main memory.

Either half duplex or full duplex DMA operation (DMA on transmit and receive data) is supported for all sixteen channels. The allocation of DMA channels depends on the state of SDTR bits in the Local Control Registers 1 and 2 as shows below:

Local Control Register 1 (LCR1) at 3EAh

D7	D6	D5	D4	D3	D2	D1	D0
				SDTR6	SDTR5	SDTR2	SDTR1

Local Control Register 2 (LCR2) at 3F0h

D7	D6	D5	D4	D3	D2	D1	D0
				SDTR8	SDTR7	SDTR4	SDTR3

After power up all SDTR bit will be reset to "0" and the allocation of DMA channels 1, 2, 3, 4, 5, 6, 7, 8 will be to ports 1, 2, 3, 4, 5, 6, 7, 8 respectively in half duplex mode. For full duplex operation, all SDTR bits must be set to logic "1". The following table shows DMA channel allocation in both half and full duplex:

Table 2.1 DMA Channel Allocation

SCC Port Number	DMA Channel Allocated in Half Duplex Mode	DMA Channel Allocated in Full Duplex Mode
1	**1**	**1 and 3**
2	**2**	**2 and 4**
3	3	9 and 11
4	4	10 and 12
5	5	5 and 7
6	6	6 and 8
7	7	13 and 15
8	8	14 and 16

Note: each of the 16 channels of the DMA controllers will be connected to the SCC's DMA request lines W/REQ and DTR/REQ according to the following table:

SCC'S DMA Request Signal	DMA Ch Allocated in Half Duplex Mode SDTR1,2,3,...8 = 0	DMA Ch Allocated in Full Duplex Mode SDTR1,2,3,4,...8 = 1
W/REQ Port 1	**1 (DMA1)**	**1 (DMA1)**
W/REQ Port 2	**2 (DMA1)**	**2 (DMA1)**
W/REQ Port 3	3 (DMA1)	9 (DMA3)
W/REQ Port 4	4 (DMA1)	10 (DMA3)
W/REQ Port 5	5 (DMA2)	5 (DMA2)
W/REQ Port 6	6 (DMA2)	6 (DMA2)
W/REQ Port 7	7 (DMA2)	13 (DMA4)
W/REQ Port 8	8 (DMA2)	14 (DMA4)
DTR/REQ Port 1	**Used as DTR1 Signal**	**3 (DMA1)**
DTR/REQ Port 2	**Used as DTR2 Signal**	**4 (DMA1)**
DTR/REQ Port 3	Used as DTR3 Signal	11 (DMA3)
DTR/REQ Port 4	Used as DTR4 Signal	12 (DMA3)
DTR/REQ Port 5	Used as DTR5 Signal	7 (DMA2)
DTR/REQ Port 6	Used as DTR6 Signal	8 (DMA2)
DTR/REQ Port 7	Used as DTR7 Signal	15 (DMA4)
DTR/REQ Port 8	Used as DTR8 Signal	16 (DMA4)

Each DMA controller has End Of Process (EOP) signal which is pulsed whenever any of its DMA channels reaches Terminal Count. The EOP signals are connected to interrupt request inputs of the primary 82C59 controller in the following order:

EOP of DMA1 => IR1 of 82C59 Interrupt Controller.
EOP of DMA2 => IR4 "
EOP of DMA3 => IR1 "
EOP of DMA4 => IR4 "

3.5.1 DMA Page Addressing

The DMA page registers supply the upper 8-bits of 23-bit DMA address for each channel (note: DMA channels are limited to 16-bit address, thus, each channel capable of maximum transfer of 65,536 bytes). The bit assignment for the DMA page registers will be as shown below:

DMA Page Register Bit Assignment

D7	D6	D5	D4	D3	D2	D1	D0
A19	A18	A17	A16	N/A	N/A	A21	A20

DMA page registers are write-only and supply the eight most significant address bits during DMA cycle to the local memory. These registers will be undefined after power up.

The following tables show all four DMA's Register's I/O Addresses:

Table 3.6 First DMA Register's I/O Addresses

8237A First DMA Registers	Address Hex
DMA1 Base/Current Address Register - CH1	300
DMA1 Base/Current Word Count Register - CH1	301
DMA1 Base/Current Address Register - CH2	302
DMA1 Base/Current Word Count Register - CH2	303
DMA1 Base/Current Address Register - CH3	304
DMA1 Base/Current Word Count Register - CH3	305
DMA1 Base/Current Address Register - CH4	306
DMA1 Base/Current Word Count Register - CH4	307
DMA1 Command/Status Register	308
DMA1 Software Request Register	309
DMA1 Mask Register	30A
DMA1 Mode Register	30B
DMA1 Clear Byte Pointer Flip/Flop	30C
DMA1 Master Clear Register	30D
DMA1 Clear Mask Register	30E
DMA1 Set Mask Register	30F
DMA1 Page Register - CH1	310
DMA1 Page Register - CH2	311
DMA1 Page Register - CH3	312
DMA1 Page Register - CH4	313

Note: a two ports card has only on DMA chip (first DMA 4 channels)

Second DMA Register's I/O Addresses

8237A Second DMA Registers	Address Hex
DMA2 Base/Current Address Register - CH5	320
DMA2 Base/Current Word Count Register - CH5	321
DMA2 Base/Current Address Register - CH6	322
DMA2 Base/Current Word Count Register - CH6	323
DMA2 Base/Current Address Register - CH7	324
DMA2 Base/Current Word Count Register - CH7	325
DMA2 Base/Current Address Register - CH8	326
DMA2 Base/Current Word Count Register - CH8	327
DMA2 Command/Status Register	328
DMA2 Software Request Register	329
DMA2 Mask Register	32A
DMA2 Mode Register	32B
DMA2 Clear Byte Pointer Flip/Flop	32C
DMA2 Master Clear Register	32D
DMA2 Clear Mask Register	32E
DMA2 Set Mask Register	32F
DMA2 Page Register - CH5	314
DMA2 Page Register - CH6	315
DMA2 Page Register - CH7	316
DMA2 Page Register - CH8	317

Table 3.6 Third DMA Register's I/O Addresses

8237A Third DMA Registers	Address Hex
DMA3 Base/Current Address Register - CH9	330
DMA3 Base/Current Word Count Register - CH9	331
DMA3 Base/Current Address Register - CH10	332
DMA3 Base/Current Word Count Register - CH10	333
DMA3 Base/Current Address Register - CH11	334
DMA3 Base/Current Word Count Register - CH11	335
DMA3 Base/Current Address Register - CH12	336
DMA3 Base/Current Word Count Register - CH12	337
DMA3 Command/Status Register	338
DMA3 Software Request Register	339
DMA3 Mask Register	33A
DMA3 Mode Register	33B
DMA3 Clear Byte Pointer Flip/Flop	33C
DMA3 Master Clear Register	33D
DMA3 Clear Mask Register	33E
DMA3 Set Mask Register	33F
DMA3 Page Register - CH9	350
DMA3 Page Register - CH10	351
DMA3 Page Register - CH11	352
DMA3 Page Register - CH12	353

Fourth DMA Register's I/O Addresses

8237A Fourth DMA Registers	Address Hex
DMA4 Base/Current Address Register - CH13	340
DMA4 Base/Current Word Count Register - CH13	341
DMA4 Base/Current Address Register - CH14	342
DMA4 Base/Current Word Count Register - CH14	343
DMA4 Base/Current Address Register - CH15	344
DMA4 Base/Current Word Count Register - CH15	345
DMA4 Base/Current Address Register - CH16	346
DMA4 Base/Current Word Count Register - CH16	347
DMA4 Command/Status Register	348
DMA4 Software Request Register	349
DMA4 Mask Register	34A
DMA4 Mode Register	34B
DMA4 Clear Byte Pointer Flip/Flop	34C
DMA4 Master Clear Register	34D
DMA4 Clear Mask Register	34E
DMA4 Set Mask Register	34F
DMA4 Page Register - CH13	354
DMA4 Page Register - CH14	355
DMA4 Page Register - CH15	356
DMA4 Page Register - CH16	357

3.5.2 DMA Priority Selection

Each 82C37A DMA controller chip (there are four onboard) has two types of software selectable priority encoding scheme. A Fixed and a Rotating Priority schemes. The Fixed Priority scheme gives the highest priority to channel 1 and the lowest priority to channel 4. In the Rotating Priority scheme the last channel to get service becomes the lowest priority channel with the others rotating accordingly. An eight channel version of iPC486P8 has four DMA controllers onboard. A hard-wired rotating priority scheme has been employed to define the priority order between the DMA controller chips. In this priority scheme the last DMA chip to get service becomes the lowest priority DMA chip with other DMA chips rotating accordingly. The selection of Priority scheme between DMA controllers is selected via link LK1 pins 5-6. For a fixed priority scheme insert jumper across pin 5-6 of Lk1. For Rotating priority scheme omit jumper.

3.5.3 DMA Hardware Implementation

In order to maintain software compatibility with DCP286i, HTEC386 and DCP386i/e cards, the following constrains are implemented on the DMA hardware:

i) Memory to memory DMA transfer operation is not supported. Thus, bit D0 of Command Registers must be set to "0".

ii) Only DMA transfer cycles with normal timing is implemented and Compressed timing is not supported. Thus, bit D3 of Command registers must be set to "0".

iii) Due to hardware implementation, bit D5 of the Command Register must be programmed to logic "0" for late write cycles generation.

iv) Due to hardware implementation, DMA request lines (DREQs) are active low. Thus, bit D6 of Command Register must be set to logic "1".

v) Due to hardware implementation DMA's DACKs signals is expected to be active low. Thus, bit D7 of Command Registers must be set to logic "0".

vi) Due to hardware implementation the operating mode of DMA controllers should be set to Single Mode. Thus, bits D6 and D7 of Mode Registers must be set to logic "1" and "0" respectively.

3.6 Programmable Timer

There is a programmable counter/timer onboard (82C54) providing three uncommitted 16-bit timers for user software with maskable interrupts support. The counter is clocked at 460.8 KHz and is identical to that of the HTEC IPC386 and the Emulex DCP286i cards. The I/O addresses of 82C54 registers are as follows:

82C54 Counter/Timer I/O Addresses

Register Description	Port I/O Address 82C54
Count Register 0	0284h
Count Register 1	0285h
Count Register 2	0286h
Control Register	0287h

3.6.1 Programmable Interrupt Controller

The card includes an 82C59 interrupt controller. The interrupt controller is identical to that of DCP286i and the HTEC iPC386 cards and will receive interrupts from a number of sources as shown below:

Primary 82C59 Interrupt Request I/P	Allocation
IR0	Not Used
IR1	End of Process EOP1 and EOP3 (DMA 1 and 3)
IR2	Maskable Interrupt from Host PC
IR3	Primary Timer Channel 2
IR4	End of Process EOP2 and EOP4 (DMA 2 and 4)
IR5	Not Used
IR6	Primary Timer Channel 0
IR7	Primary Timer Channel 1

3.6.2 82C59 Interrupt Priority

The hardware arbiter will give SCC interrupts priority over the 82C59 interrupts. It also ensures that SCC interrupt cannot monopolise the non-maskable interrupt request and lock out the 82C59 entirely. The interrupt

priority within 82C59 is under program control and can either be fixed or be rotating priority.

3.7 Local Control and Status Registers

3.7.1 Local Control Registers

There are two local Control registers and three Local Status registers. A local Control Registers 1 is at I/O address 03eah and the Local Control Register 2 at local I/O address 03F0h.

3.7.1.2 Local Control Register 1 (at 03EAh)

This write only register is used to setup ports 1, 2, 5 and 6 for full-duplex DMA operation. Its bit assignment will be as follows:

Local Control Register 1 Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
RSVD	RSVD	RSVD	RSVD	SDTR6	SDTR5	SDTR2	SDTR1

Bit 0 - Full-duplex Port 1 and Data Terminal Ready Port 1

When set to "1", this bit enables full-duplex DMA for port 1 and asserts DTR for port 1. When cleared to "0", port 1 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC1 channel A. Note that when full-duplex DMA operation is selected, DMA channels 1 and 3, in the first DMA controller, are allocated to port 1. This bit is cleared after power up.

Please note: each DMA controller has four DMA channels 1, 2, 3 and 4. There are 4 DMA chips on board providing 16 DMA channels 1, 2, 3, ... 16.

Bit 1 - Full-duplex Port 2 and Data Terminal Ready Port 2

When set to "1", this bit enables full-duplex DMA for port 2 and asserts DTR for port 2. When cleared to "0", port 2 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC1 channel B. Note that when full-duplex DMA operation is selected, DMA channels 2 and 4, in the first DMA controller, are allocated to port 2. This bit is cleared after power up.

Bit 2 - Full-duplex Port 5 and Data Terminal Ready Port 5

When set to "1", this bit enables full-duplex DMA for port 5 and asserts DTR for port 5. When cleared to "0", port 5 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC3 channel A. Note that when full-duplex DMA operation is selected, DMA channels 1 and 3, in the second DMA controller, are allocated to port 5. This bit is cleared after power up.

Bit 3 - Full-duplex Port 6 and Data Terminal Ready Port 6

When set to "1", this bit enables full-duplex DMA for port 6 and asserts DTR for port 6. When cleared to "0", port 6 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC3 channel B. Note that when full-duplex DMA operation is selected, DMA channels 2 and 4, in the second DMA controller, are allocated to port 6. This bit is cleared after power up.

3.7.1.3 Local Control Register 2 (at 03F0h)

This write only register will be used to set up ports 3, 4, 7 and 8 for full-duplex DMA operation. Its bit assignment will be as follows:

Local Control Register 2 Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
RSVD	RSVD	RSVD	RSVD	SDTR8	SDTR7	SDTR4	SDTR3

Bit 0 - Full-duplex Port 3 and Data Terminal Ready Port 3

When set to "1", this bit enables full-duplex DMA for port 3 and asserts DTR for port 3. When cleared to "0", port 3 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC2 channel A. Note that when full-duplex DMA operation is selected, DMA channels 1 and 3, in the third DMA controller, are allocated to port 3. This bit is cleared after power up.

Bit 1 - Full-duplex Port 4 and Data Terminal Ready Port 4

When set to "1", this bit enables full-duplex DMA for port 4 and asserts DTR for port 4. When cleared to "0", port 4 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC2 channel B. Note that when full-duplex DMA operation is selected, DMA channels 2 and 4, in the third DMA controller, are allocated to port 2. This bit is cleared after power up.

Bit 2 - Full-duplex Port 7 and Data Terminal Ready Port 7

When set to "1", this bit enables full-duplex DMA for port 7 and asserts DTR for port 7. When cleared to "0", port 7 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC4 channel A. Note that when full-duplex DMA operation is selected, DMA channels 1 and 3, in the fourth DMA controller, are allocated to port 7. This bit is cleared after power up.

Bit 3 - Full-duplex Port 8 and Data Terminal Ready Port 8

When set to "1", this bit enables full-duplex DMA for port 8 and asserts DTR for port 8. When cleared to "0", port 8 is selected for half-duplex DMA and the modem control signal, DTR, is controlled by WR5, bit 7 of the SCC4 channel B. Note that when full-duplex DMA operation is selected, DMA channels 2 and 4, in the fourth DMA controller, are allocated to port 8. This bit is cleared after power up.

3.7.2 Local Status Registers

There are three local status registers on the board at I/O addresses 03EAh, 03F0h and 03A0h. These registers are mainly responsible for monitoring Data Set Ready (DSR) status. Note that the 85C30 SCC does not have a dedicated pin for the DSR signal. Thus, this signal is made available through the Status Registers.

3.7.2.1 Local Status Register (at 3EAh)

An I/O read from this port provides the status of the DSR signal for serial ports 1, 2, 3 and 4 on the iPC486P8. A logical "0" indicates DSR is asserted on the line, and a logical "1" indicates DSR is not asserted on the line. The format of the Local Status Register 1 is shown below.

Local Status Register 1 Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
DSR4 PORT4	DSR3 PORT3	**DSR2** **PORT2**	**DSR1** **PORT1**	FDX/ DTR PORT6	FDX/ DTR PORT5	**FDX/** **DTR** **PORT2**	**FDX/** **DTR** **PORT1**

Bits 0-3 - Full-duplex/DTR Status Monitoring

These bits reflects the status of bits 0-3 of the Local Control Register 1.

Bits 4-7 - Data Set Ready

The Data Set Ready bits indicate the status of the DSR signal. When read as "0", they indicate that Data Set Ready is active from ports 1-4, respectively.

3.7.2.2 Local Status Register 2 (at 3F0h)

The format of the Local Status Register 2 is shown below.

Local Status Register 2 Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
DSR8 PORT8	DSR7 PORT7	DSR6 PORT6	DSR5 PORT5	FDX/ DTR PORT8	FDX/ DTR PORT7	FDX/ DTR PORT4	FDX/ DTR PORT3

Bits 0-3 - Full-duplex/DTR Status Monitoring

These bits reflects the status of bits 0-3 of the Local Control Register 2.

Bits 4-7 - Data Set Ready

The Data Set Ready bits indicate the status of the DSR signal. When read as "0", they indicate that Data Set Ready is active from ports 5-8, respectively.

3.7.2.3 Local Status Register 3 (at 3A0)

The format of the Local Status Register 3 is shown below.

Local Status Register 3 Bit Assignments

D7	D6	D5	D4	D3	D2	D1	D0
COD4	COD3	COD2	COD1	COD0	0	HSTIP	NMI

Bit 0 = NMI - This bit is same as bit 0 of the Host Accessible Register HAR that is mapped by the Host into its PCI memory address space..

Bit 1= HSTIP - Shows status of Host Interrupt Pending bit. This bit is the same as bit D6 of HAR register mapped by the Host into its PCI memory address space.

Bit 3 TO 7 Board Identification Number

This field identifies the particular comms card. At present the following identifiers are allocated by Htec:

8-Channels RS232 card with 16 DMA channels	Device ID = 08h
8-Channels RS422 card with 16 DMA channels	Device ID = 10h
2-Channels RS422/423/232/X.21 4 DMA channels	Device ID = C0h

3.8 Serial Number PAL

A PAL socket is provided that can be fitted with a 16V8 GAL. The PAL functions as a read-only memory with a unique serial number programmed into it.

3.9 Software Compatibility

From the local point of view, the card is 100% software compatible with the Emulex DCP286i and iPC486X/XT cards.

4. 2 PORTS RS232/422/423/X.21 DAUGHTER BOARD

4.1 General Description

The two ports daughter card has two channels of user configurable transceivers (physical interface). The user can configure the ports individually as either RS232, RS422 or RS423 via link setting.

The following physical interfaces are supported. The interface for channel 1 and 2 can be individually selected as either RS422\X.21 or RS232\423 via links LK3, LK4, Lk5 and LK6. The following table shows how to chose a particular interface for each channel:

TABLE 4.1 SELECTING INTRERAFCE FOR PORT 1

CHANNEL NUMBER	INTERFACE OPTION	LK3 CLUSTER	LK5 CLUSTER
1	RS232/423	JUMPER COL 2-3	JUMPER COL 2-3
1	RS422\X.21	JUMPER COL 1-2	JUMPER COL 1-2

TABLE 4.2 SELECTING INTERFACE FOR PORT 2

CHANNEL NUMBER	INTERFACE OPTION	LK4 CLUSTER	LK6 CLUSTER
2	RS232/423	JUMPER COL 2-3	JUMPER COL 2-3
2	RS422\X.21	JUMPER COL 1-2	JUMPER COL 1-2

4.3 Setting Data Clock Direction (DTE or DCE)

Each channel has an associated link block that are used to set data clock direction as either DTE or DCE. Note: the term DTE describes the external clocking and the term DCE describes the internal clocking.

Link blocks LK1 and LK2 set data direction for channels 1 and 2 respectively, as shown in the following table.

TABLE 4.3 SELECTING CLOCK DIRECTION FOR PORT 1

CHANNEL NUMBER	INTERFACE OPTION		LK1 CLUSTER
1	DTE	JUMPER	1-2, 3-4, 5-6, 7-8, 9-10
1	DCE	JUMPER	11-12

TABLE 4.4 SELECTING CLOCK DIRECTION FOR PORT 2

CHANNEL NUMBER	INTERFACE OPTION		LK2 CLUSTER
1	DTE	JUMPER	1-2, 3-4, 5-6, 7-8, 9-10
1	DCE	JUMPER	11-12

The two ports daughter card has two channels of user configurable transceivers (physical interface). The user can configure the ports individually as either RS232, RS422 or RS423 via link setting.