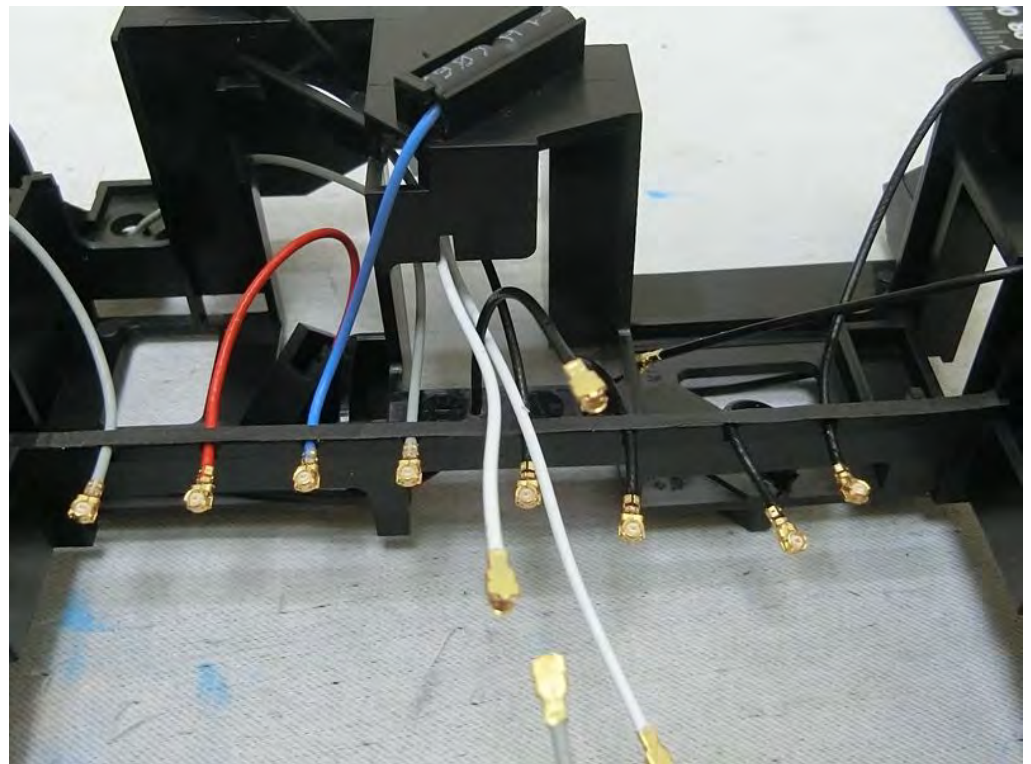
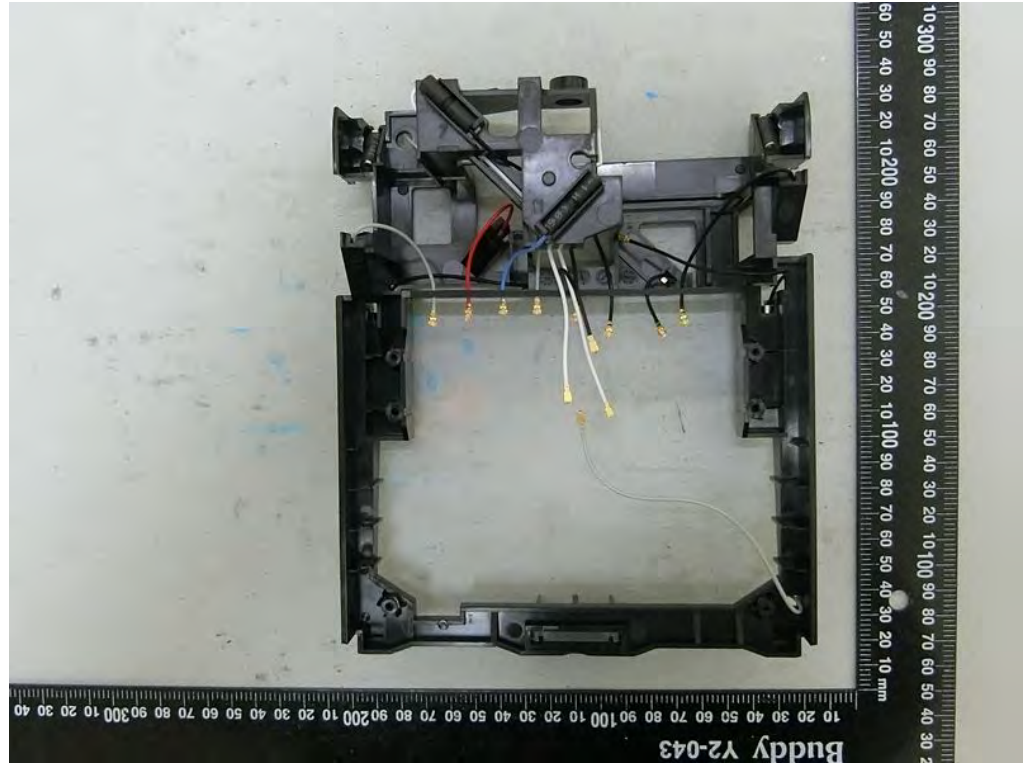
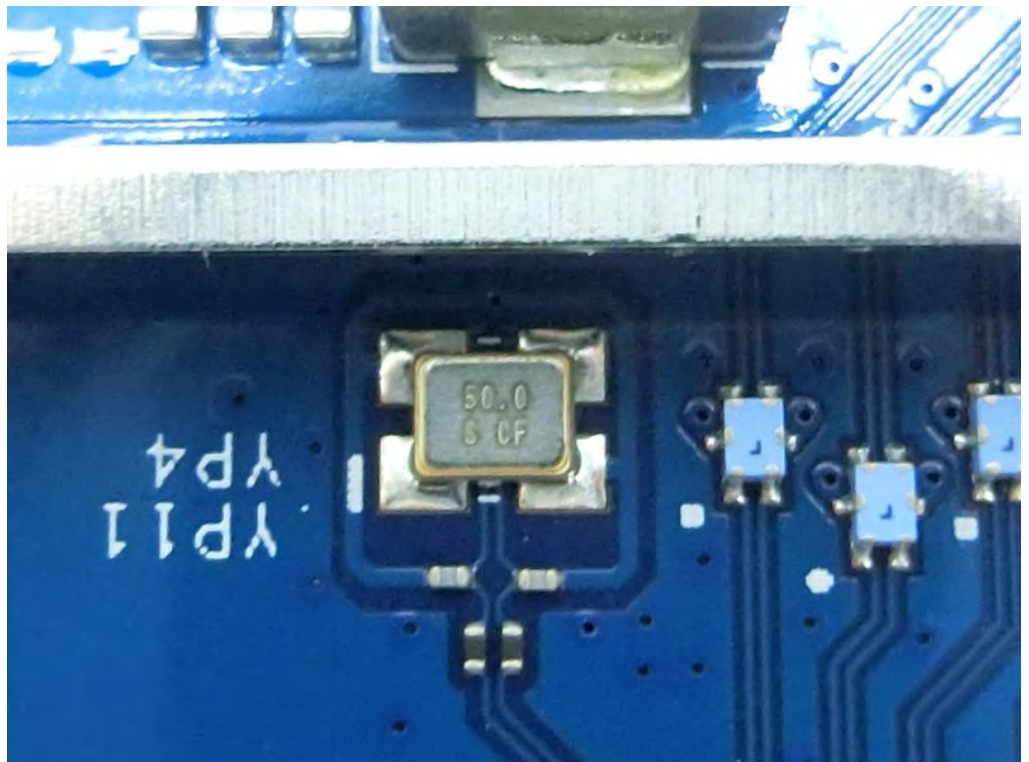
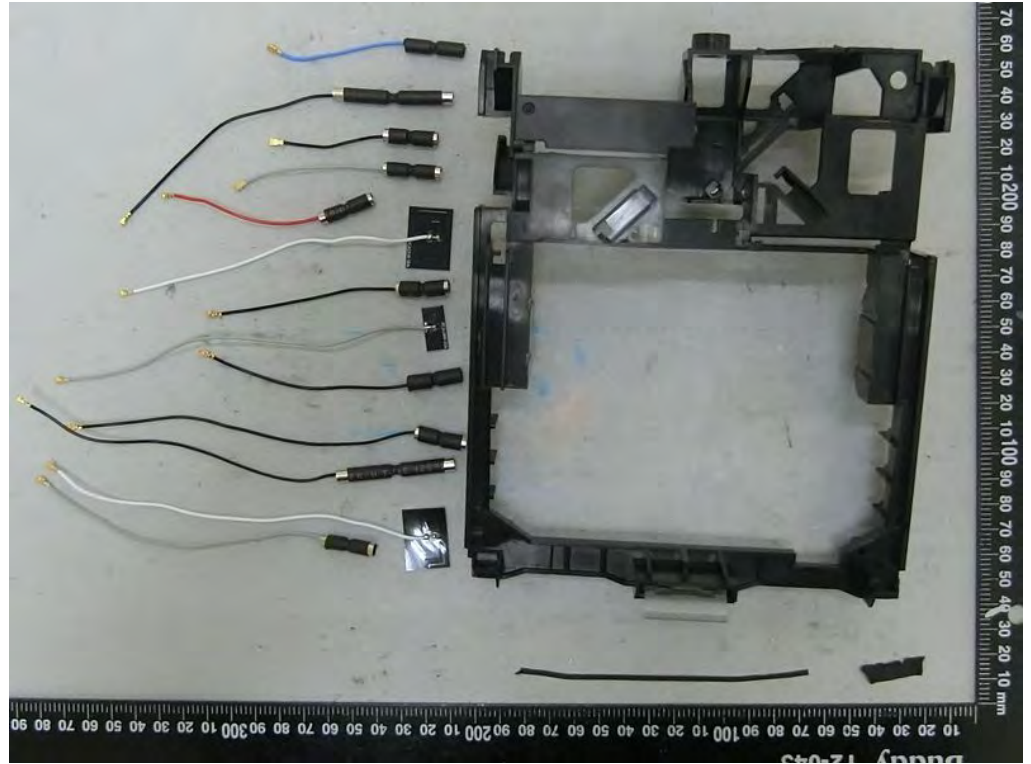


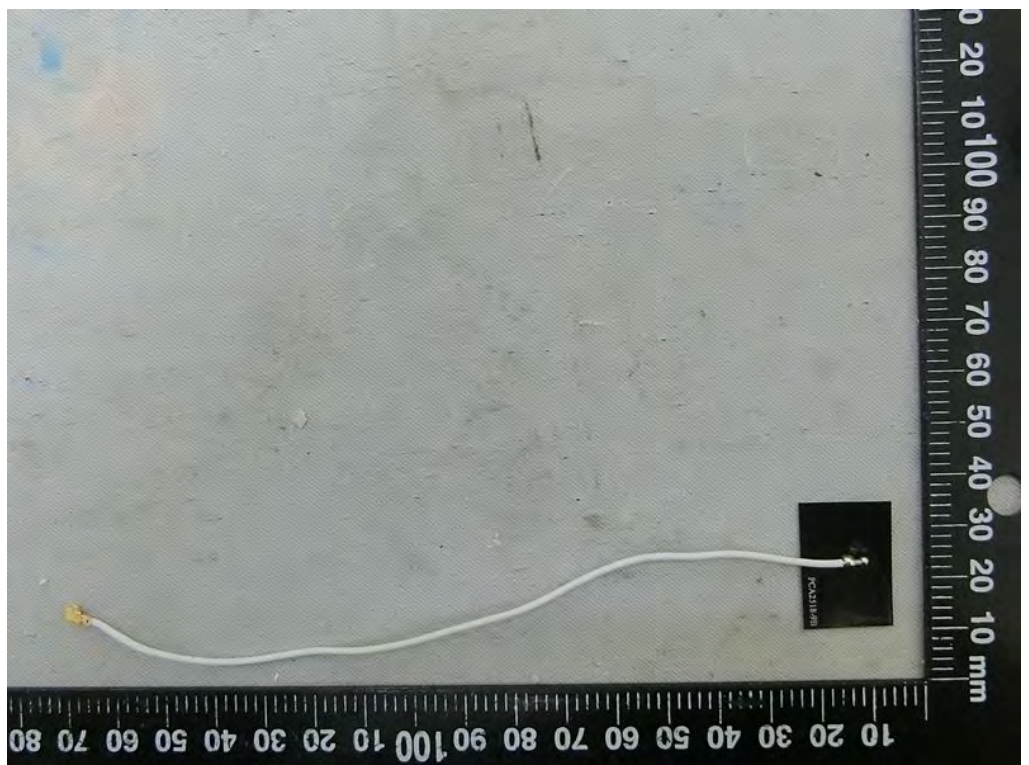
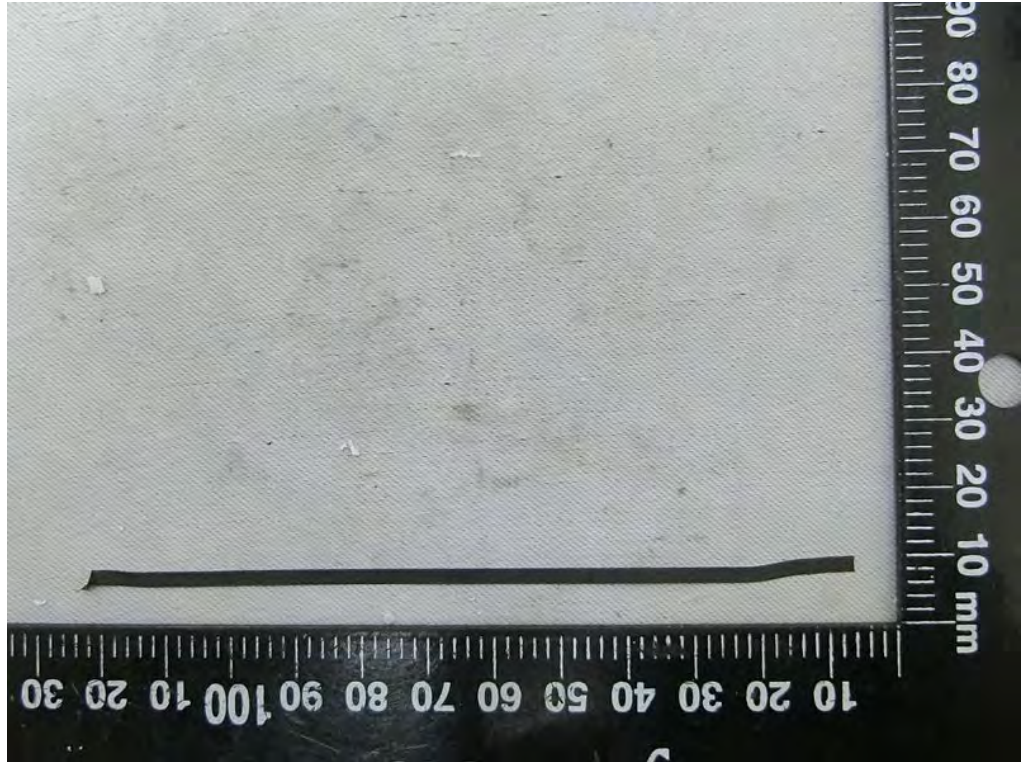
Integrated circuit
packaging
(Location: UP1)

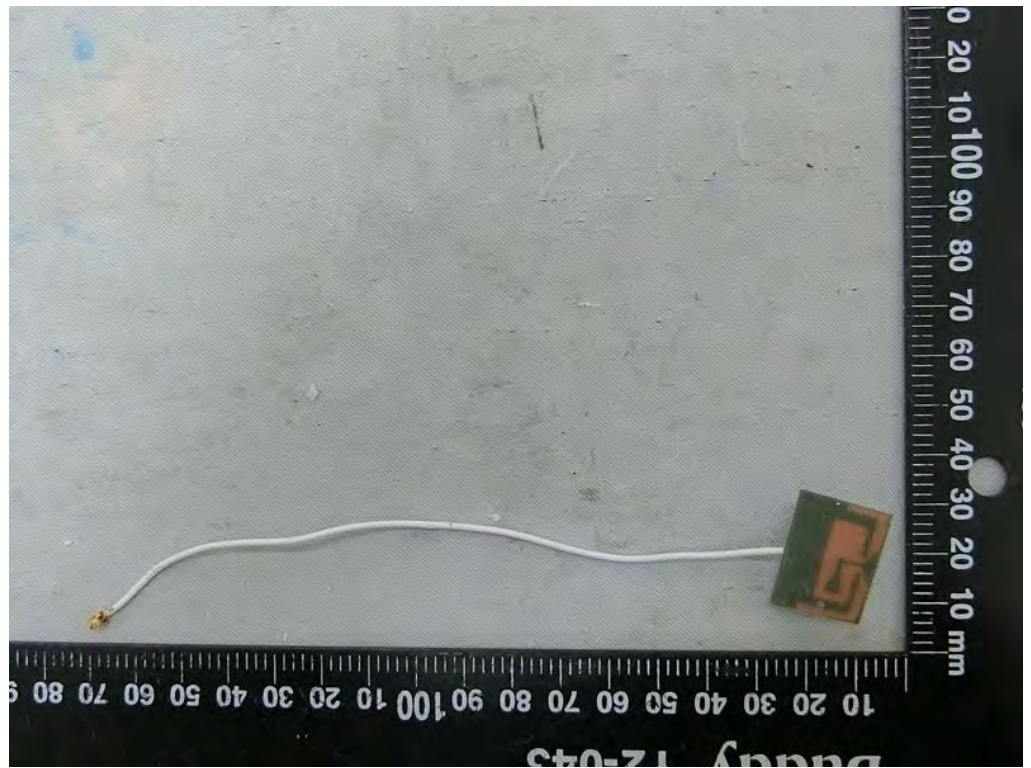


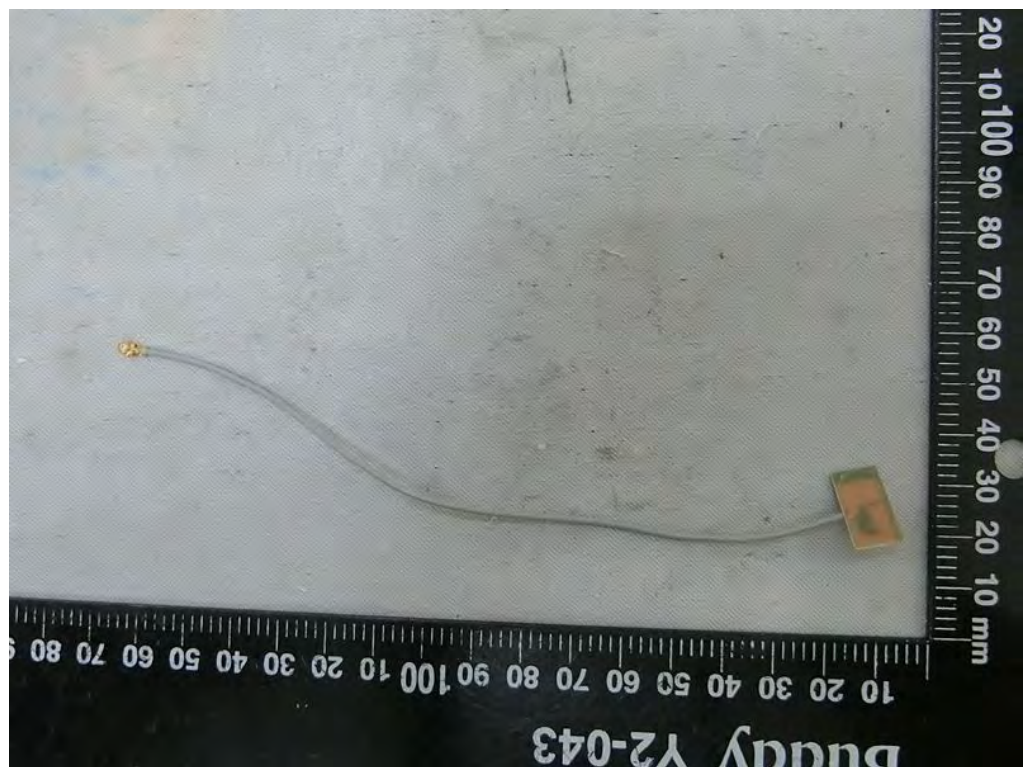
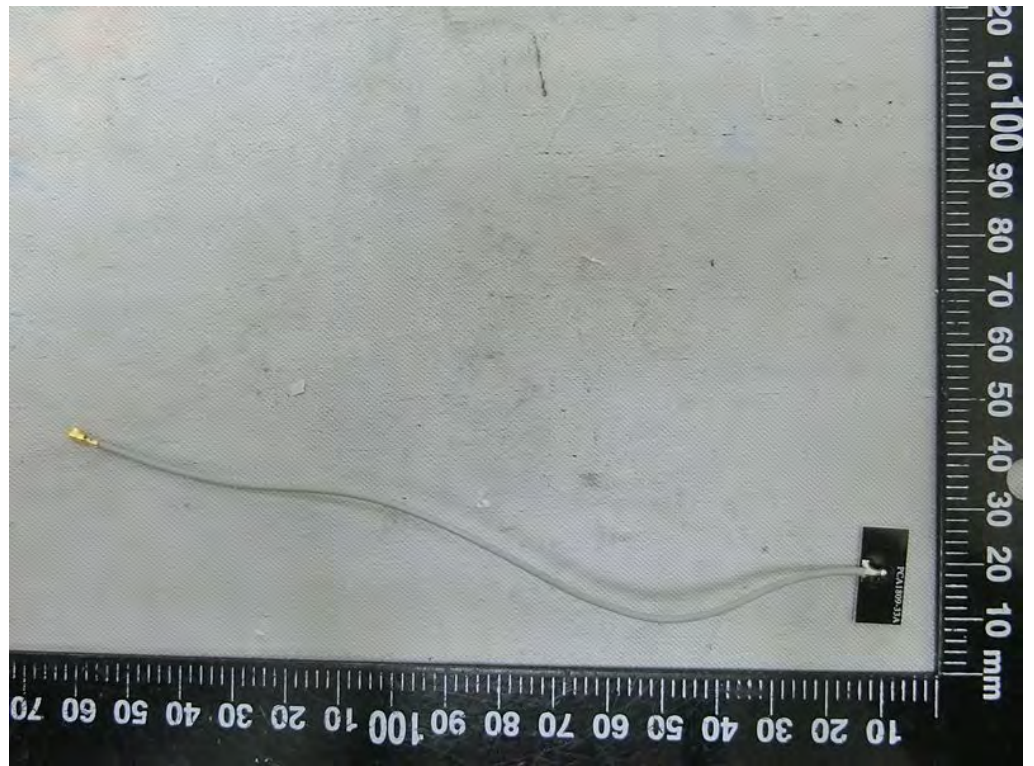


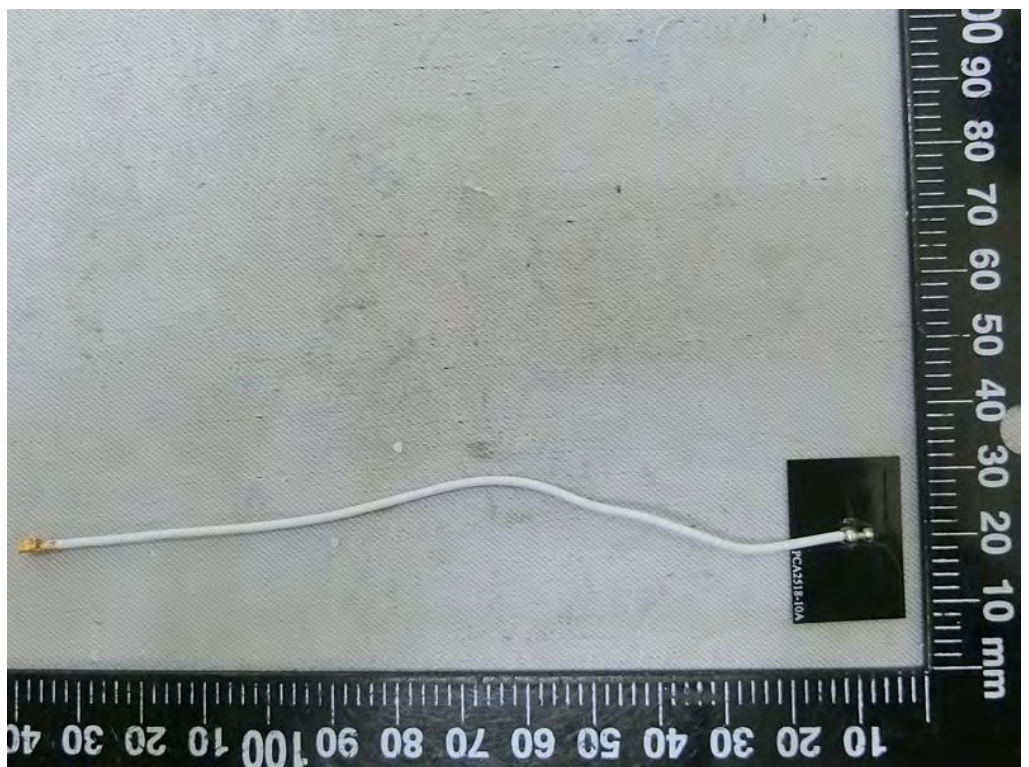


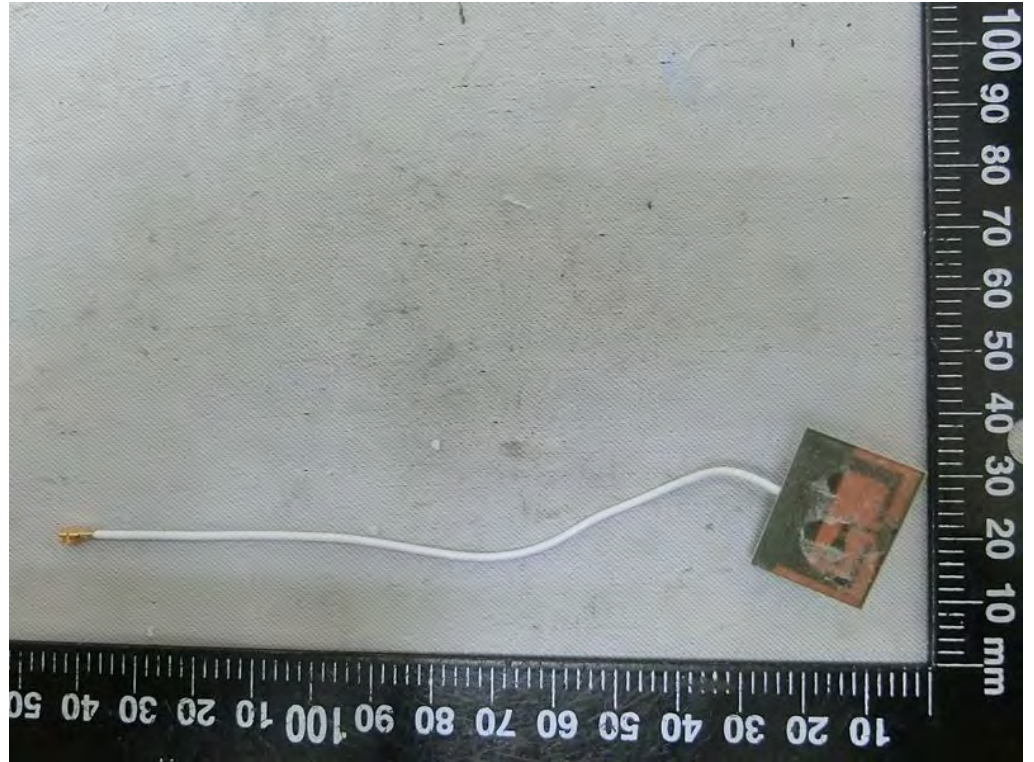


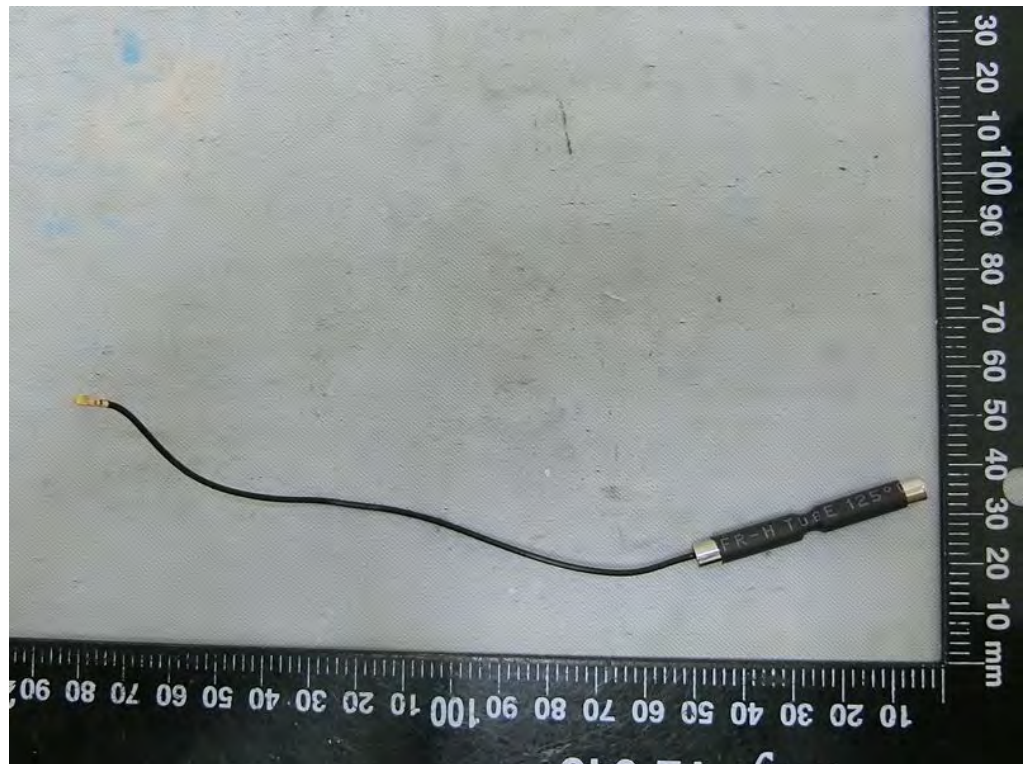
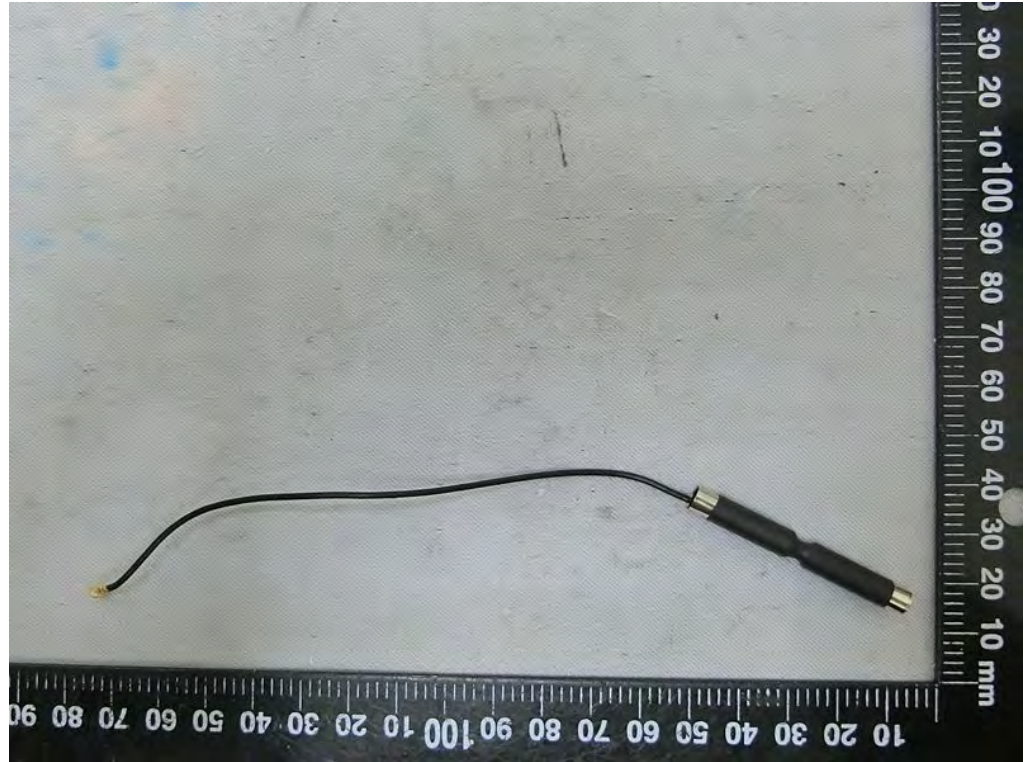


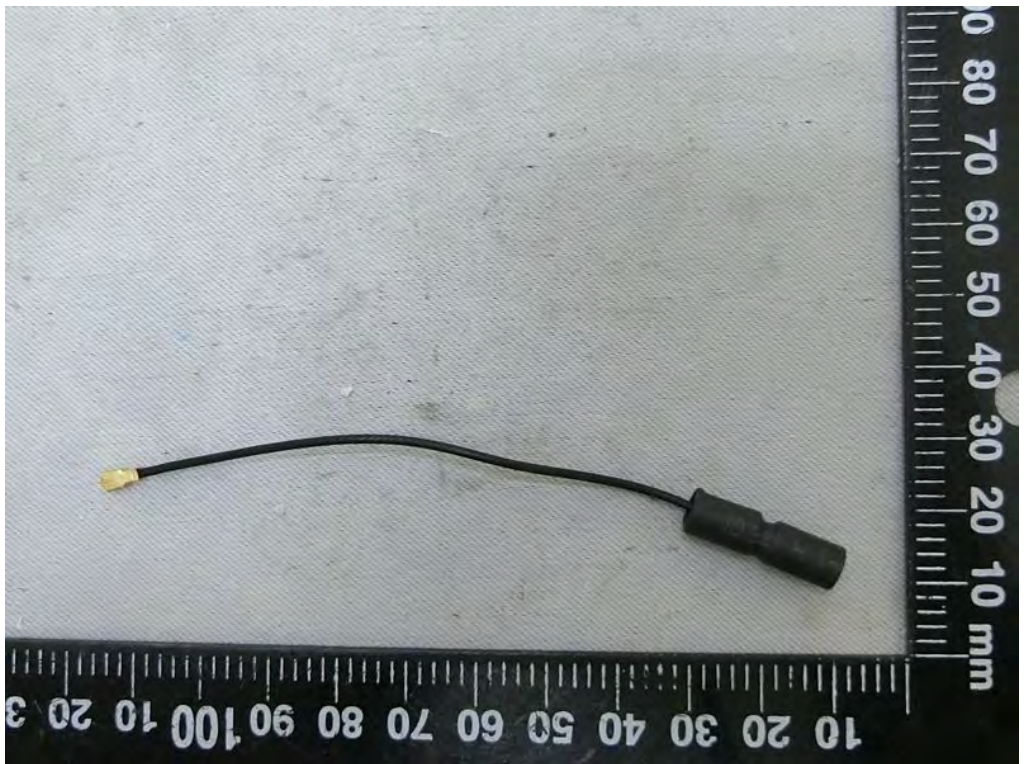


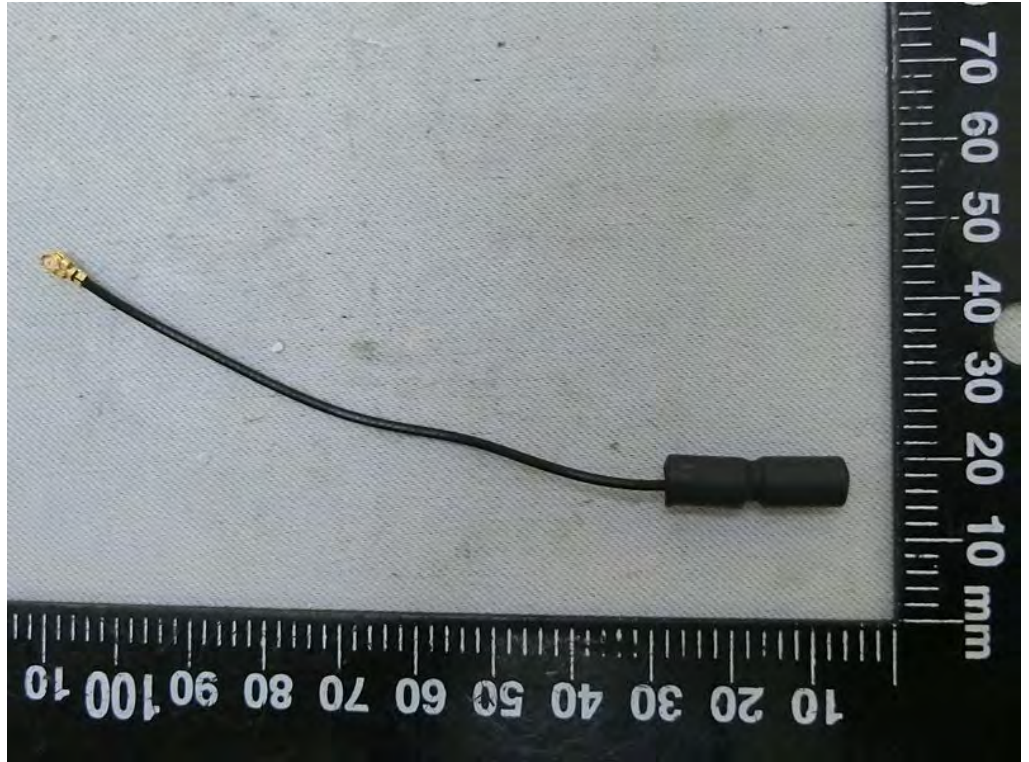


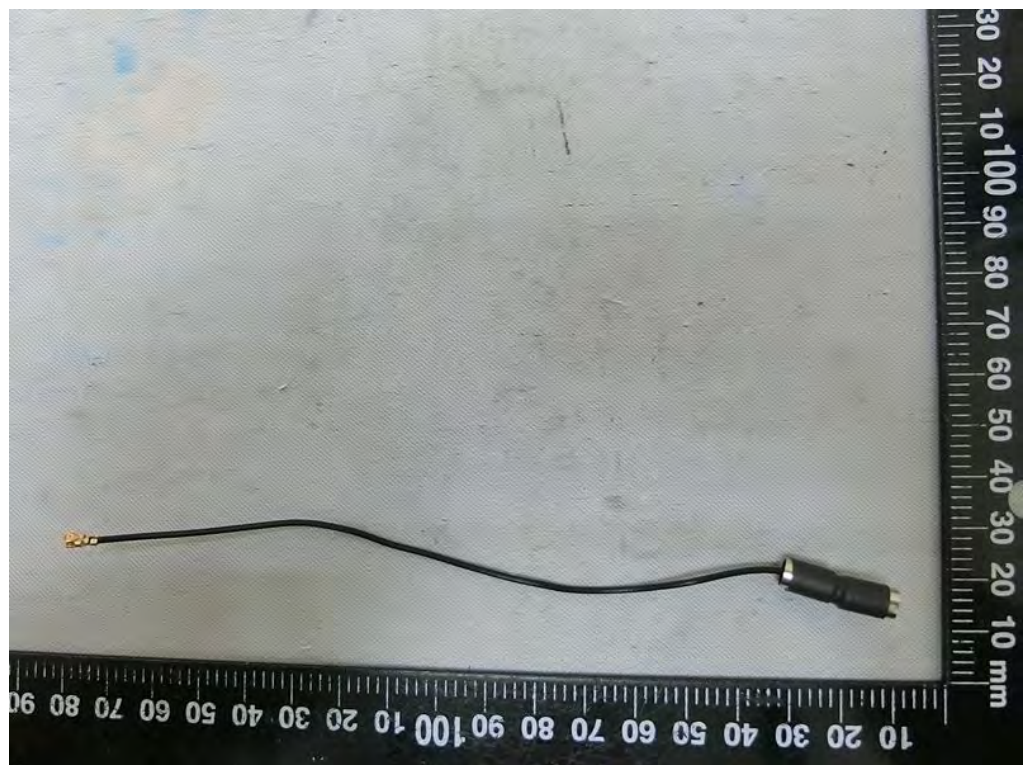
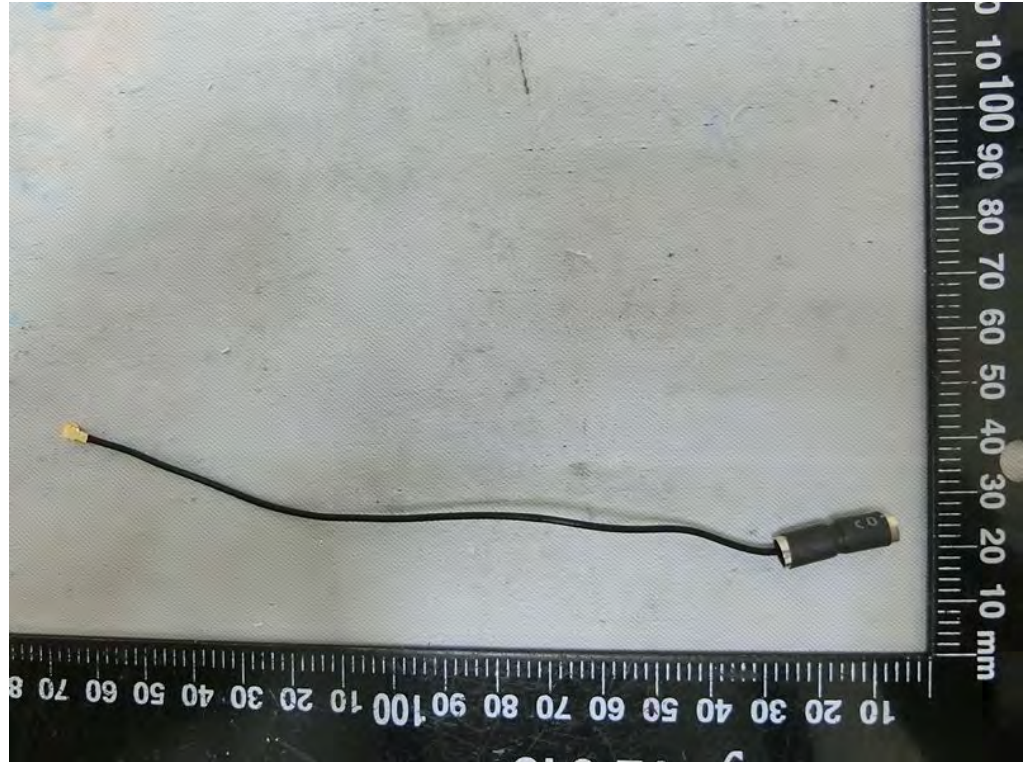


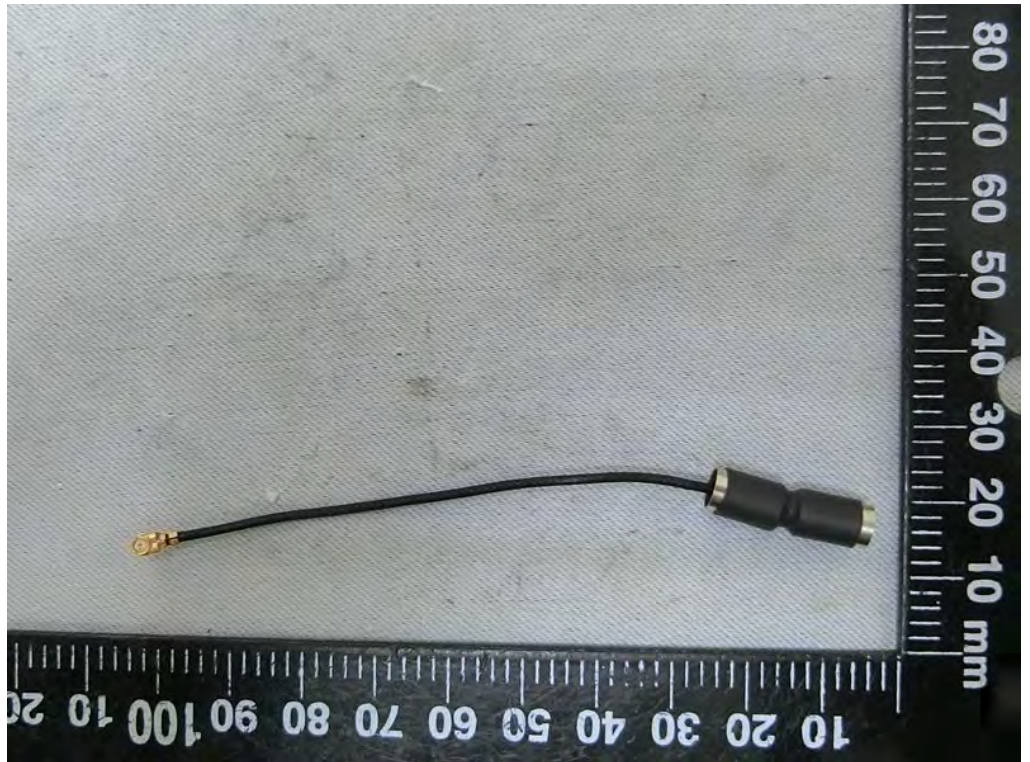


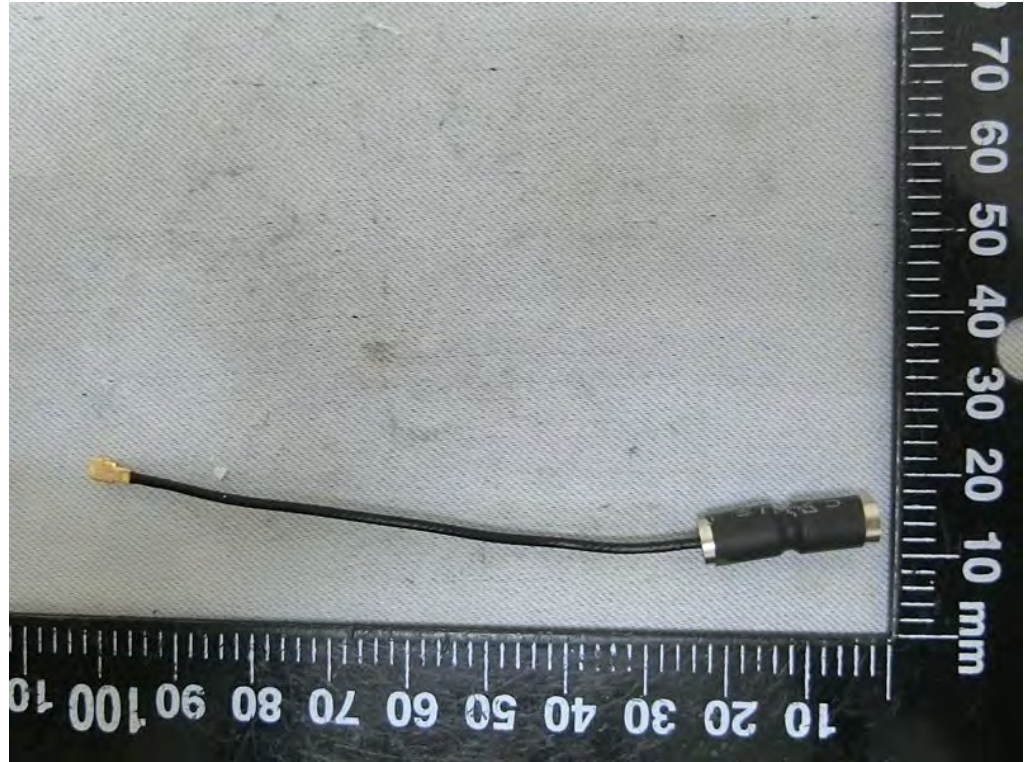


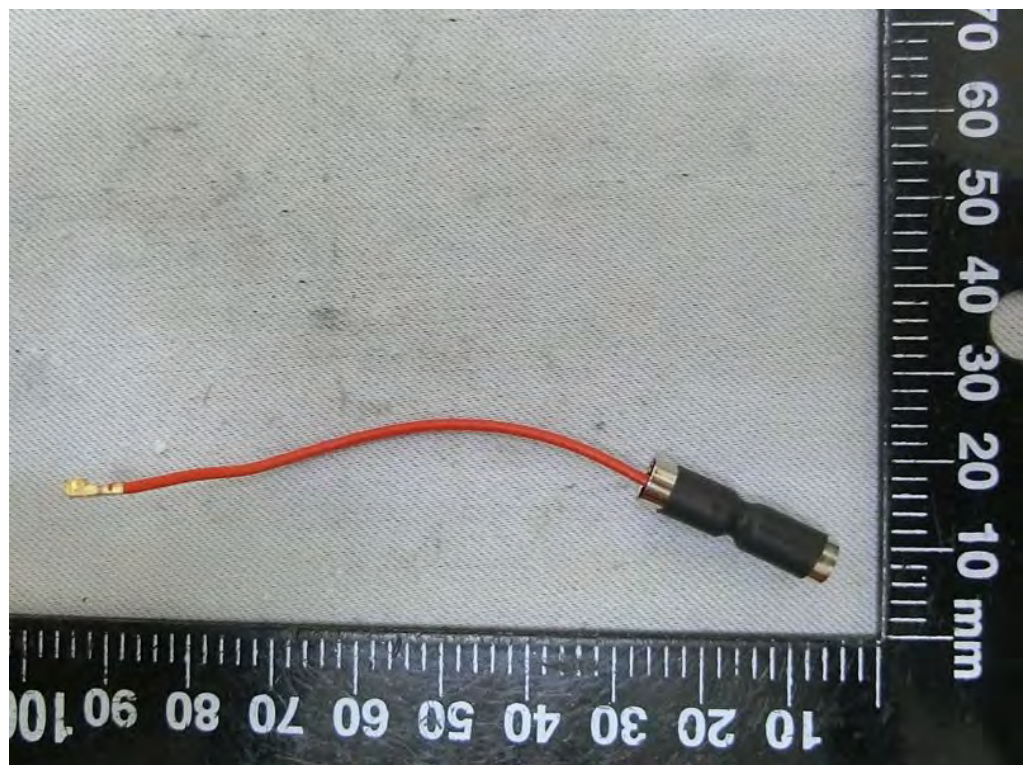
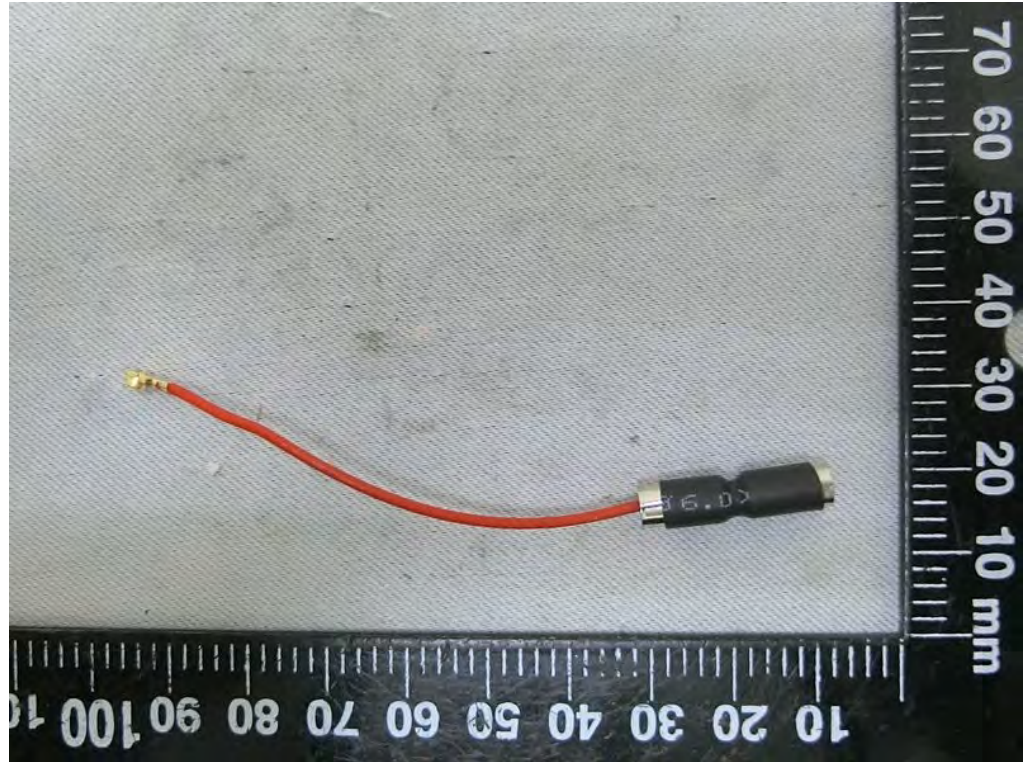




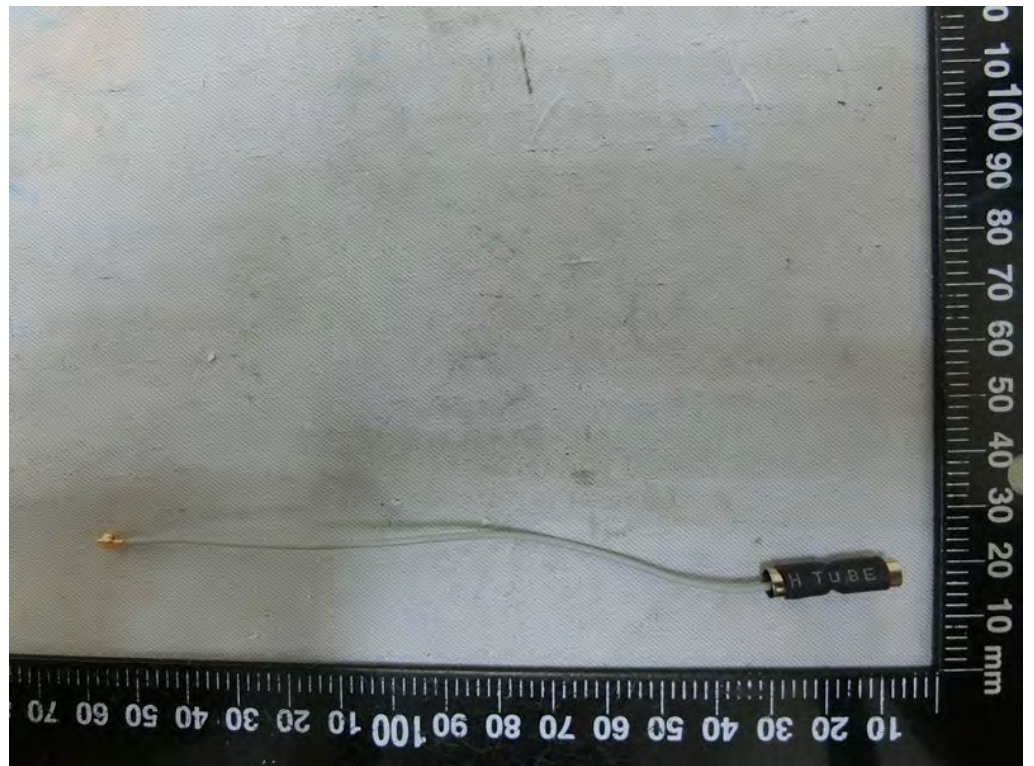


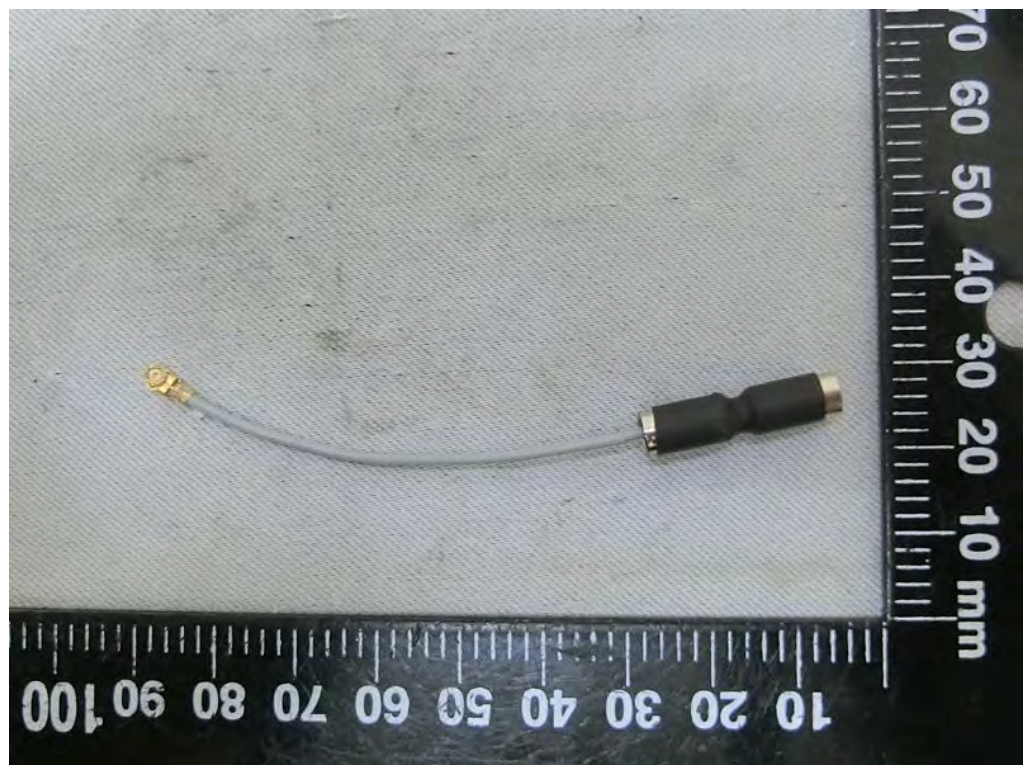
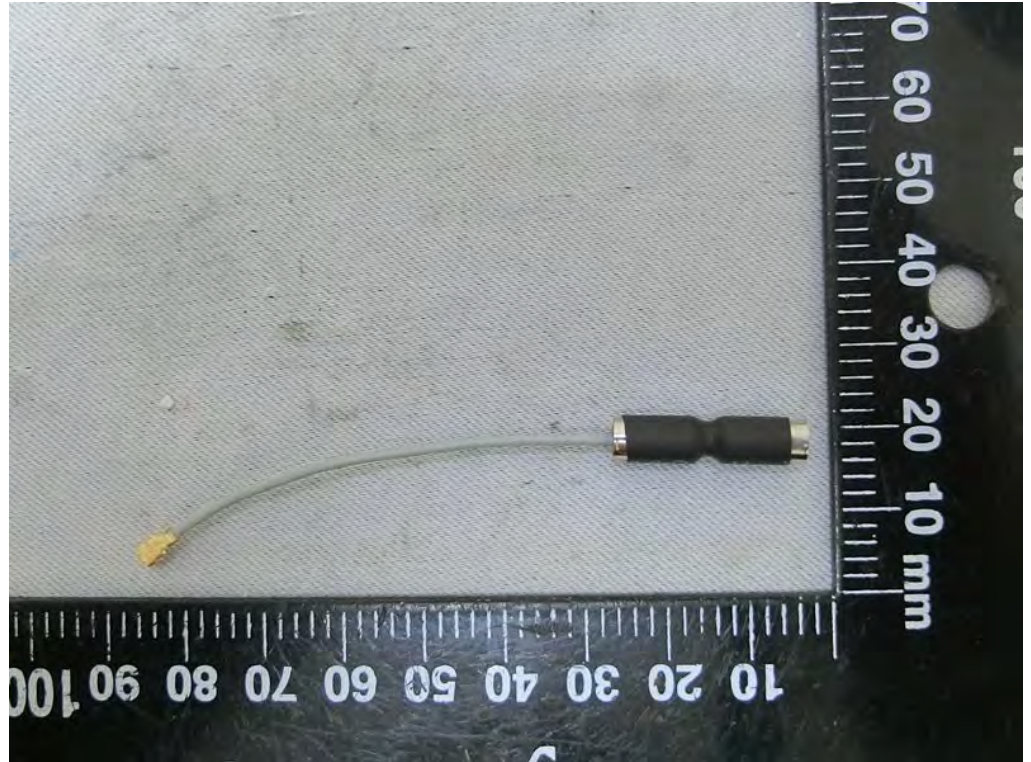




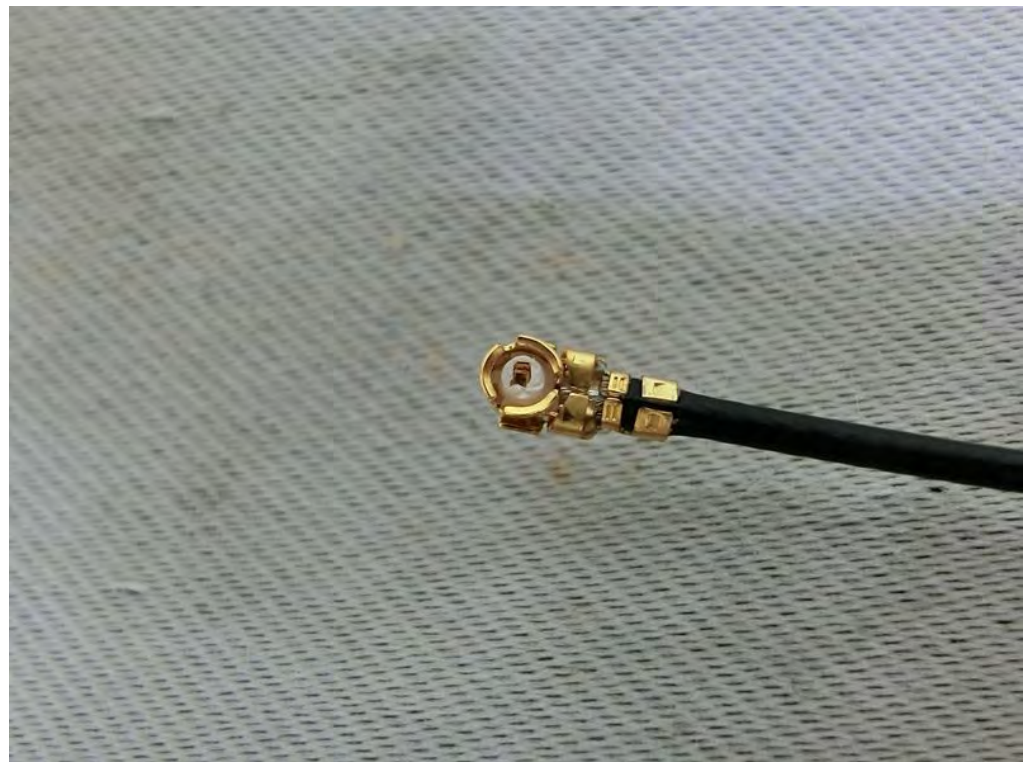
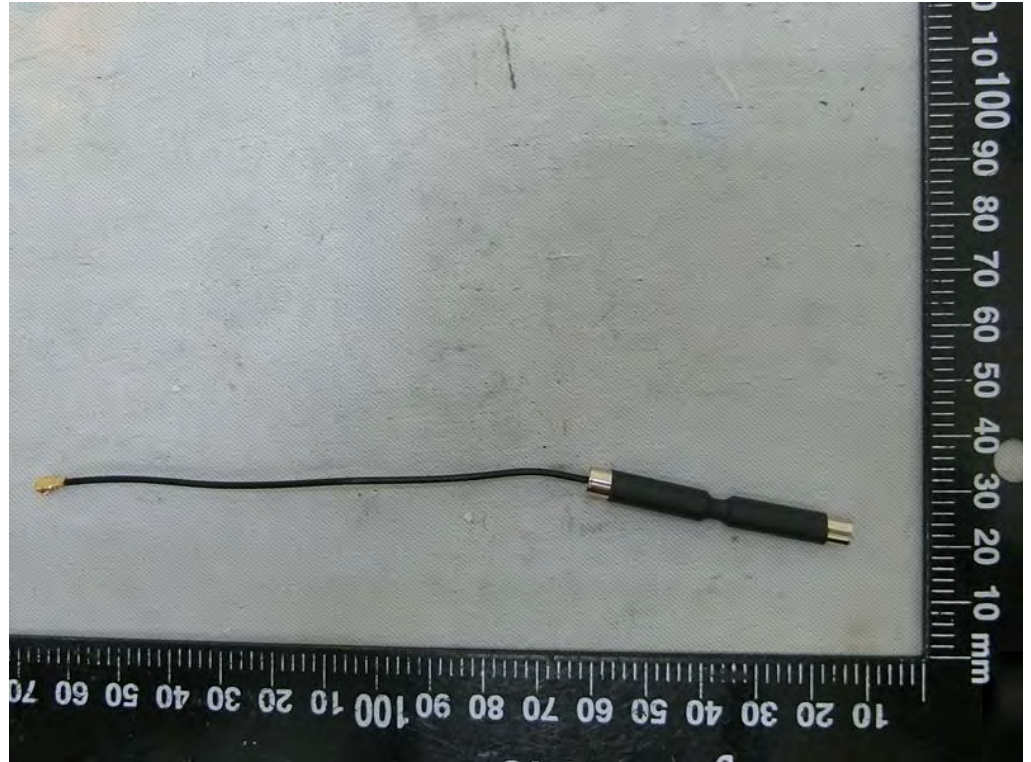


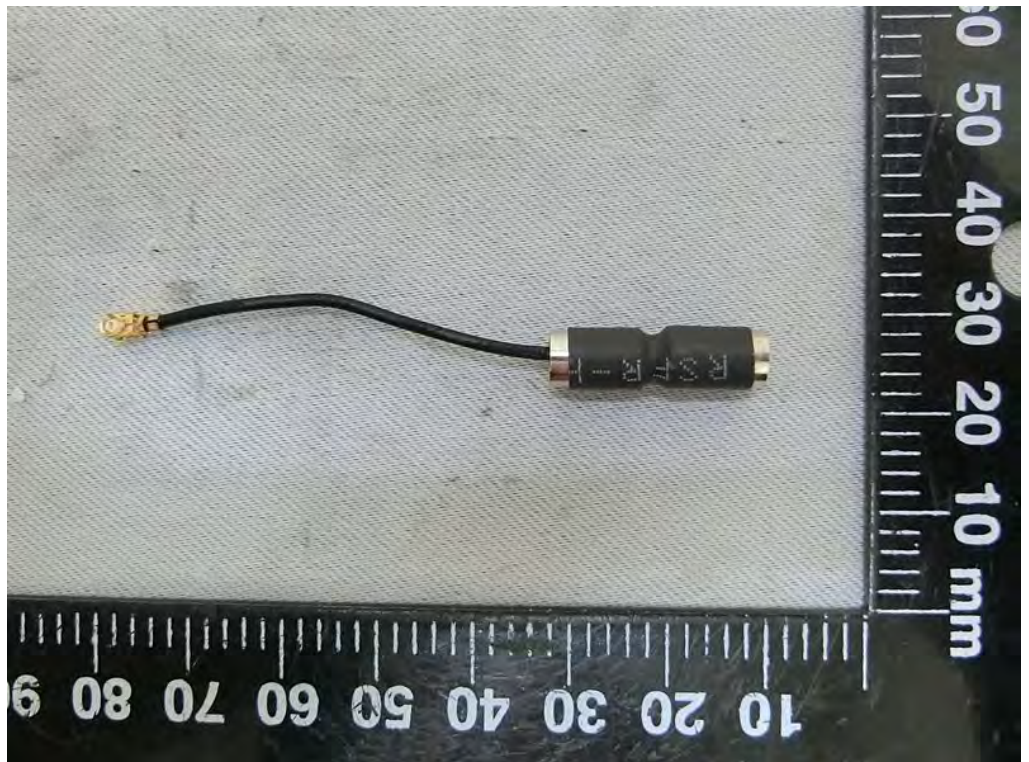
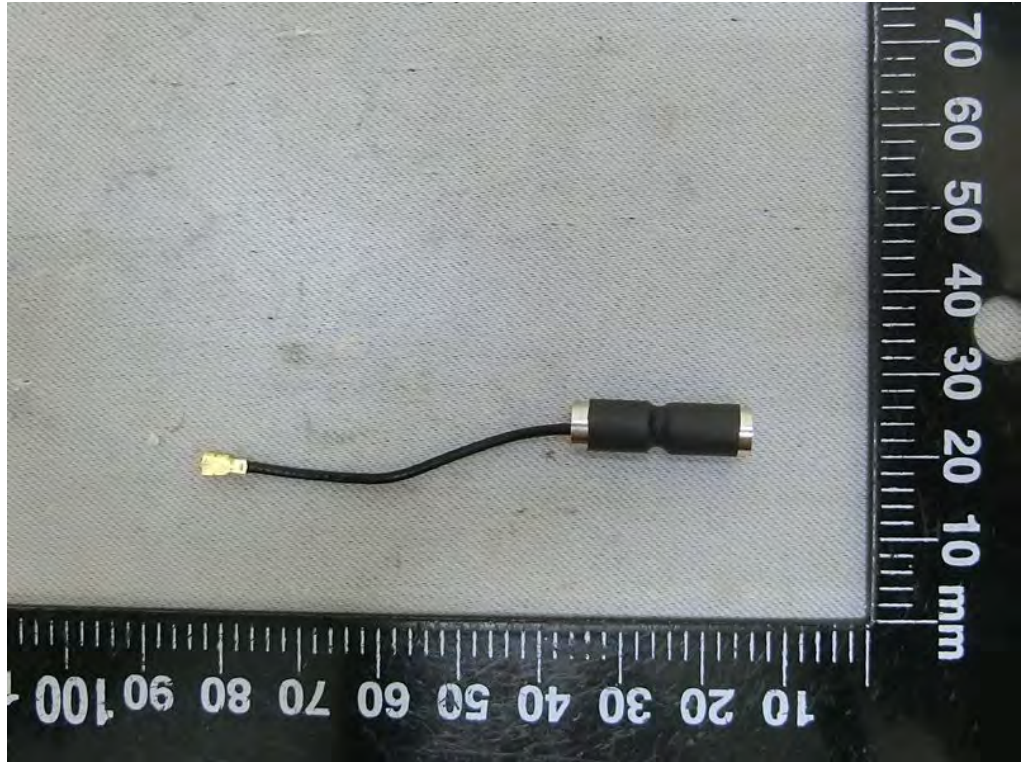


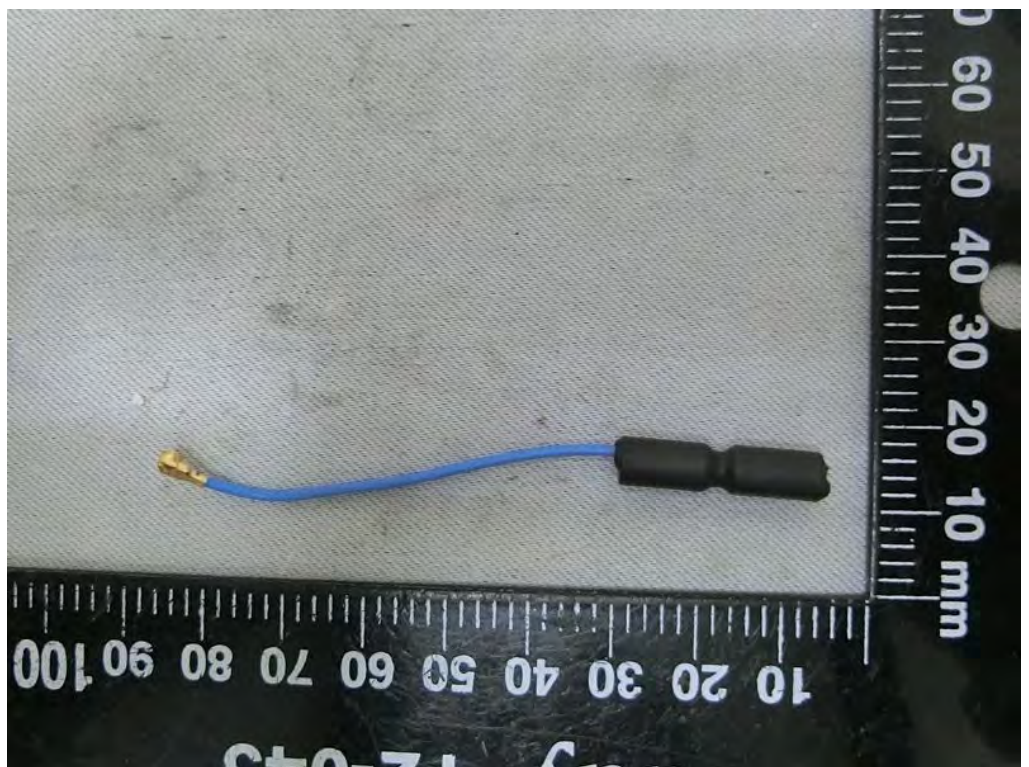


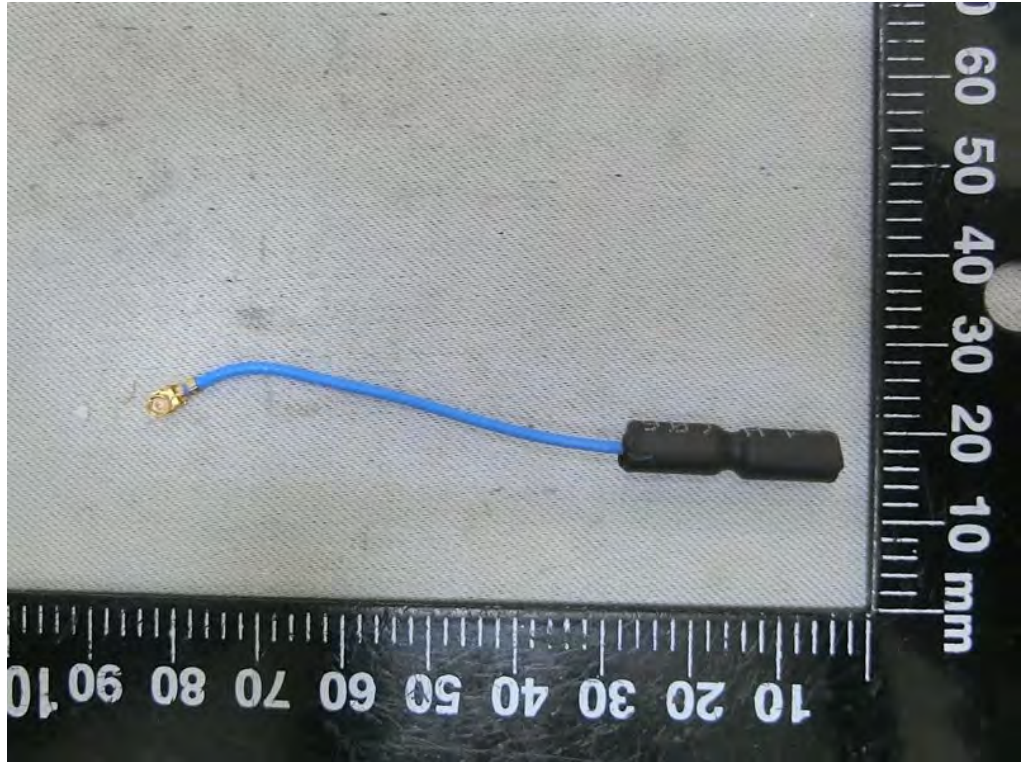












EUT 2

