Section 2.1033(c)(10) - Circuit Diagrams and Descriptions

The top level circuit diagram for the entire system is shown below in Figure 1.

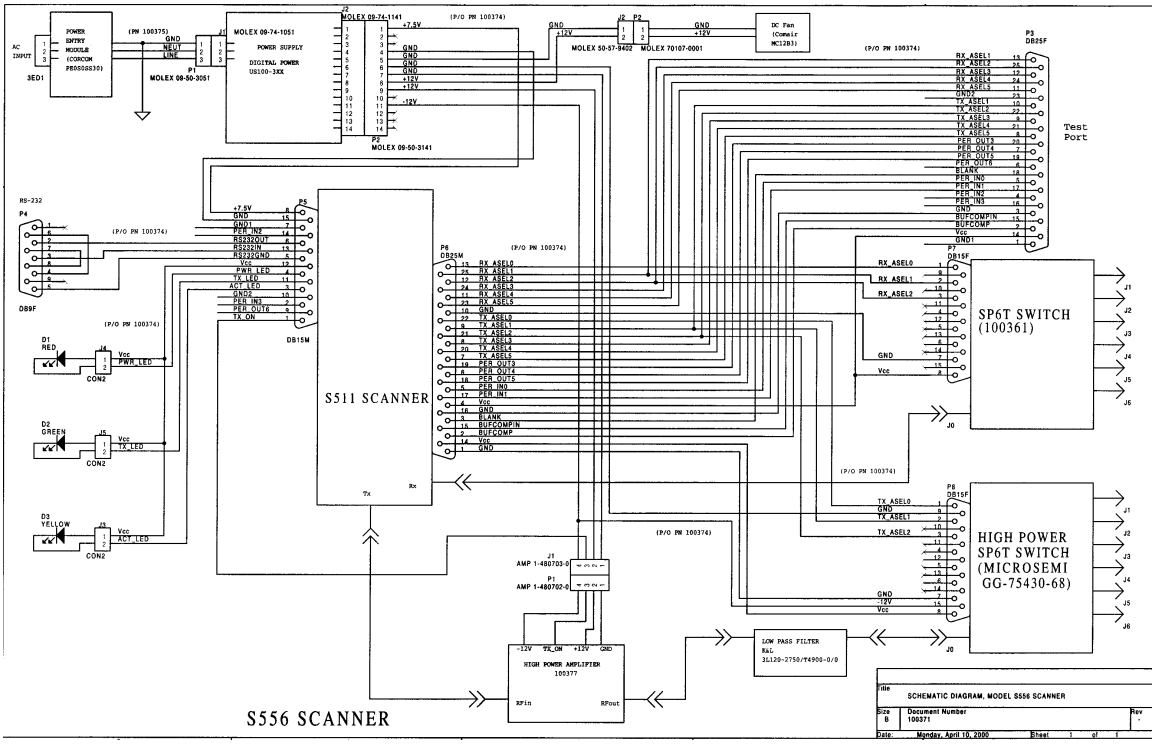


Figure 1. MKRS556 Top Level Schematic Diagram

A. Description of frequency determining circuitry
The RF frequency is generated using a phase locked loop (PLL) circuit. The licensed frequency data is burned into flash memory. At startup the microprocessor sends the PLL integrated circuit (National Semiconductor's LMX2325TM) the serial information for the set frequency. The PLL IC uses a 20 MHz crystal oscillator as a reference frequency. The PLL IC generates a voltage for the voltage controlled oscillator (VCO). The VCO generates the RF signal, which is fed back to the PLL IC. The PLL IC divides this signal down, and compares it to the 20 MHz reference. In the closed control loop, the PLL IC's output voltage is adjusted to precisely maintain the set frequency.

B. Description of circuitry used for spurious, modulation and power limiting
The MKR S556 RF output is on/off modulated. This modulation is accomplished using the analog gain control pin of an RF amplifier (RF Micro Devices RF2126). This gain control is set with a discrete signal from the field programmable gate array (FPGA). An RC filter on this line provides transmission bandwidth limiting. Spurious emissions are limited by a 3 section, low-pass filter located at

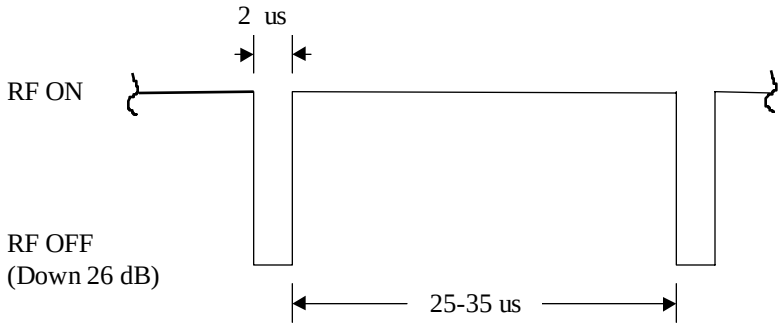
the output of the final RF amplifier. The RF output power level is set using an analog control voltage in the amplification stage prior to the final amplifier. During final assembly, a digital potentiometer is adjusted to provide a desired output power at the RF output port. The digital potentiometer value that corresponds to the desired output power is then burned into flash memory.

C. Description of Modulation technique and circuitry

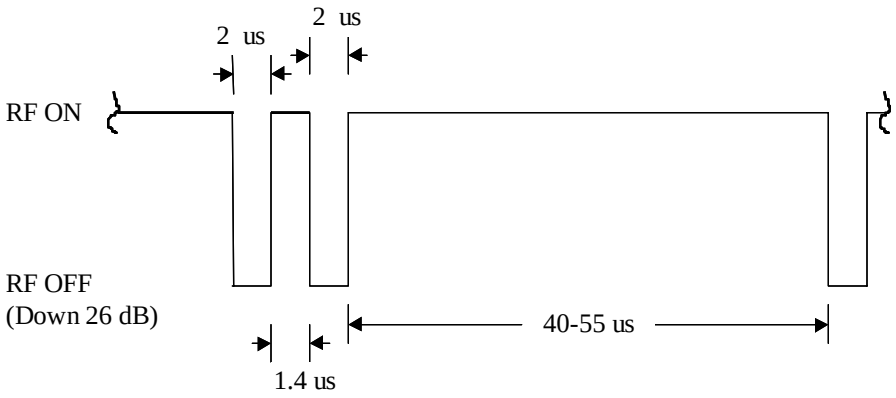
The MKR S556 Transceiver uses an RF on/off modulation scheme. The RF signal powers the ID tag in the field, and then communicates with the tag by briefly turning off the RF power at the proper time. The waveform timing and duty cycle depend on the transmitted symbol. There are 3 transmitter waveforms. The transceiver is either sending just a clock, sending a logic "0", or sending a logic "1". Figure 2 shows the timing for each of these waveforms. The range of time for the next frame of data or clock varies as a function of the interrupt latency of the microprocessor. The modulation either has the RF at full strength in the "on" state, or attenuated by at least 20 dB in the off state. Any time the scanner is normally operating, the RF signal is continuously being modulated. The system is operating CW (unmodulated) only when the transceiver is instructed to operate as such, via operator command. The sequence of clock, logic "0" and logic "1" information being transmitted is completely dependent on the commands issued by the processor, and by the tag responses.

The modulation of the signal is controlled with a digital pulse sequence from the FPGA. This signal is RC filtered to limit the transmission bandwidth, and then is sent to the analog gain control of an RF amplifier. The RF amplifier attenuates the RF signal by a minimum of 20 dB when in the "off" state.

CLOCK ONLY



LOGIC “0” TRANSMITTED



LOGIC “1” TRANSMITTED

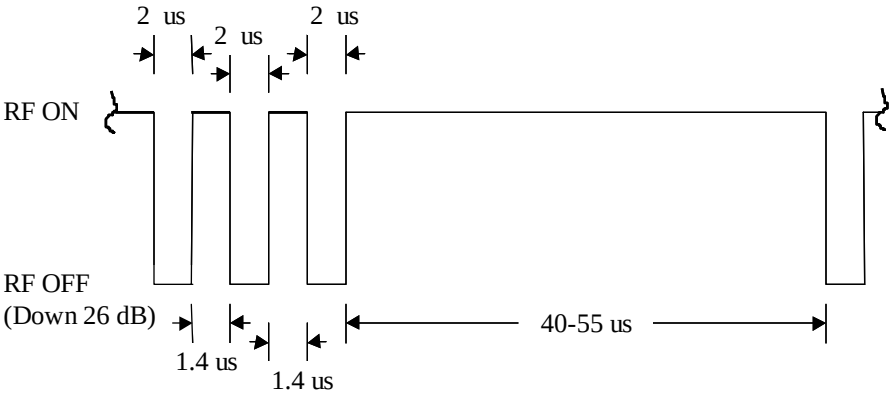


Figure 2. Modulation Modes of the MKRS556 Transceiver