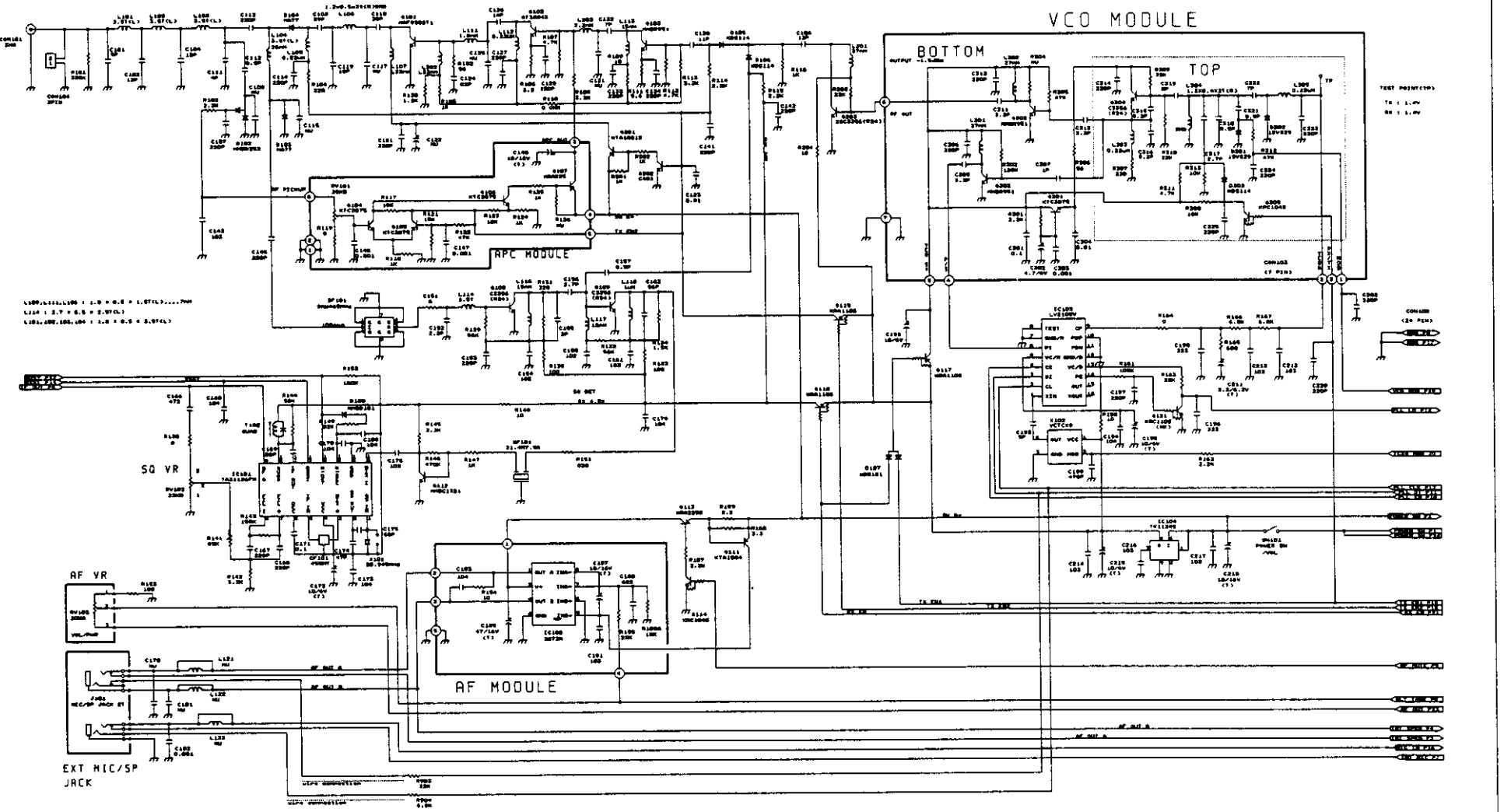
APPENDIX 4

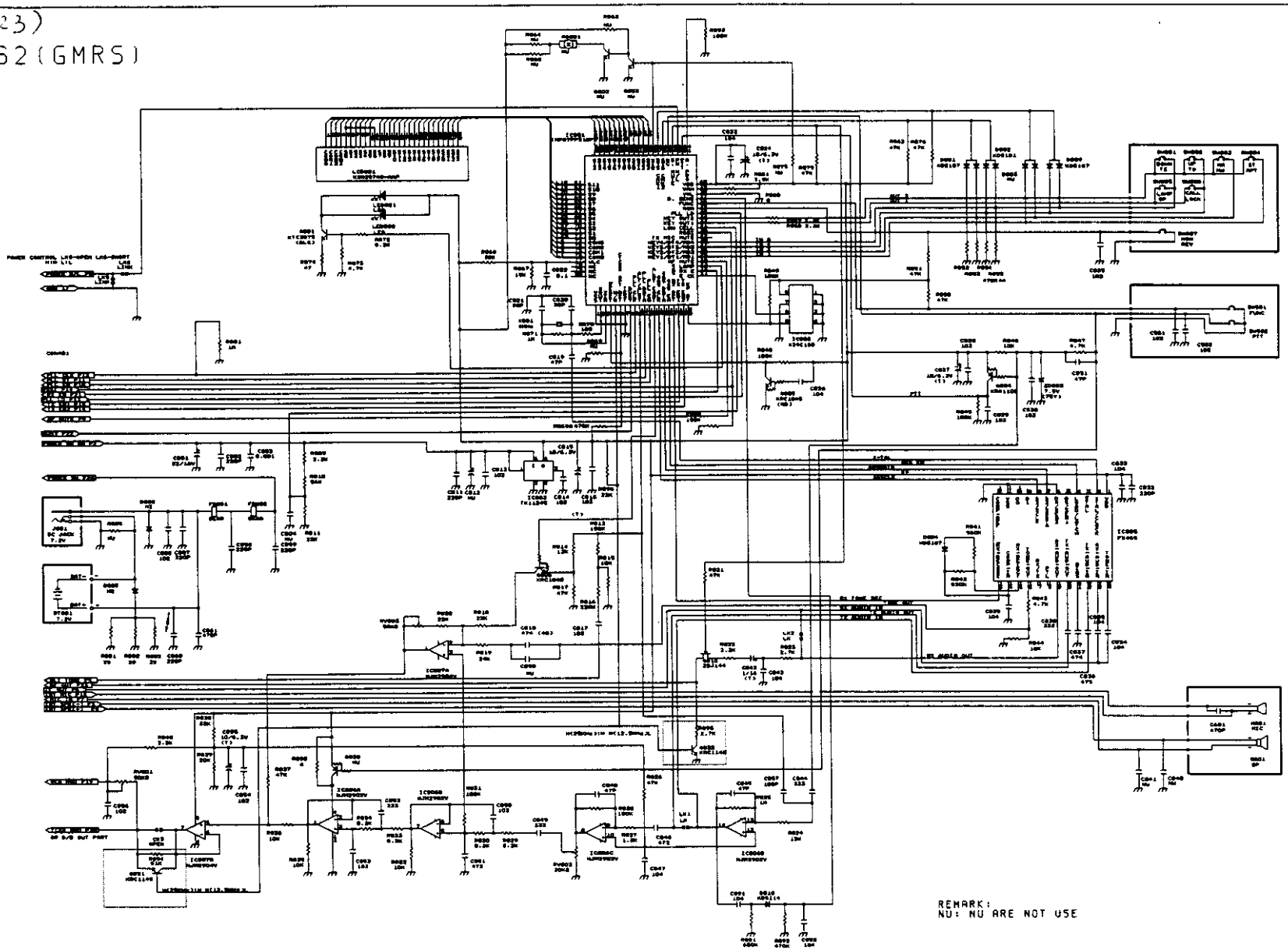
SCHEMATIC DIAGRAMS

TWO (2) SCHEMATIC DIAGRAMS FOLLOWS THIS PAGE

(GR823)
MH-462/462C



(GR823)
MH-462(GMRS)



REMARK:
NU: NU ARE NOT USE

APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

TWO (2) PAGE CIRCUITS & DEVICES TO STABILIZE FREQUENCY
FOLLOWS THIS SHEET

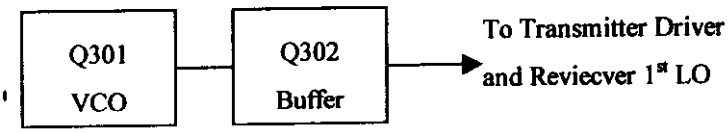
2. DESCRIPTION OF FREQUENCY DETERMINING AND STABILING CIRCUIT

(REFER TO GR-823 (MH462) BLOCK DIAGRAM)

2.1 INTRODUCTION

THE FREQUENCIES FOR TRANSMITTER AND RECEIVER LOCAL FREQUENCIES ARE ALL DERIVED FROM A SINGLE 12.8 [MHz] CRYSTAL BY MEANS OF PHASE LOCKED LOOP.THE RECEIVER FIRST LOCAL OSCILLATOR FREQUENCIES ARE 441.150 [MHz] TO 441.325 [MHz].THE SECOND LOCAL FREQUENCY IS FIXED AT 20.945 [MHz].TO GENERATE SECOND IF 455 [KHz].

DURING TRANSMIT, THE VCO OF THE PLL OPERATES 462.550 [MHz] TO 467.725[MHz].



441.150 MHz to 441.325 MHz (Rx)

462.550 MHz to 467.725 MHz (Tx)

THE VCO OPERATING FREQUENCY DURING RECEIVE IS 441.150 [MHz] TO 441.325 [MHz] THE FREQUENCY IS, INJECTED THROUGH THE BUFFER AMP Q302 INTO THE FIRST LO MIXER Q109

2.2 DESCRIPTIONS OF EACH BLOCK

(1) INTRODUCTION

THE SYNTHESIZER CIRCUIT CONSISTS OF THE FOLLOWING COMPONENTS : PLL IC (IC103), VCTCXO (X102), VCO, VARICAP DIODE (D302)

IC103 IS A CMOS LSI THAT INCLUDES A PRESCALLER.

Q304, D302, C322, 318, 317, 319, L304 FORMED A CLAPP OSCILLATOR CIRCUIT TO OPERATE AS THE VCO FOR IC103.

Q305 IS A SWITCHING TRANSISTOR TO CONNECT OR DISCONNECT THE TUNING CAPACITOR IN THE VCO OSCILLATOR TANK CIRCUIT FOR TRANSMIT OR RECEIVE OPERATION.

Q303 WORKS AS A BUFFER AMP FOR RX LOCAL OSCILLATOR FREQUENCIES AND TX CARRIER FREQUENCIES.

(2) REFERENCE FREQUENCY

THE VOLTAGE CONTROLLED TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR, VCTCXO X102(12.80 [MHz]) AND OTHER COMPONENTS AT PIN.1 AND 16 OF IC103 PROVIDES THE REFERENCE FREQUENCY FOR THE PLL.

(3) VCO

Q304 AND SURROUNDING PARTS FORM A CLAPP OSCILLATOR VCO FOR IC103. WITH APPROPRIATE CONTROL VOLTAGE ON D302, THE VCO CAN OPERATE OVER THE REQUIRED RANGE OF 441.150 [MHz] TO 467.725 [MHz].

(4) PROGRAMMABLE DIVIDER AND ITS CONTROL

THE CHANNEL INFORMATION ARE MASK PROGRAMMED INTO THE CPU IC801. WHEN THE FRONT PANEL CHANNEL UP/DOWN KEYS ARE OPERATED, KEY MATRIX INPUT PINS 25 AND 28 ARE ASSERTED, THE CPU WOULD CONVERT THE SELECTION INTO APPROPRIATE DIVISION RATIO CODES. THE CODES ARE SENT SERIALLY TO THE.THE PROGRAMMABLE DIVIDER OF THE PLL IC301 FOR GENERATION OF THE CORRECT CHANNEL FREQUENCIES.

AS THE PLL/VCO OUTPUT FREQUENCIES ARE DIFFERENT BETWEEN TRANSMIT AND RECEIVE OPERATION, THE CPU SENSES PTT STATUS THROUGH PIN 42. A DIGITAL HIGH AT PIN 4 INDICATES THE RADIO IS IN TRANSMIT MODE.

THE VCO FREQUENCY IS DIVIDED WITH THE CPU CONTROLLED DIVISION RATIO IN IC103. IT IS THEN FED TO THE PHASE DETECTOR FOR COMPARING AND PHASE LOCK WITH THE 6.25 KHz SIGNAL DEVRIVED FROM THE 12.8MHz REFERENCE FREQUENCY.

(5) PHASE DETECTOR AND VCO CONTROL

THE PHASE DETECTOR IS A DIGITAL PHASE COMPARATOR WHICH COMPARES THE PHASE OF THE REFERENCE SIGNAL WITH PROGRAMMABLE DIVIDER. THE DETECTOR OUTPUT IS A SERIES OF PULSES WHOSE WIDTH DEPENDS ON THE PHASE ERROR BETWEEN THE TWO SIGNALS. THE PHASE DETECTOR PULSE OUTPUT IS FED TO AN ACTIVE LOW PASS FILTER TO CONVERT THE PULSES INTO DC VOLTAGE LEVELS WHICH DRIVES THE VARICAP DIODE D302 TO CONTROL THE VCO FREQUENCY.

(6) TRANSMITTER / RECEIVER BUFFER AMP

OUTPUT SIGNAL FROM VCO Q304 IS FED INTO THE BUFFER AMPLIFIERS - Q302 TO DRIVE TX RF POWER AMPLIFIERS AND THE RECEIVER 1'st LO MIXER, AND Q303 TO DRIVE THE PLL PHASE DETECTOR.

(7) SWITCHING OF TUNING CAPACITOR IN VCO

THE VCO CIRCUIT MUST TUNE WITH A WIDE RANGE OF FREQUENCIES 462.550- 467.725 [MHz] FOR TRANSMIT AND 441.150 – 441.325 [MHz] FOR RECEIVE. ADDITIONAL TUNING CAPACITOR IS SWITCHED INTO THE VCO CIRCUIT FOR RECEIVE OPERATION.

THE TUNING CIRCUIT CONSISTS OF D302, C322, C321, C318, C317, L304, C319, Q304, C315. DURING RECEIVE, Q305 CONDUCTS AND SWITCHED C317 INTO VCO TUNING CIRCUIT WITH D303. DURING TRANSMIT OPERATION, Q305 AND D303 BECOMES TURNED OFF AND SWITCHED C317 OUT OF THE VCO TUNING PATH..

D301 FORMS A FM MODULATOR CIRCUIT CONTROLLED BY TRANSMIT AUDIO LEVEL.

(8) RECEIVER LOCAL OSCILLATOR OUTPUTS

1'st MIXER : THE OUTPUT OF VCO Q302 IS INJECTED TO THE BASE OF THE 1st MIXER Q109 THROUGH DIODE SWITCH D106.

2'nd MIXER : THE SECOND LO IS GENERATED INTERNALLY IN IC101 WITH 20.945 [MHz] CRYSTAL X101. THE FREQUENCY IS MIXED WITH THE 1ST IF AT 21.400MHz IN THE 2ND IF MIXER TO PROVIDE 2'nd IF SIGNAL AT 455 KHz. FM DEMODULATION IS DONE BY QUARDRATURE DETECTOR T102 – ALL WITHIN THE FM IF IC.

APPENDIX 8

CIRCUITS TO SUPPRESS SPURIOUS RADIATION AND LIMIT MODULATION

CIRCUITS TO SUPPRESS SPURIOUS RADIATION AND HARMONICS

The tuning circuit between the output of final amp Q101 and antenna, 4-stage "PI-type" network L101, L102, L103, L106, C101, C102, C104, C111 serves as a spurious radiation suppressor. This network also serves to match the impedance between TX final power amp Q101 and the antenna.

CIRCUITS TO LIMIT MODULATION

Audio signals from microphone and alert tones generated by the CPU are amplified by IC806D. After preemphasis equalizing circuit IC806C, the output goes through two stages of splatter filters IC806A-B to limit the audio bandwidth. The signal is then mixed with CTCSS signals generated by IC805, and then routed to the FM modulator in the VCO.

Maximum CTCSS deviation is set by RV803 for ±300 Hz, and maximum audio deviation is set at ±-4.6 kHz with 1 Khz signal at 20 dB input from the microprophone jack, and CTCSS is set to active.

Q821 controls the output level from IC807B to the VCO with preset the maximum modulation to ±4.6 kHz on 25 kHz bandwidth operation, and reduce modulation level to ±-2.8 kHz on 12.5 kHz bandwidth operation when instructed by the CPU.