Oban50 Main Board SPIN 7 TI USB redriver

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REVISION HISTORY

Rev. 007-25 107-25 **Date** 04/03/2023 **Full Package Release - ECO 23-0944**

Page	Description
28	HWE - 3132. Connect GP1 I2C 3.3V bus to CPLD
29,31,32	HWE - 3210. Fully implement the HPD level shifting issue for all three HPD signals going into the CPLD. Add the 38.3K 0402 resistor to the two output HPD signals (R3683, R3684)and remove rework instructions on the input HPD
31,32	HWE - 3211. Add proper bulk bypass capacitors on all bead isolated power rails for the P1V2 and P3V3 rails to the Lontium LT9611UXC converter chips
31,32	HWE - 3253. Add a transistor as a pass FET to the CEC signal path to each LT9611UXC. Also update the ESD diode connectivity to be at the pins vs after the ferrite bead.
46	HWE - 3234. Correct the alternate OVP circuit. Change the two FET power transistors (Q66, Q67) to a common source arrangement.
29	HWE - 3255. Depopulate D1069 and R3207 as these are duplicates in function relative to page 31.
47.48	Insert a 10 ohm 0201 resistor into the top leg of the feedback path for all switching regulators. This enables the use of the BODE100 for stability measurements
30	HWE - 3268. Change the Firestorm programmed PN for U98 to 2470-87205-002 to use the latest firmware that solves the I2S start/stop issues
29,48	HWE - 3272. Add 10 uF bulk cap to node P1V1_EQ_HDMI_RX_TX . Change ferrite bead FB1114 to 1402-05687-221 for lower DCR. Add 22.1 ohm load resistors (1448-63671-221) to P1V1, P1V2, and P1V2_USB to minimize low load ripple.

Rev. 007-26 107-26 **Date** 04/24/2023 **Schematic and BOM Release - ECO 23-1256**

Page	Description
33	HWE - 3294. Depopulate R3423, R3424, and R3425 from the BOM so that the USB hub port power control remains disabled during HUB reset assertion.

Rev. 007-A 107-A **Date** 07/19/2023 **Schematic and BOM Release - ECO 23-2304**

Page	Description
40	HWE - 3331. Change the load caps on the radio crystal for proper frequency centering - required for regulatory. go to 8.2 pF - 1422-58918-082
26	HWE - 3332. Change the load caps on the Microchip LAN controller crystal for better accuracy. New 5 pF cap 1422-37153-050.

Rev. 007-B 107-B **Date** 10/23/2023 **Schematic and BOM Release - ECO 23-3939**

Page	Description
28	Depopulate the two I2C monitoring resistors (R3681 and R3682) that were added for HWE-3132. The current CPLD image drives these inputs as outputs and causes I2C bus errors.

Rev. 207-25 307-25 **Date** 02/26/2024 **Schematic and BOM Release - ECO 24-0314**

Page	Description
28	Populate the I2C monitor resistors since the TI redriver version requires a new CPLD that will fix the driver conflict issue.
24,25,28	Populate the option to use the TI USB redriver chip (TUSB1044 - U41). The NXP redriver is EOL. The use of the TI redriver requires the Dalmore CPLD image to be upgraded to a minimum of version 0x10. System SW must also be upgraded to know to use the TI redriver and not to expect the NXP redriver

Rev. 207-26 307-26 **Date** 09/09/2024 **Schematic and BOM Release - ECO 24-2843**

Page	Description
42	HWE-3423 - replace the FEM modules with Qorvo parts due to EOL of QTI parts. Also change R2890, R2891, R72, and R2903 from 0 ohms to 10 ohms (0201 resistor)

Release for BOM planning

Variant will select which schematic to populate into the BOM.

SCH DWG
3822-87388-207
SCHEM,PCB,MLB,OBAN 50
ADOC3

DNP
DNP
SCHEM,PCB,MLB,OBAN 50
ADOC3

All variants use the same base pcb, assembly and fab drawing

FAB DWG
1360-87388-007
FAB,PCB,MLB,OBAN 50
ADOC1

ASSY DWG
3202-87388-007
ASSY DWG,PCB,MLB,OBAN 50
ADOC1

Notes:

1) All are capacitors are X5R dielectric in 0201 package unless otherwise specified.
2) All resistors are 1% metal film in 0201 package unless otherwise specified
3) 2202 BOM takes precedent over all notes and indications in this schematic

Z21
XXXXXX
2668-47145-001

Z22
2202-XXXXX-XXX
REV X
2668-61687-003

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Title Page & Change History

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Saturday, September 07, 2024

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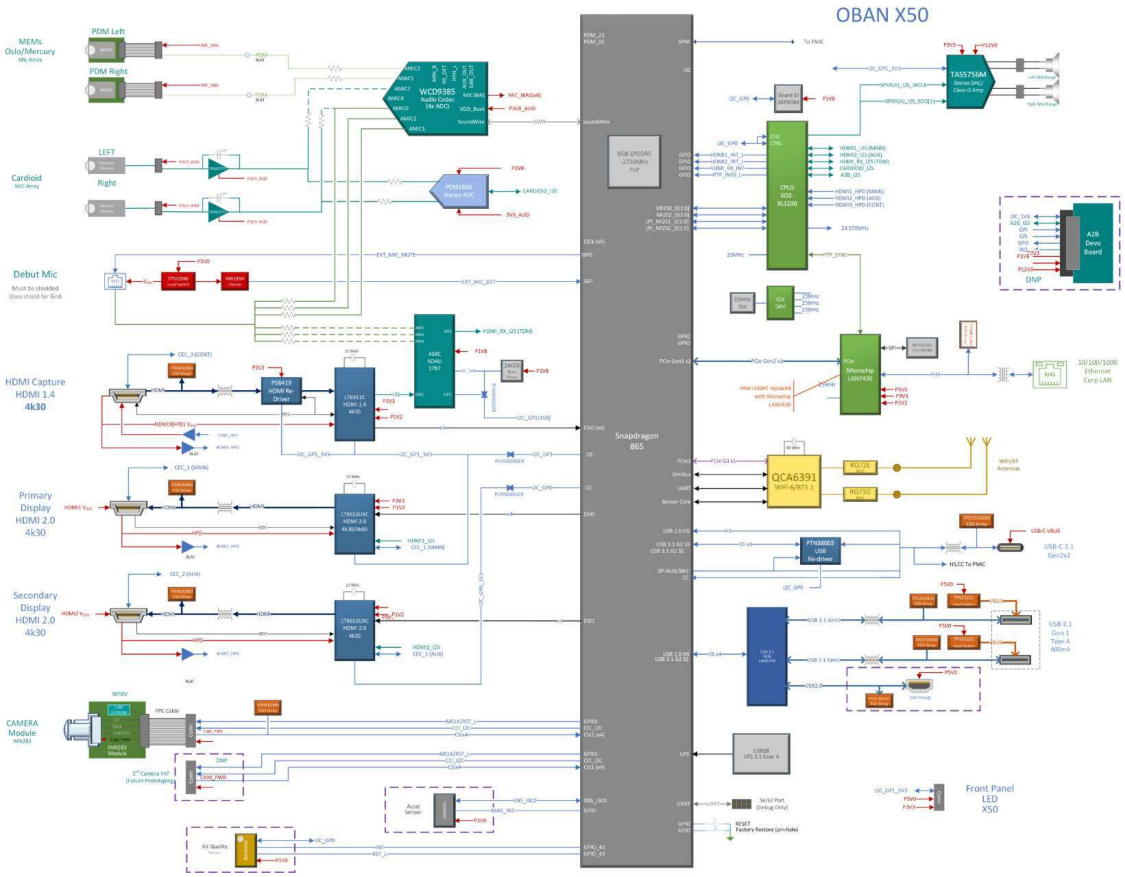

See the OBAN50 HW Architecture Confluence page for a higher quality block diagram

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Block Diagram -

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I2C Devices and (7-bit) Addresses

Bus	Name	Address	Device	RefDes	Comments
CCI I2C 1	CCI_I2C_Sxx1	0x1A 0x50	IMX283 Imager (400kHz) AT24C32D Camera Cal Data EEPROM (400kHz)	U1 (Sensor PCB) U2 (Sensor PCB)	This sensor is for OBAN70 Debug Not present in OBAN50
CCI I2C 2	CCI_I2C_Sxx2	0x1A 0x50	IMX283 Imager (400kHz) AT24C32D Camera Cal Data EEPROM (400kHz)	U1 (Sensor PCB) U2 (Sensor PCB)	
I2C GP0 I2C_GP0 sourced from IBI_I3C_QUP1	I2C_GP0_Sxx	0x40,0x41 0x70 0x32 0x57 0x2B 0x44 0x2D 0x30	CPLD - Flash Configuration Interface CPLD - Register Programming Interface ZMOD4410AI1 CO2 Sensor AT24C02C - System ID PROM (400kHz) LT9611UXC - Main HDMI Out (400kHz) Main LTC9611UXC 8051 USB HUB - USB5744 PTN38003AEAV - USB Type-C Re-Driver	U94 U94 U36 U20 U100 U100 U2076 U1044	 This has been depricated Undocumented internal uC
I2C GP1 I2C_GP1 sourced from IBI_I3C_QUP0	I2C_GP1_Sxx	0x2B 0x44 0x68 0x6B 0x4C 0x28 0x50 0x4A	LT6911 - HDMI Input (400kHz) Main LTC6911 8051 KTD2061 LED Controller - LEDs 1-12 KTD2060 LED Controller - LEDs 2-24 TAS5756M - Digital Audio Amp ADI ADAU1787 DSP (ASRC) EEPROM for ADI ADAU1787 DSP PCM1860DBTR - Line Audio Input ADC	U95 U95 U1 U4 U37 U96 U98 U1037	 Undocumented internal uC OBAN LED board U+ LED board - proto only Path not enabled
I2C GP2 I2C_GP2 sourced from QUP_U0(15)	I2C_GP2_Sxx	0x3F 0x44 0x43 0x90 - 0xAF	LT9611UXC - Aux HDMI Out (400kHz) Aux LTC9611UXC 8051 FSA4480UCX PS8419QFN46GTR-A1 - HDMI-Redriver	U1001 U1001 U11 U1045	 Undocumented internal uC
I3C SNS 0	SNS_I3C0_Sxx	0x6A	LSM6DSO Accelerometer	U2	Sensor Core I2C0

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Power Sequencing & I2C Addr -

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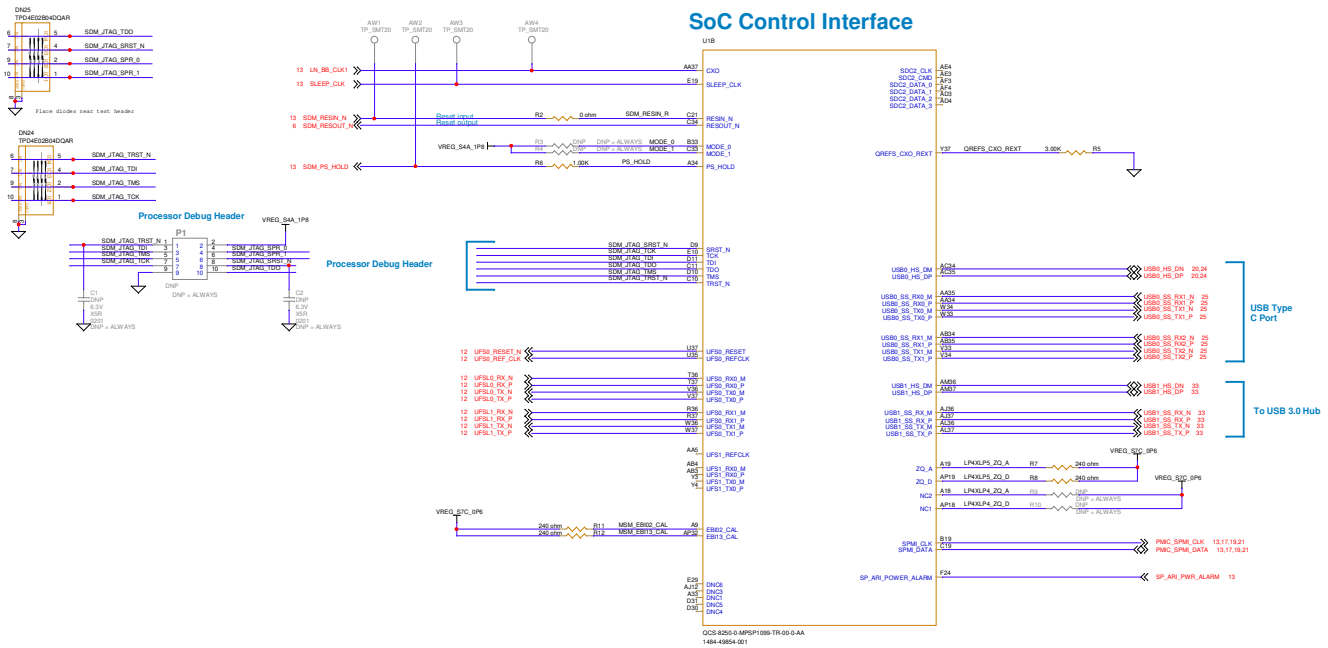
SoC Control Interface



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SM8250 - Control

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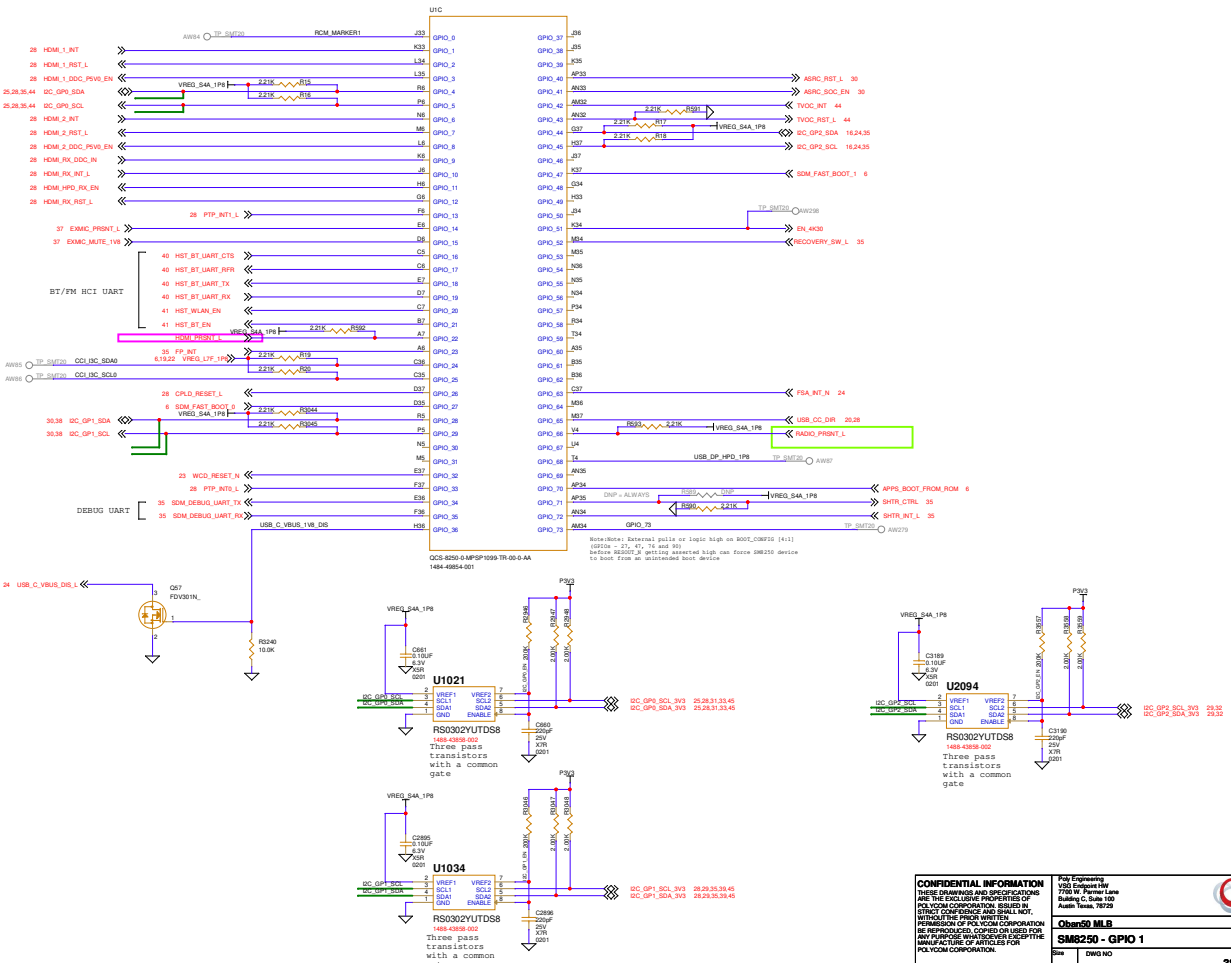
SoC GPIO Block 1



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SM8250 - GPIO 1	-
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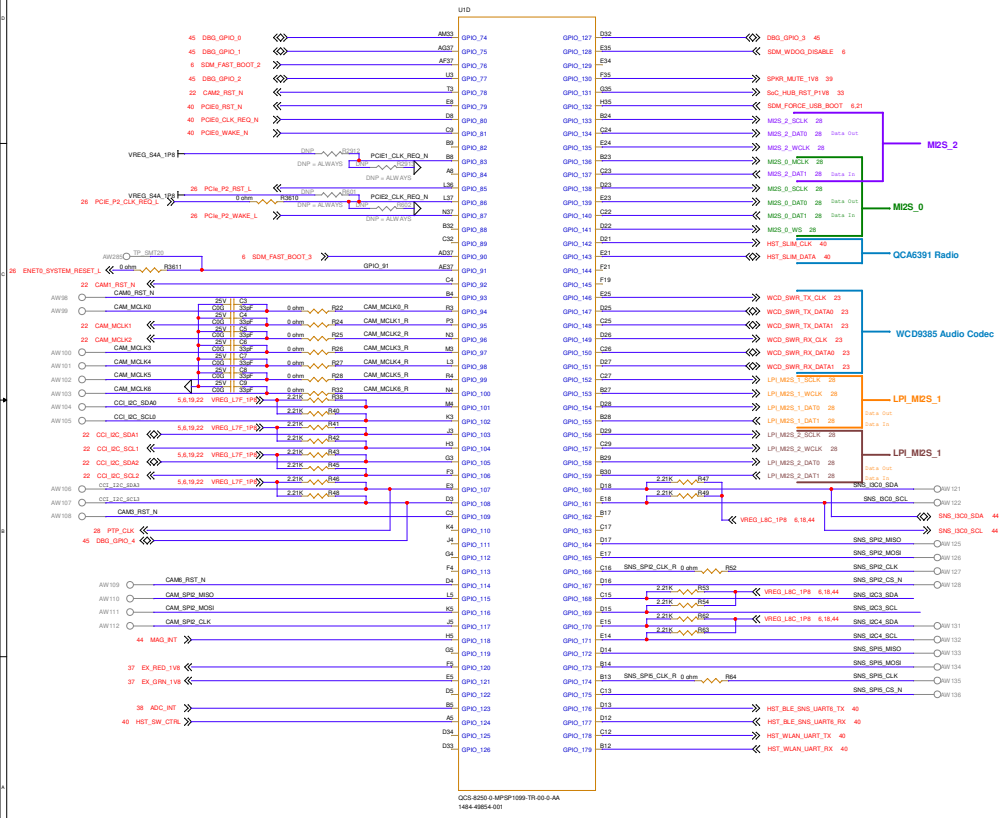
SoC GPIO Block 2

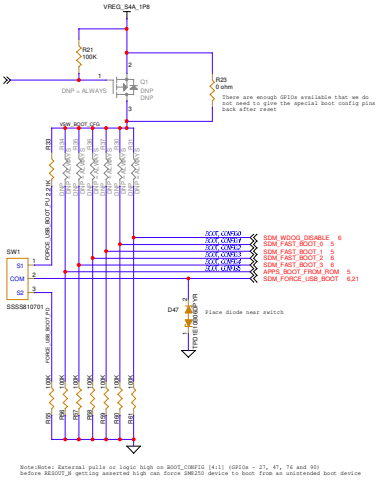


BOOT Option	GPIO_90 BOOT_CONFIG[4] FAST_BOOT[3]	GPIO_76 BOOT_CONFIG[3] FAST_BOOT[2]	GPIO_47 BOOT_CONFIG[2] FAST_BOOT[1]	GPIO_27 BOOT_CONFIG[1] FAST_BOOT[0]
This is the normal boot setting → UFS-HS-G1->3D->USB30->eDL	0	0	0	0
3D->UFS-HS-G1->eDL	0	0	0	1
3D->eDL	0	0	1	0
USB->eDL	0	0	1	1
QPR->eDL	0	1	0	0
SPI->eDL	0	1	0	1
	0	1	1	0
	0	1	1	1

BOOT Option	GPIO 123 BOOT_CONFIG[0] WATCHDOG_DISABLE
This is the normal boot setting → Enabled	0
This is the proto setting → Disabled	1

BOOT Option	GPIO 122 FORCE_USB
This is the QPR setting → Enabled	1
This is the normal boot setting → Disabled	0

BOOT Option	GPIO 122 FORCE_USB
This is the normal boot setting → Enabled	1
Disabled	0



Note:Note: External pulls or logic high on BOOT_CONFIG [4:1] (GPIOs - 27, 47, 76 and 90) before RESOUT_N getting asserted high can force SM8250 device to boot from an unintended boot device

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SM8250 - GPIO 2

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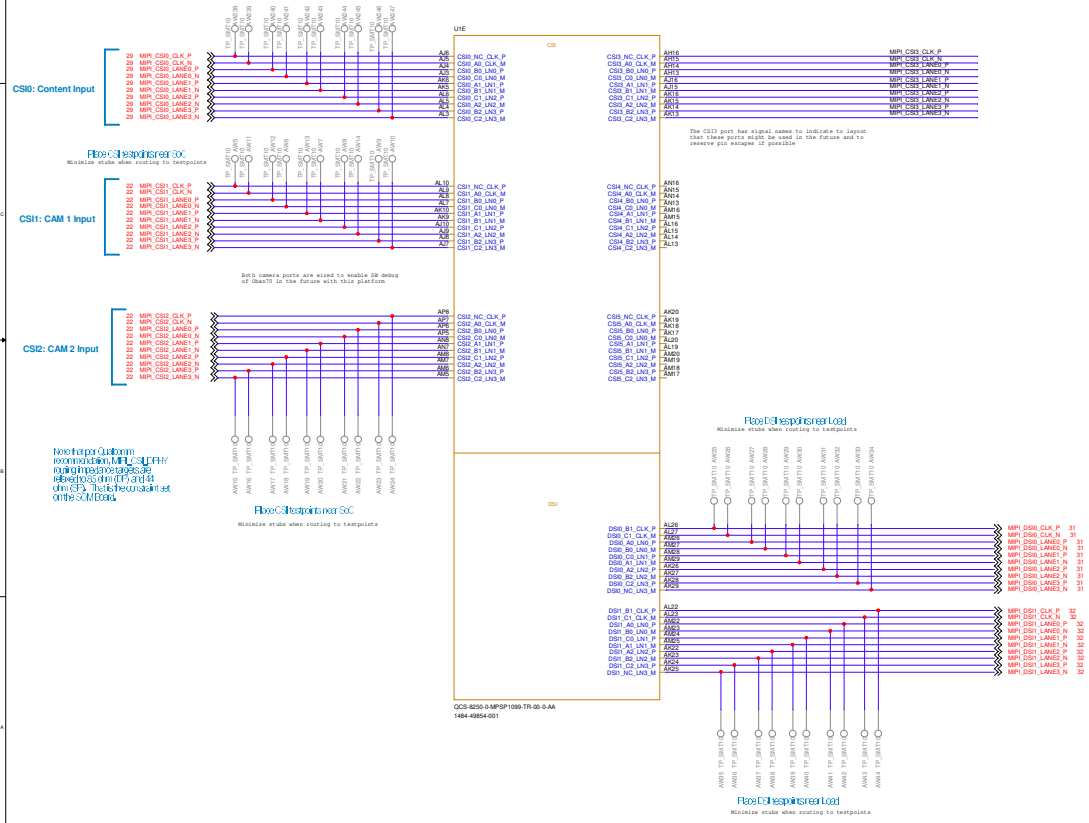
MIPI SoC Interface



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SM8250 - MIPI DSI/CSI

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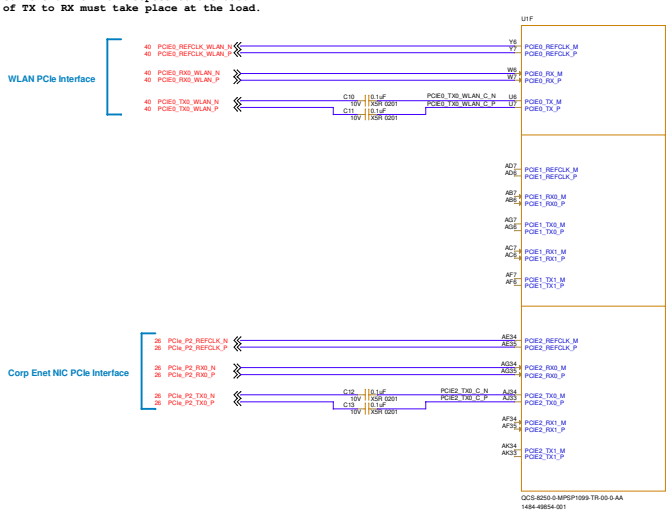
Signal naming convention is with respect to the SoC.
The crossover of TX to RX must take place at the load.



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SM8250 - PCIe Interface -

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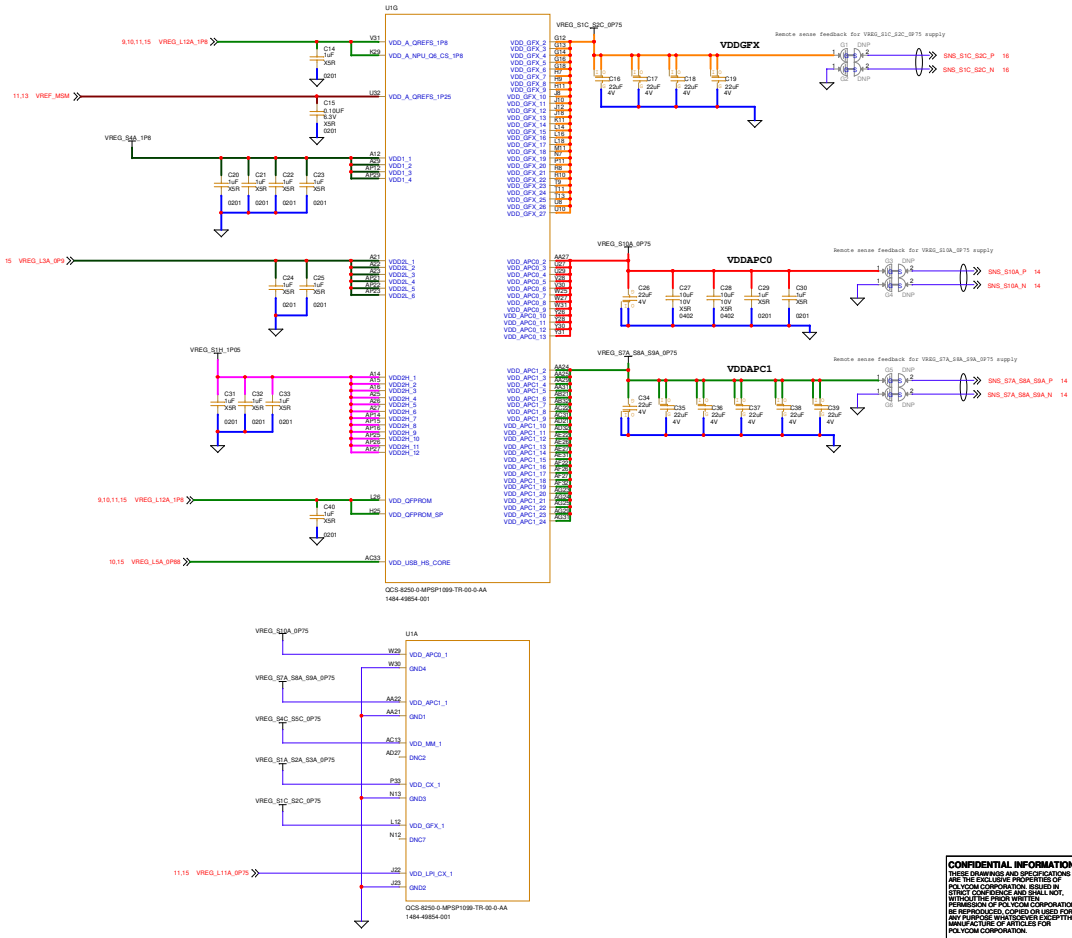

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SM8250 - Power 1

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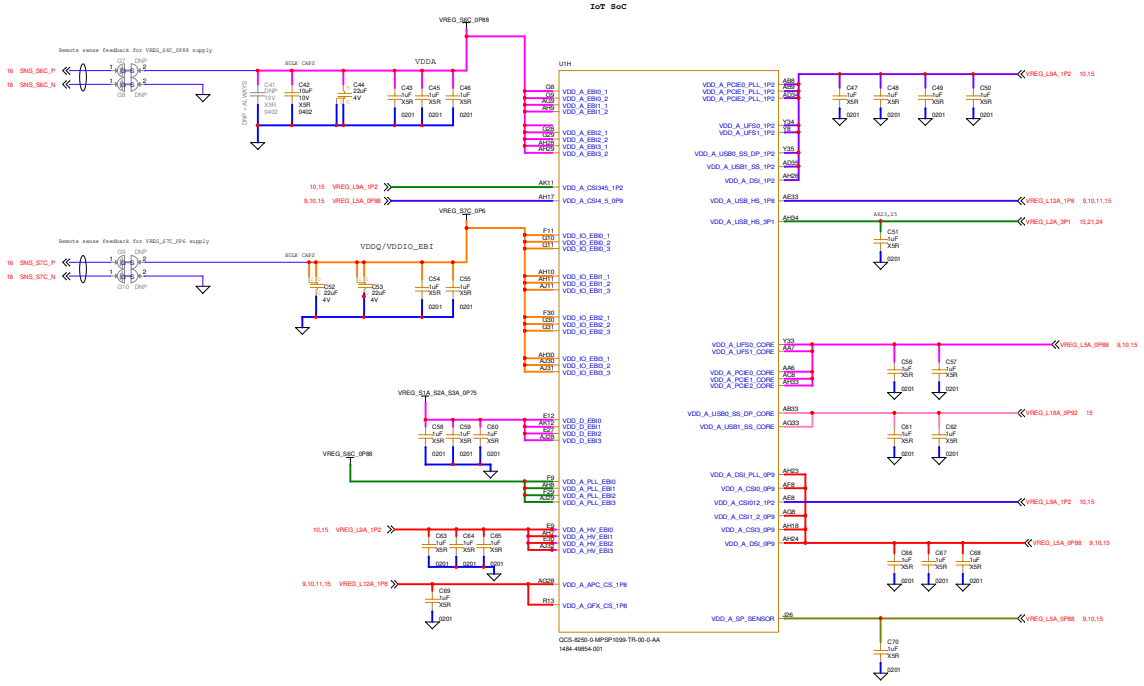
POWER SoC Interface



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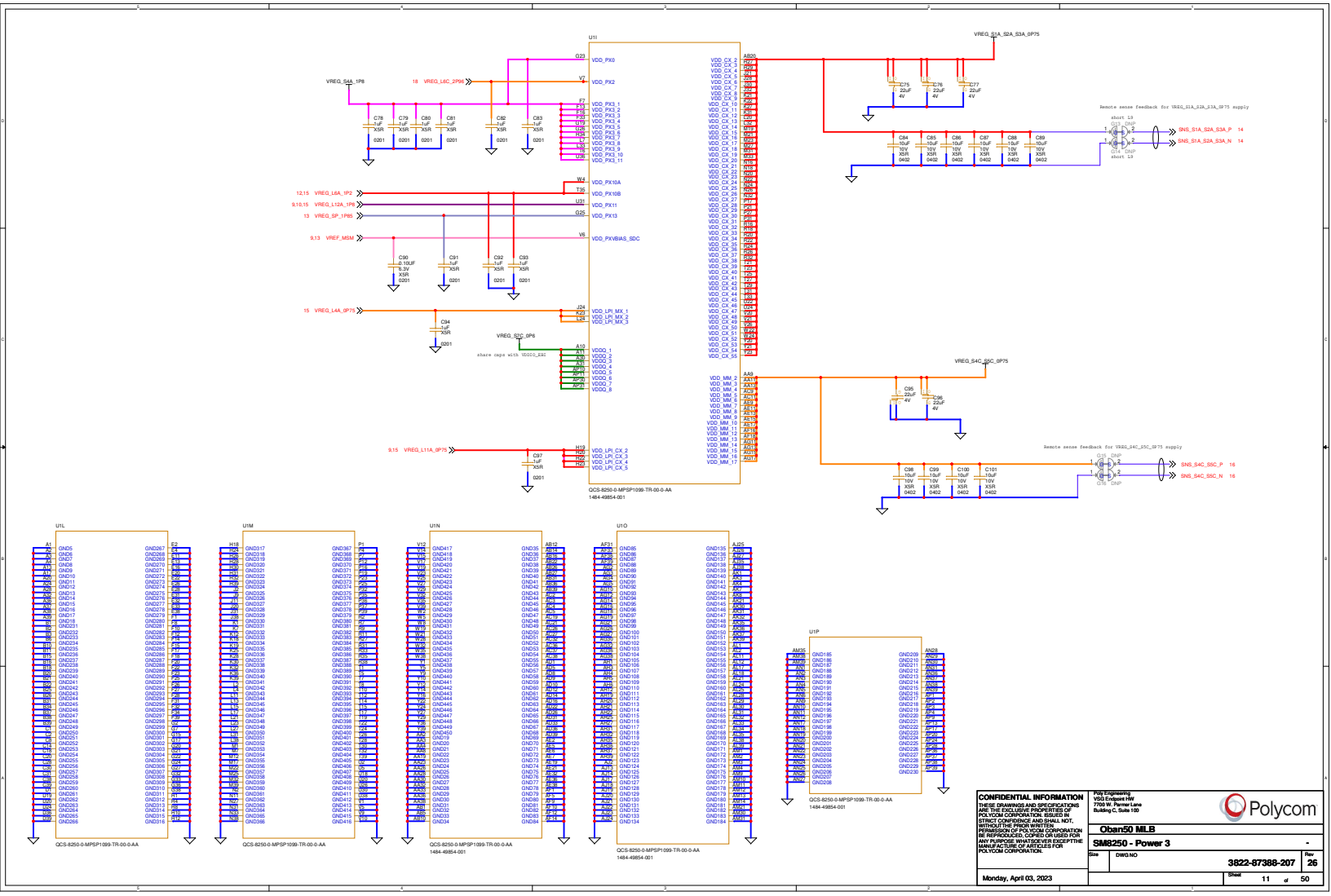

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SM8250 - Power 3

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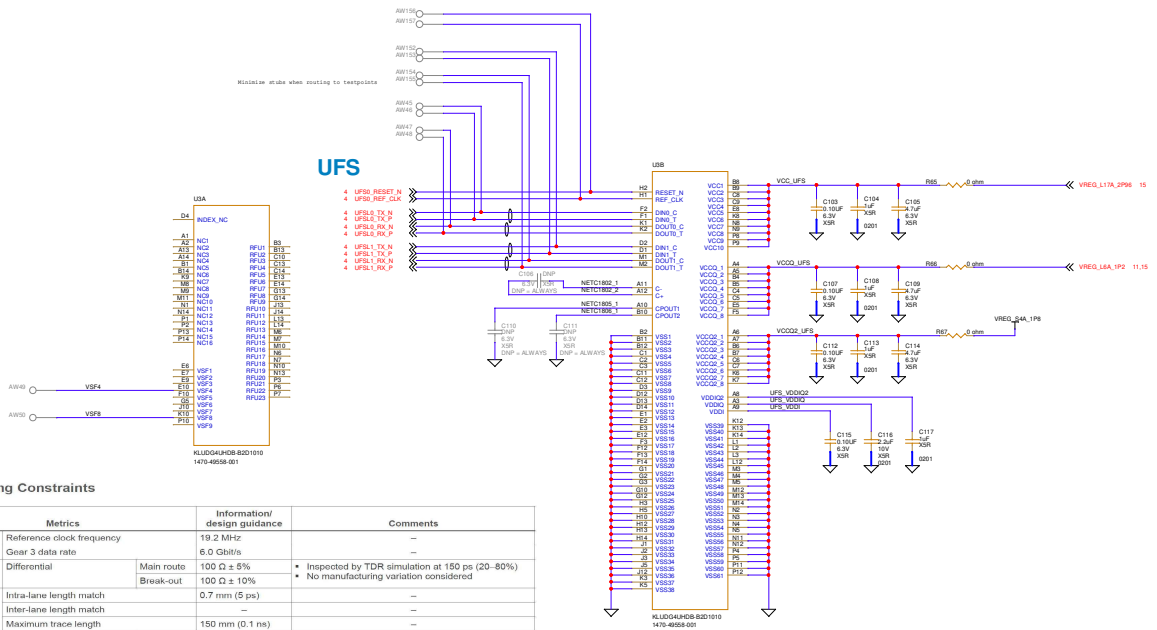

UFS Routing Constraints

Metrics			Information/ design guidance	Comments
General information	Reference clock frequency		19.2 MHz	–
	Gear 3 data rate		6.0 Gbit/s	–
Impedance	Differential	Main route	100 Ω ± 5%	• Inspected by TDR simulation at 150 ps (20–80%) • No manufacturing variation considered
		Break-out	100 Ω ± 10%	
Length match	Intra-lane length match		0.7 mm (5 ps)	–
	Inter-lane length match		–	–
	Maximum trace length		150 mm (0.1 ns)	–
Spacing	Spacing to all other signals	Main route	4 × line width	–
	Spacing data lane-to-lane		3 × line width	–
Isolation	REXT resistor net to adjacent signals		-30 dB	–

LPDDR5

PoP, not on PCB. Instantiated to include in BoM.

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SM8250 - DRAM and UFS

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