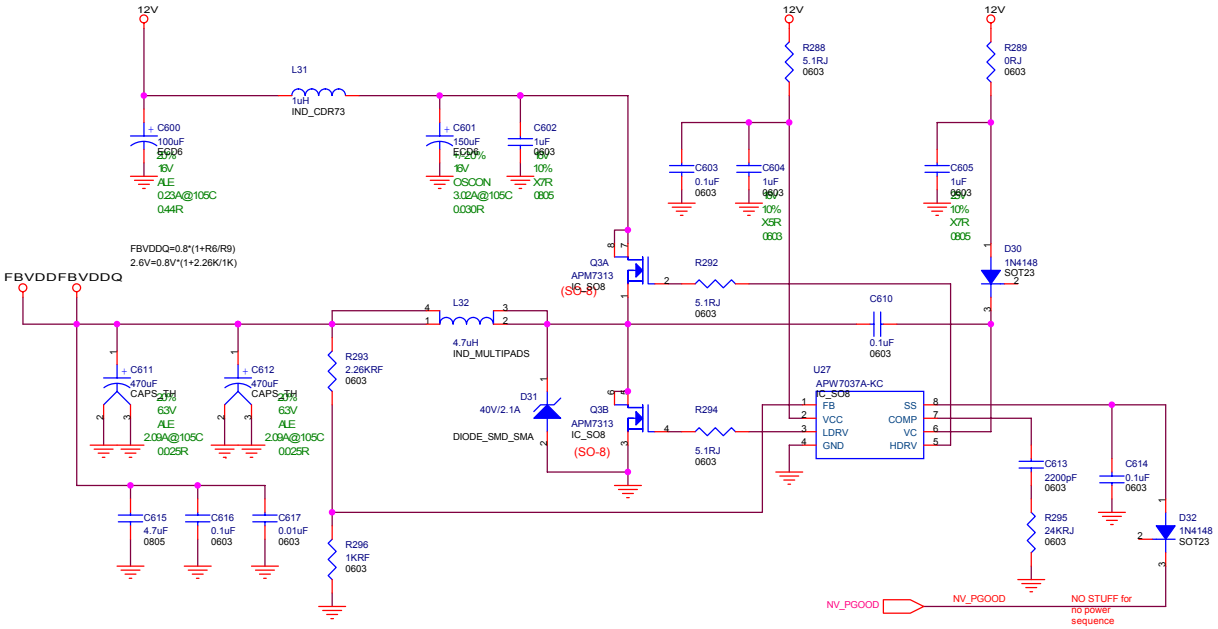
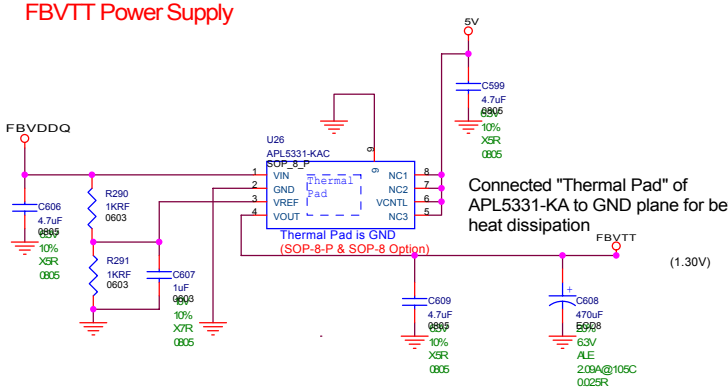
FBVDDQ Power Supply



FBVTT Power Supply



Connected "Thermal Pad" of APL5331-KA to GND plane for better heat dissipation

Note : This circuit is for SOP-8 and SOP-8-P dual layout.
If sop-8 can't priove enough thermal dissipation, you can use sop-8-p package.

FBVTT=FBVDDQ*(R3/(R3+R4))
1.3V=2.6V*(1K(1K+/1K))

SPARKLE SP8836 REVI:C1.1

2003/12/26

8/22/03: P191 was cloned from P193
8/22/03: Page(S) 4,5,7,8) - Changed Memory termination to FBVTT parrallel and added de-coupling caps.
8/26/03: Page(S) 22 - FBVDD(Q) power supply was changed from individual (HIP6012) switchers.
8/26/03: to a dual switcher (ISL6225) that generates FBVDD(Q) and FBVTT.
8/26/03: The Linear Sink/Source that generated FVBTT was also removed.
8/26/03: Page 21 - Added 10K pullup to NV_PGOOD
8/26/03: Page 6 - Added Low pass filter to GPU_VTT
8/27/03: Page 15 - Changed R562 to a 0603 to facilitate routing
8/29/03: Page 21 - Removed C765 and connected U510.12 to U510.17 (NV_SFTSTRT)
9/03/03: Page 21 - Added Schmoo two 10K (NO_STUFF) resistors for NVVDD Schmoo circuit.
9/04/03: Page 21 - Added Silent Running
9/04/08: X-Released
9/18/08: CLoned from P191_A00
9/18/03: Pages 2, 21 - Added two resistors for Droop Compensation
9/18/03: Page 12 - Removed Link-B from design
9/18/03: Page 22 - Added test point for FBVTT

PAGE SUMMARY:

SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	602-10191-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	600101910000000	602-10191-0000-000	NV36 VGA/DVI 400/300 128MB 16Mx16 VGA/VIP/DVI
2	600101910001000	602-10191-0001-000	NV36 VGA/DVI 400/300 128MB 16Mx16 VGA/VIP/DVI
3	600101910000100	602-10191-0000-100	NV36 VGA/DVI 400/300 128MB 16Mx16 VGA/VIP/DVI
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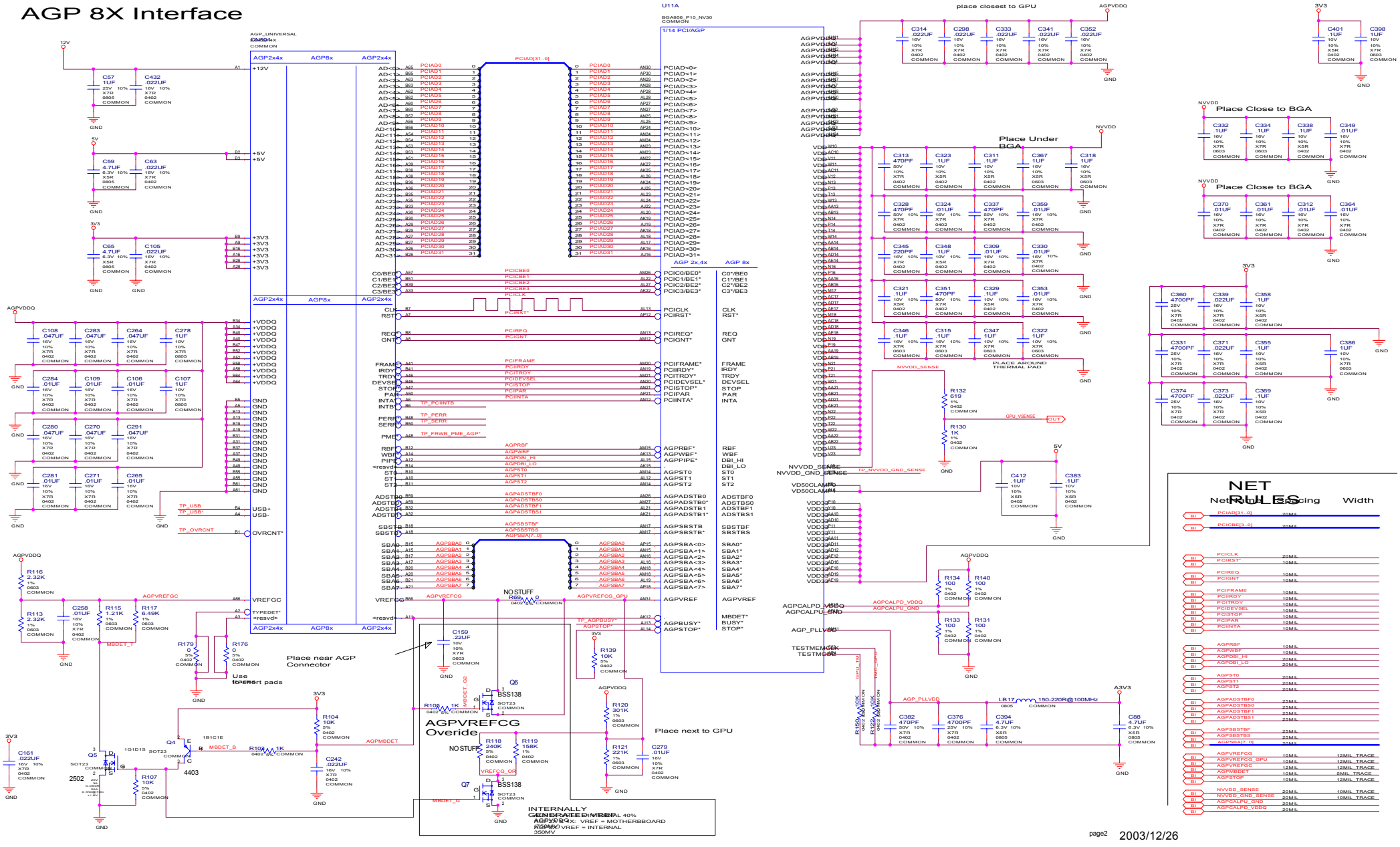
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<Edit here to insert page detail>


AGP 8X Interface
U11A
BGA956_P10_NV30
COMMON
1/14 PCI/AGP
AGP_UNIVERSAL
AGP2x4x
AGP8x
AGP2x4x
AGP 2x,4x
AGP 8x
place closest to GPU
AGPVDDQ
Place Under BGA
NVVDD
Place Close to BGA
PLACE AROUND THERMAL PAD
NVVDD_SENSE
GPU_VSENSE
NET RULES
Net Name
Spacing
Width
Place near AGP Connector
Use 1pcs smt pads
AGPVREFCG Overide
Place next to GPU
NO STUFF
INTERNALLY GENERATED VREF
AGP2X4X VREF = MOTHERBOARD
AGP8X VREF = INTERNAL
350MV
page2
2003/12/26
ASSEMBLY
BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE
<edit here to insert page detail>
PROJECT
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE
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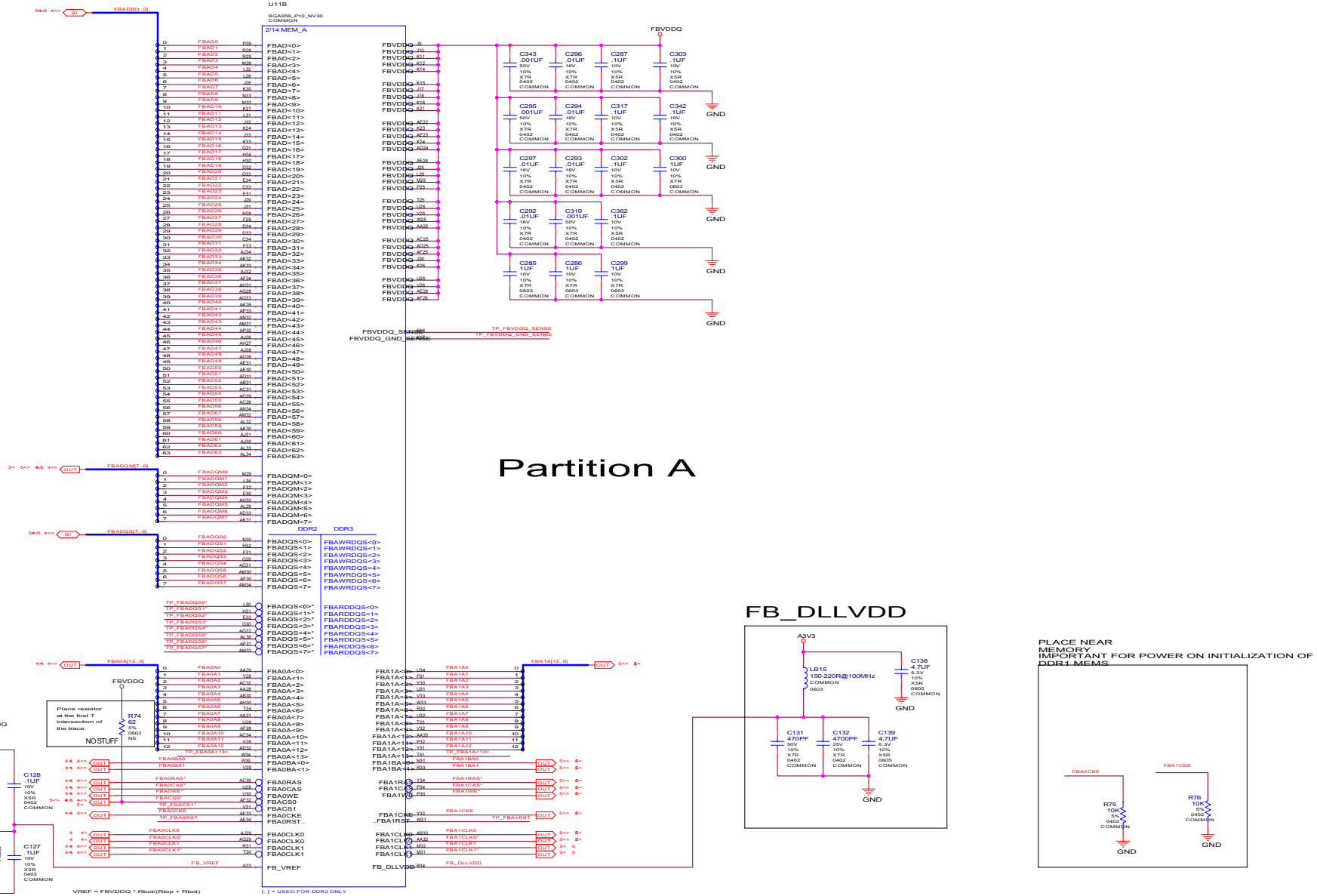
TRADE PRACTICE, OR INDUSTRY STANDARDS.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Edit Here to Insert page detail>

MEMORY 8(16)Mx16DDR Partition A , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

NET	Diffpair	NET_SPACING_RULE
FBA0CLK1	FBA0CLK1_DP	18MIL_G2G_25MIL
FBA0CLK1*	FBA0CLK1_DP	18MIL_G2G_25MIL
FBADQM[3..0]		10MIL
FBADQS[3..0]		15MIL
FBAD[31..0]		10MIL
FBADQM[3..0]		10MIL
FBADQS[3..0]		15MIL
FBA0A[12..0]		10MIL
FBA0RAS*		10MIL
FBA0CAS*		10MIL
FBA0WE*		10MIL
FBACS0*		10MIL
FBACS1*		10MIL
FBA0BA0		10MIL
FBA0BA1		10MIL
FBA0CKE		10MIL

TOP

BOTTOM

Clock Termination

FB_VREF

NO STUFF

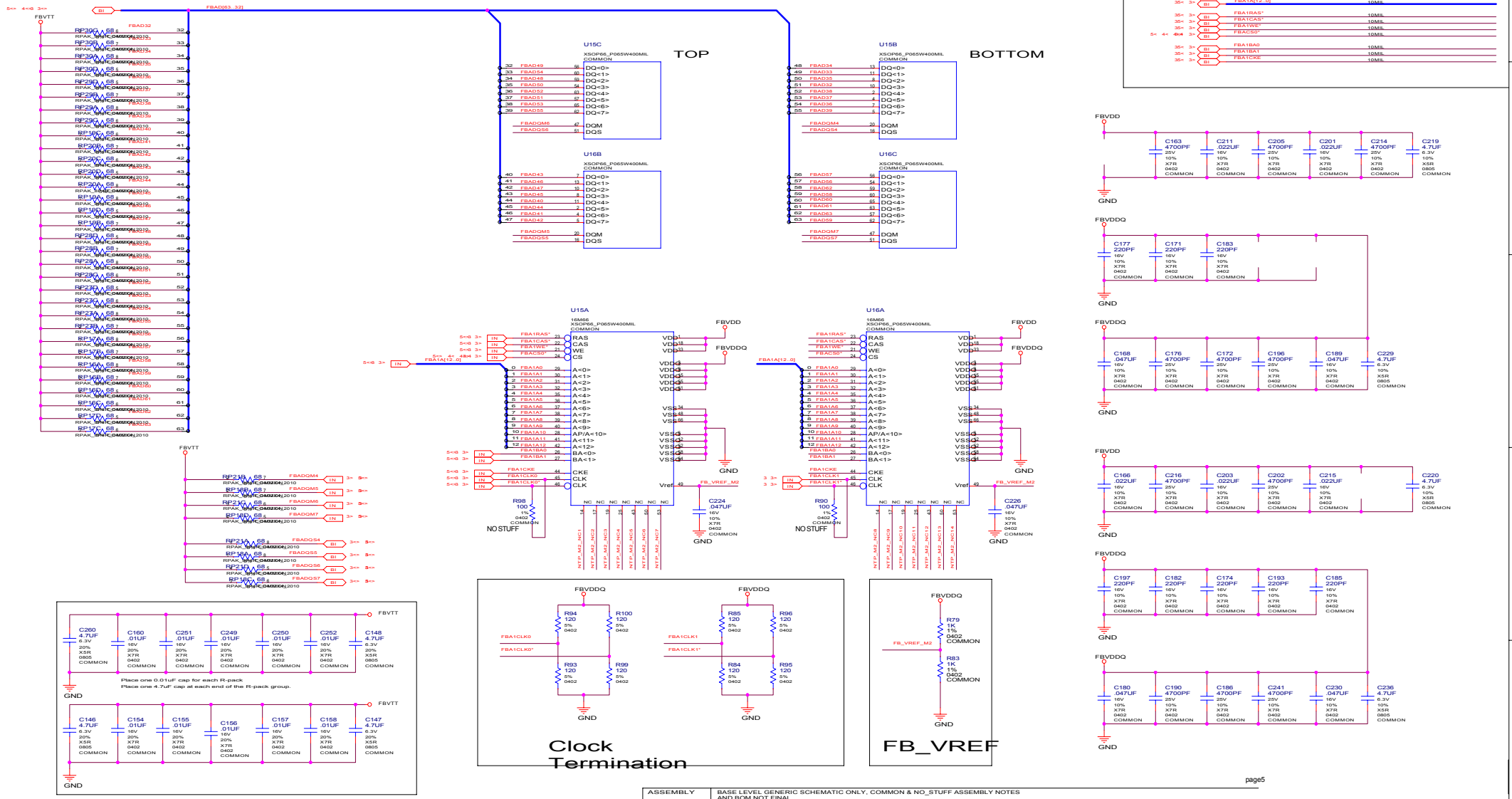
Place one 0.01uF cap for each R-pack
Place one 4.7uF cap at each end of the R-pack group.

page4

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>

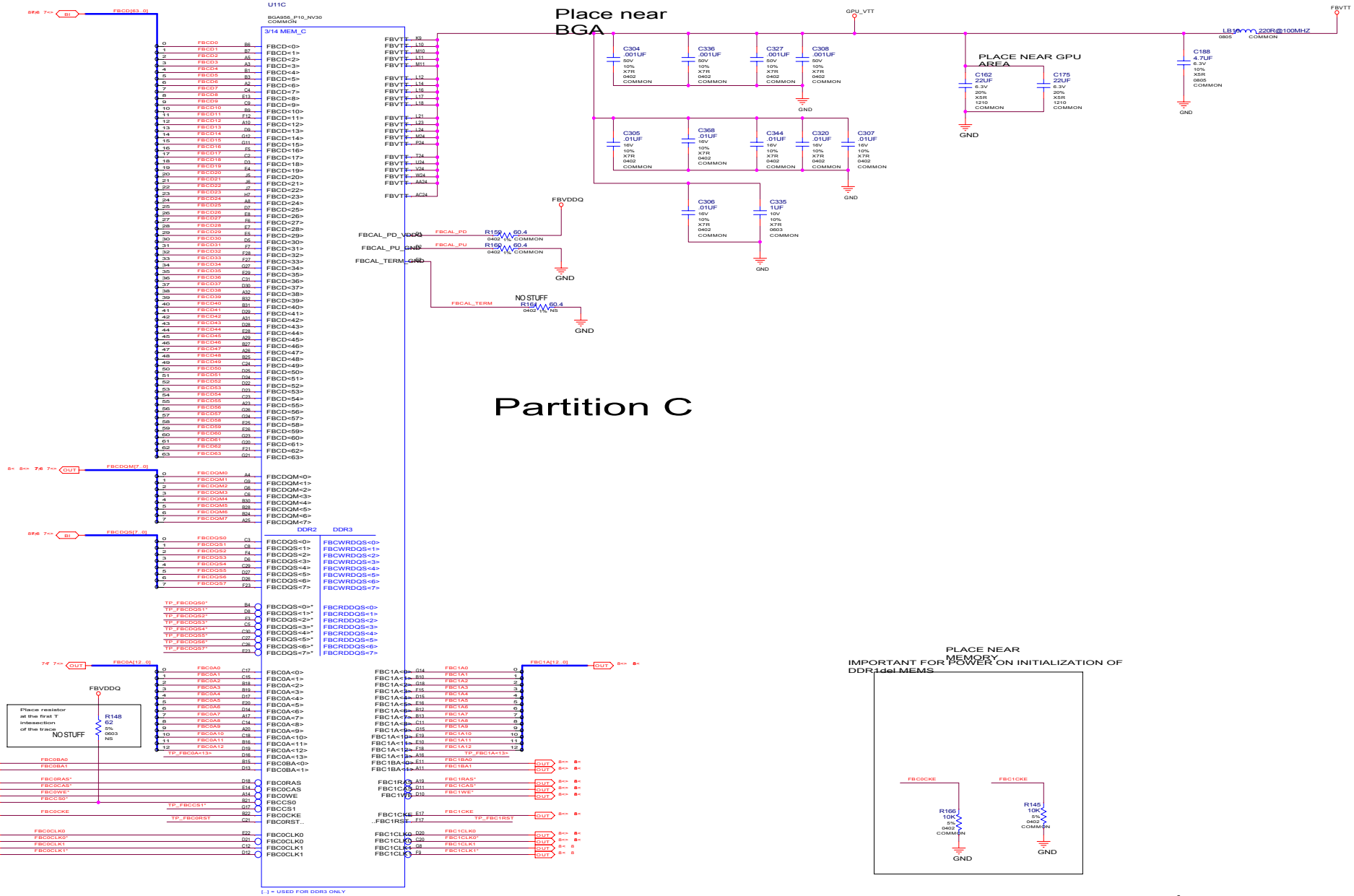
MEMORY 8(16)Mx16DDR Partition A , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



NET	Diffpair	NET_SPACING_RULE
FBA1CLK0	FBA1CLK0_DP	18MIL_G2G_25MIL
FBA1CLK0*	FBA1CLK0_DP	18MIL_G2G_25MIL
FBAD[63..32]		10MIL
FBADQM[7..4]		10MIL
FBADQS[7..4]		15MIL
FBAD[63..32]		10MIL
FBADQM[7..4]		10MIL
FBADQS[7..4]		15MIL
FBA1A[12..0]		10MIL
FBA1RAS*		10MIL
FBA1CAS*		10MIL
FBA1WE*		10MIL
FBACS0*		10MIL
FBA1BA0		10MIL
FBA1BA1		10MIL
FBA1CKE		10MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>
PAGE#	page5

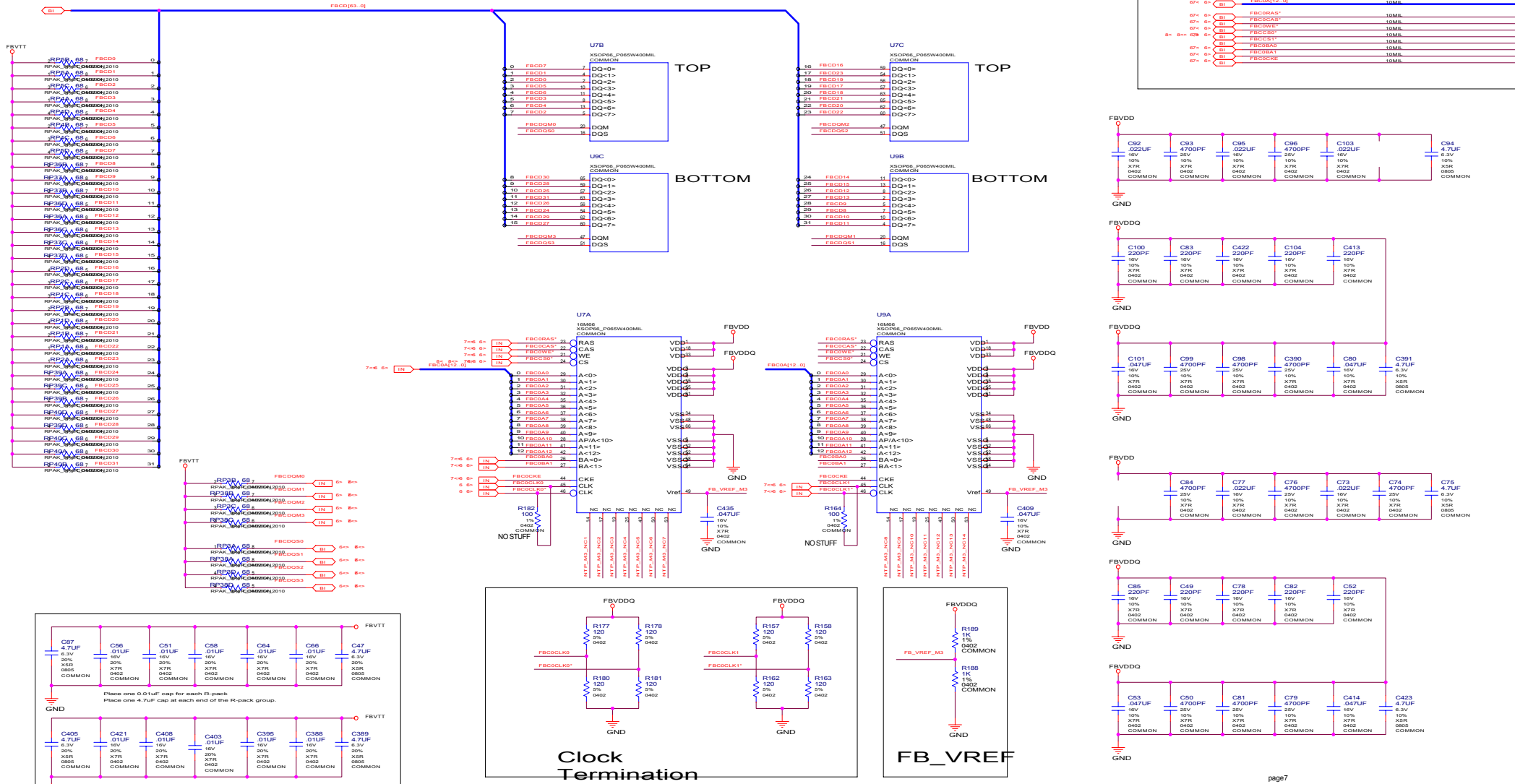


page6

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Scroll here to insert page detail>

MEMORY 8(16)Mx16DDR Partition C , Bits 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!



NET	Diffpair	NET_SPACING_RULE
FBC0CLK1	FBC0CLK1_DP	18MIL_G2G_25MIL
FBC0CLK1*	FBC0CLK1_DP	18MIL_G2G_25MIL
FBCD[31..0]		10MIL
FBCDQM[3..0]		10MIL
FBCDQS[3..0]		10MIL
FBCA[12..0]		10MIL
FBC0RAS*		10MIL
FBC0CAS*		10MIL
FBC0WE*		10MIL
FBCCS0*		10MIL
FBCCS1*		10MIL
FBC0BA0		10MIL
FBC0BA1		10MIL
FBC0CKE		10MIL

page7

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>
PAGE 31	

MEMORY 8(16)Mx16DDR Partition C , Bits 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY!

NET	Diffpair	NET_SPACING_RULE
FBC1CLK0	FBC1CLK0_DP	18MIL_G2G_25MIL
FBC1CLK0*	FBC1CLK0_DP	18MIL_G2G_25MIL
FBCD[63..32]		10MIL
FBCDQM[7..4]		10MIL
FBCDQS[7..4]		15MIL
FBCD[63..32]		10MIL
FBCDQM[7..4]		10MIL
FBCDQS[7..4]		15MIL
FBC1A[12..0]		10MIL
FBC1RAS*		10MIL
FBC1CAS*		10MIL
FBC1WE*		10MIL
FBCCS0*		10MIL
FBC1BA0		10MIL
FBC1BA1		10MIL
FBC1CKE		10MIL

TOP

BOTTOM

U10B / U12B / U12C / U10C — XSOP66_P065W400MIL COMMON

U10A / U12A — 16M66 XSOP66_P065W400MIL COMMON

R141 100 1% 0402 COMMON NO STUFF

R127 100 1% 0402 COMMON NO STUFF

C288 .047UF 16V 10% X7R 0402 COMMON

C365 .047UF 16V 10% X7R 0402 COMMON

FB_VREF_M4

FBVDD

FBVDDQ

GND

FBVTT

Place one 0.01uF cap for each R-pack
Place one 4.7uF cap at each end of the R-pack group.

Clock Termination

R135 120 5% 0402
R136 120 5% 0402
R137 120 5% 0402
R138 120 5% 0402
FBC1CLK0
FBC1CLK0*

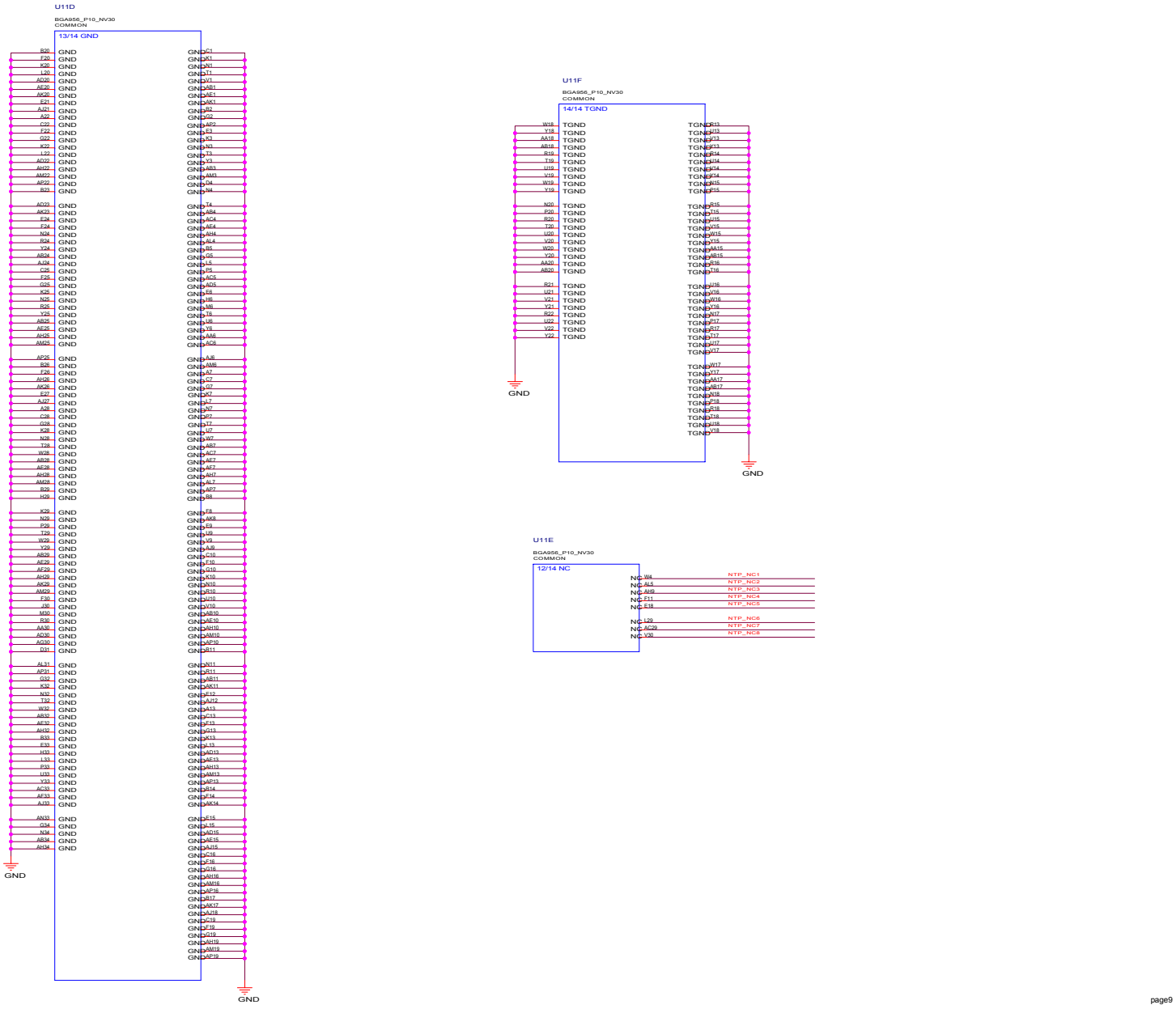
R123 120 5% 0402
R124 120 5% 0402
R125 120 5% 0402
R126 120 5% 0402
FBC1CLK1
FBC1CLK1*

FB_VREF

R129 1K 1% 0402 COMMON
R128 1K 1% 0402 COMMON
FB_VREF_M4

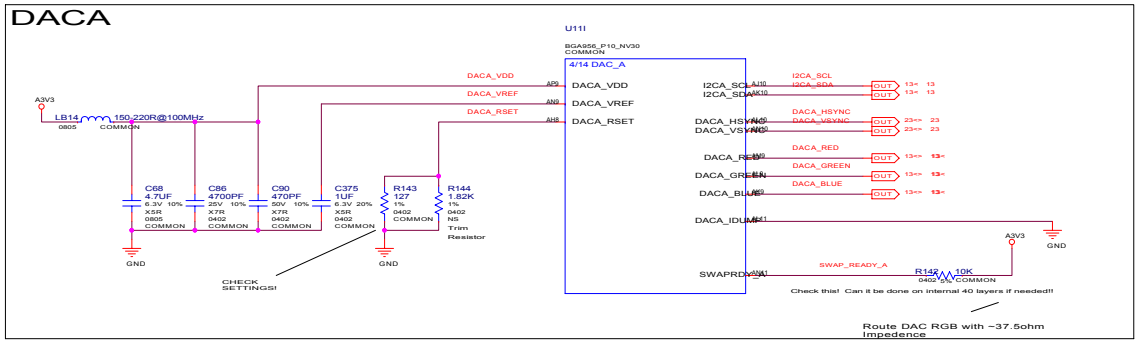
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>
PROJECT	

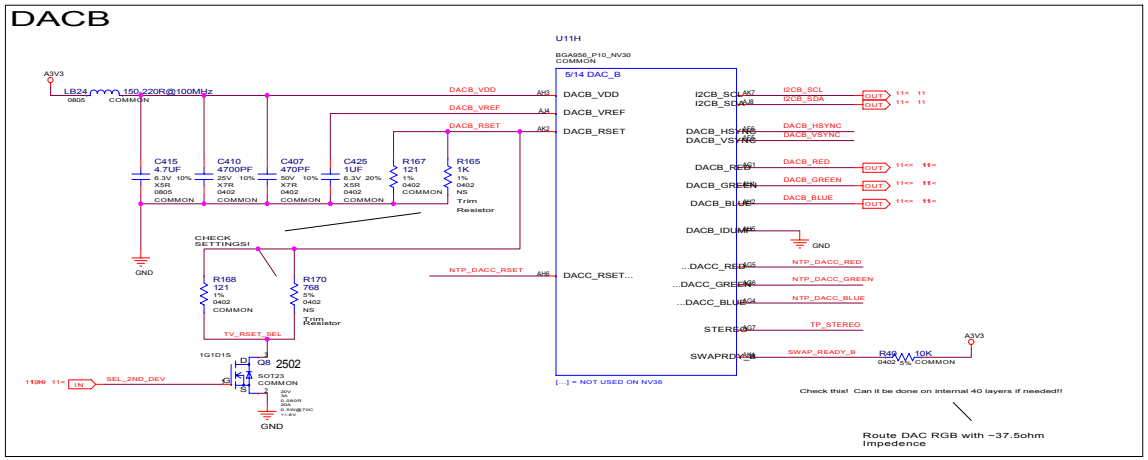
page8

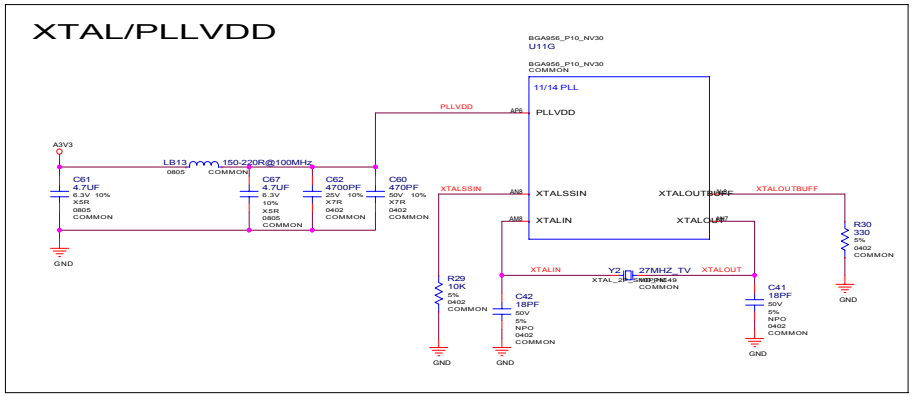


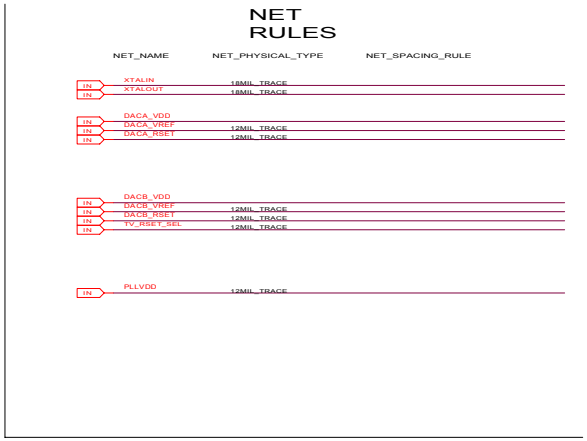
page9

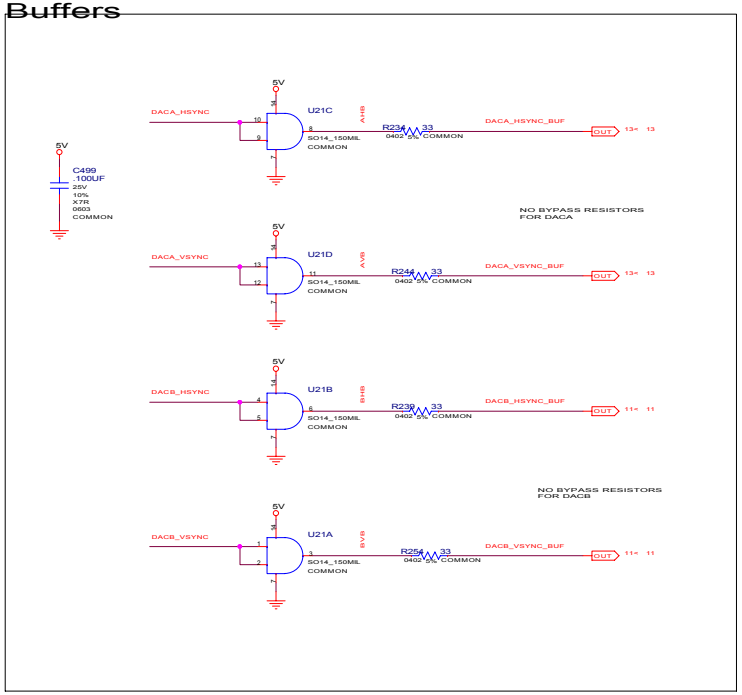
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Skip here to insert page detail>











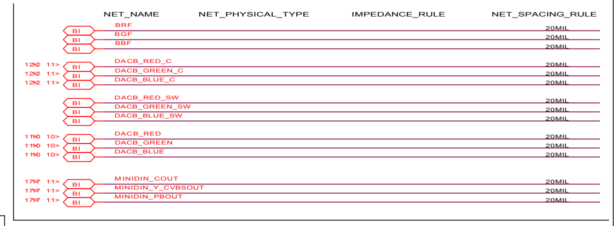
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	<edit here to insert page detail>

Secondary Display (DACB), Slim DB15

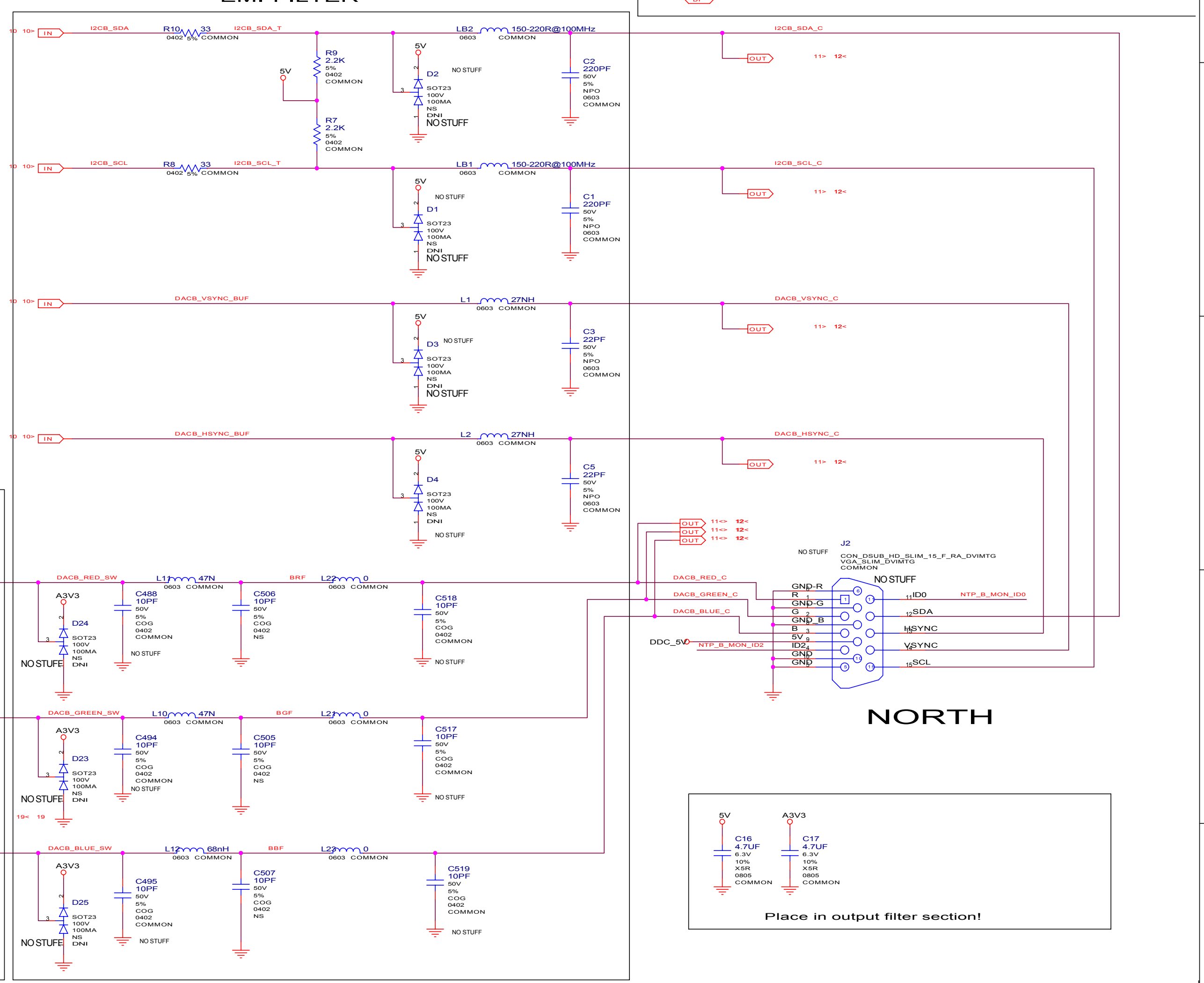
Place all filter components on the side nearest to the reference GND plane!

Route all signals only on layers referenced to GND!

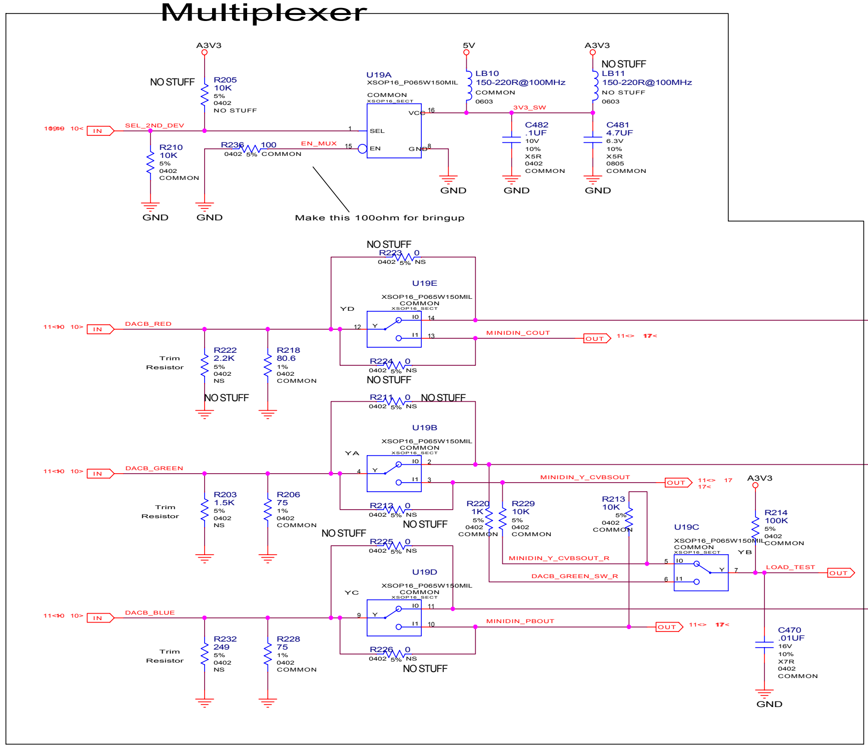
Don't split the reference GND plane beneath an RGB signal!



EMI-FILTER



DACB Multiplexer

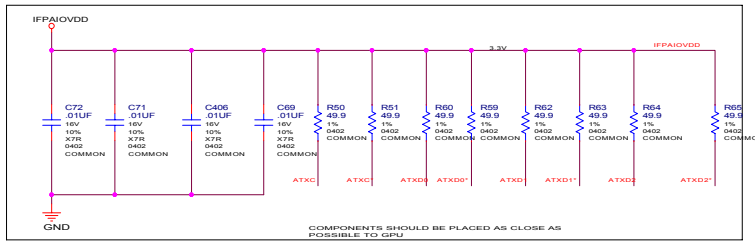


place nearest to connector

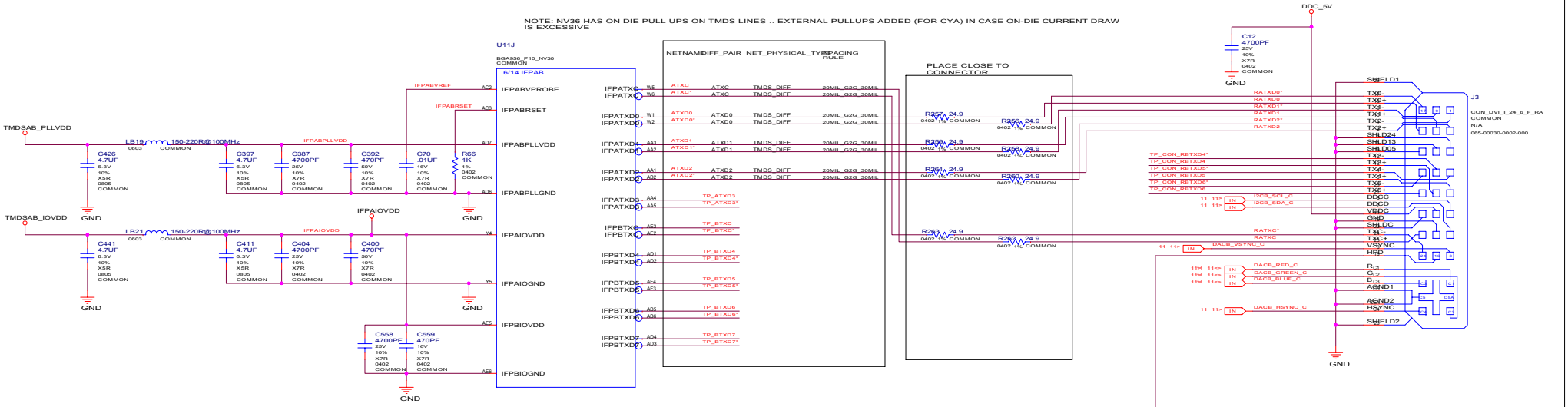
page11

ASSEMBLY PAGE DETAIL	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL <edit here to insert page detail>

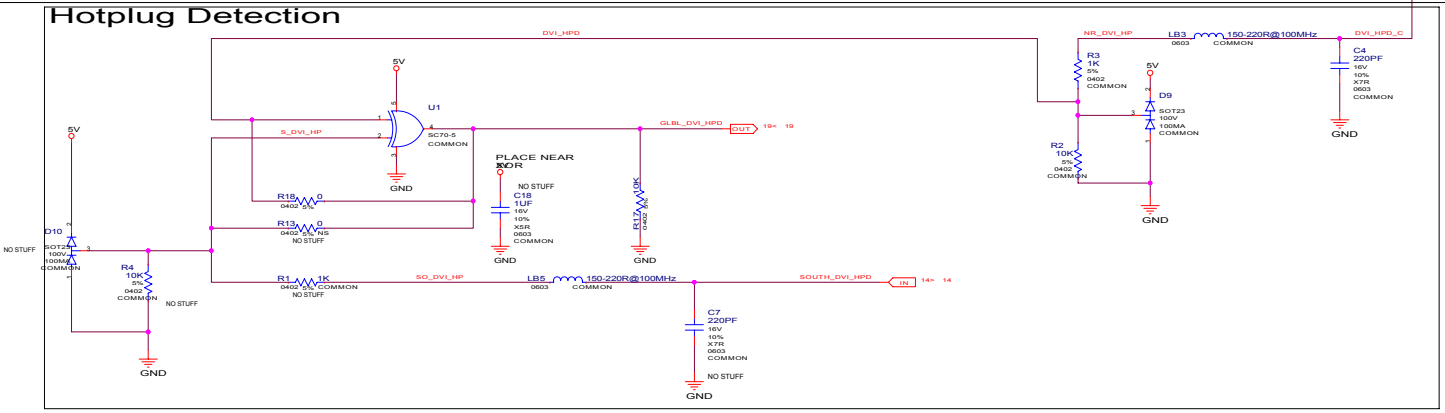
INTERNAL TMDS ..LINK A/B



NOTE: NV36 HAS ON DIE PULL UPS ON TMDS LINES .. EXTERNAL PULLUPS ADDED (FOR CYA) IN CASE ON-DIE CURRENT DRAW IS EXCESSIVE



Hotplug Detection



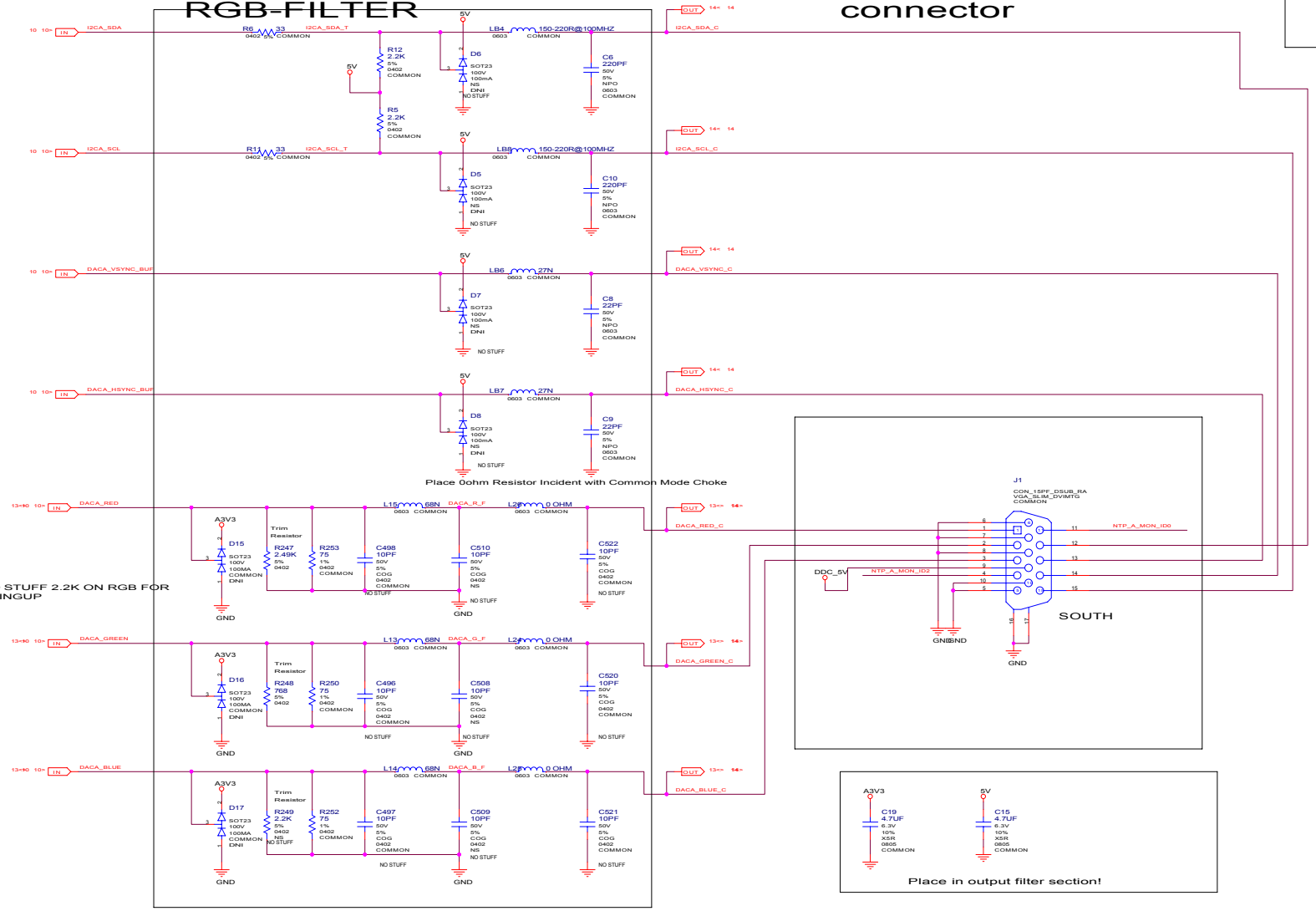
NET	NET_PHYSICAL_TYPE	VOLTAGE
IFPABVREF		3.3V
IFPABPLLVDD		3.3V

NETNAME	DIFF_PAIR	NET_PHYSICAL_TYPE	SPACING RULE
RATXD0*	RATXD0_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXD0	RATXD0_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXD1*	RATXD1_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXD1	RATXD1_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXD2*	RATXD2_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXD2	RATXD2_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXC*	RATXC_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RATXC	RATXC_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD0*	RBTXD0_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD0	RBTXD0_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD1*	RBTXD1_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD1	RBTXD1_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD2*	RBTXD2_C	TMDS_DIFF_AC	20MIL_G2G_30MIL
RBTXD2	RBTXD2_C	TMDS_DIFF_AC	20MIL_G2G_30MIL

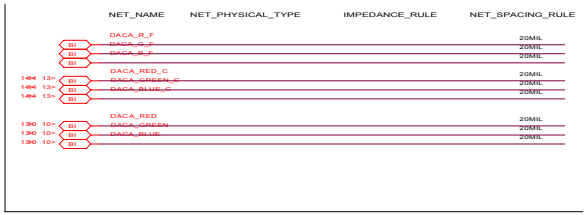
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Click here to insert page detail>

Primary Display (DACA), DB15 SLIM

DACA RGB-FILTER



DACA VGA connector



Place 0ohm Resistor Incident with Common Mode Choke

NO STUFF 2.2K ON RGB FOR BRINGUP

Place all filter components

on the side nearest to the

reference GND plane!

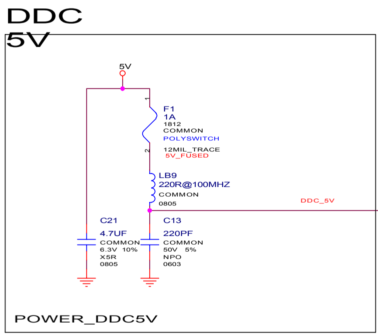
Route all signals only on

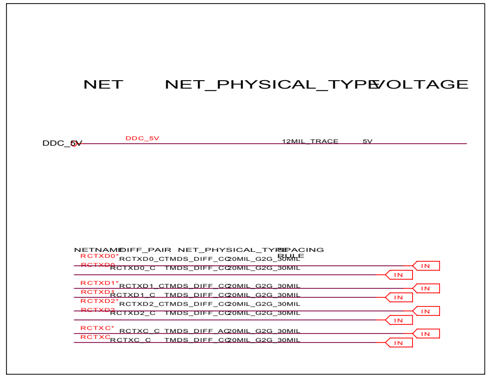
layers referenced to GND!

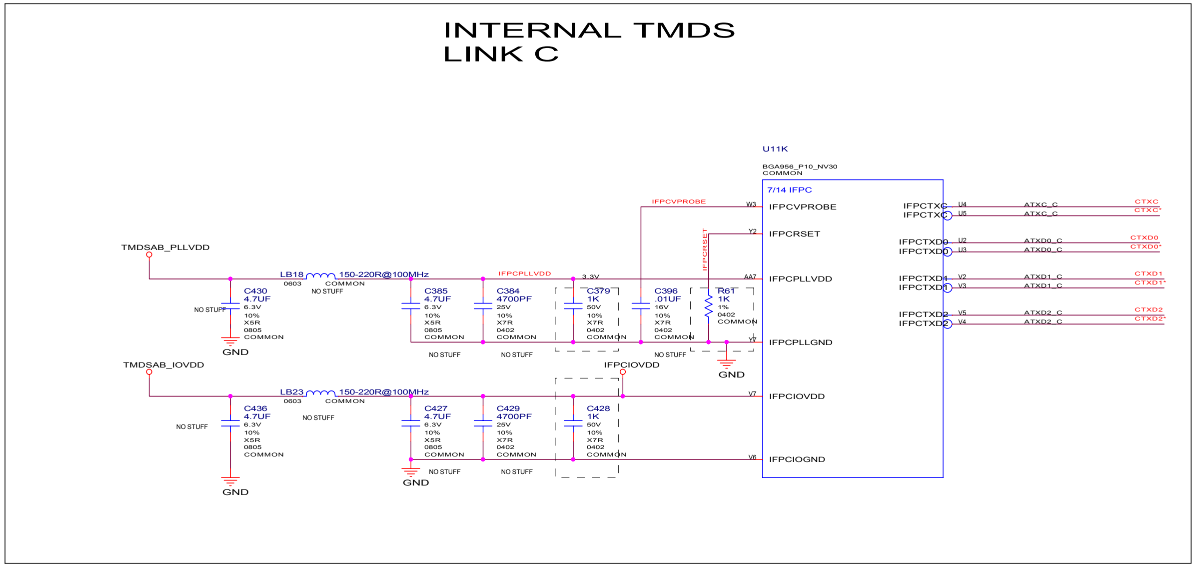
Don't split the reference

GND plane beneath an RGB signal!

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>
PAGE	







page14

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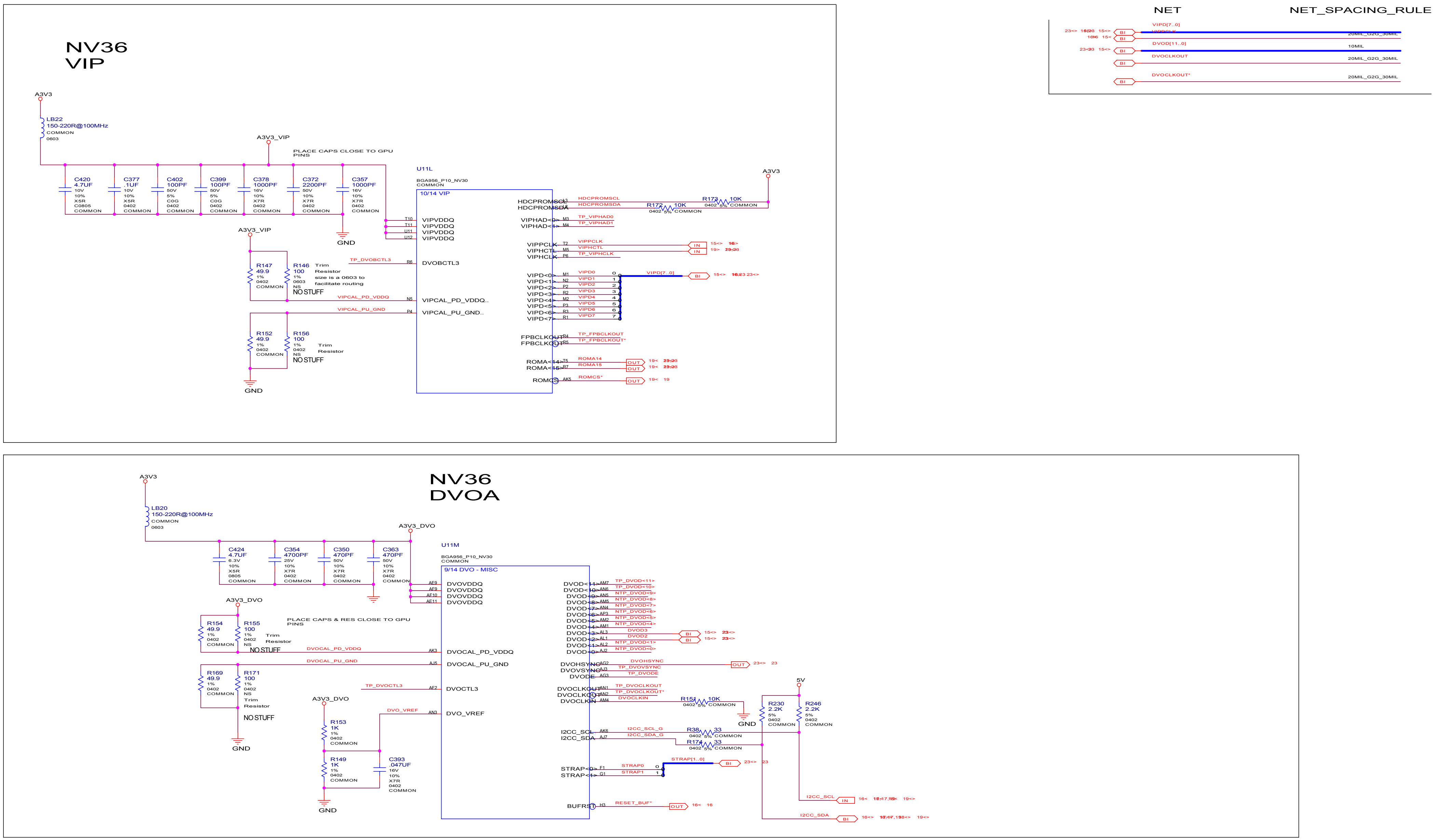
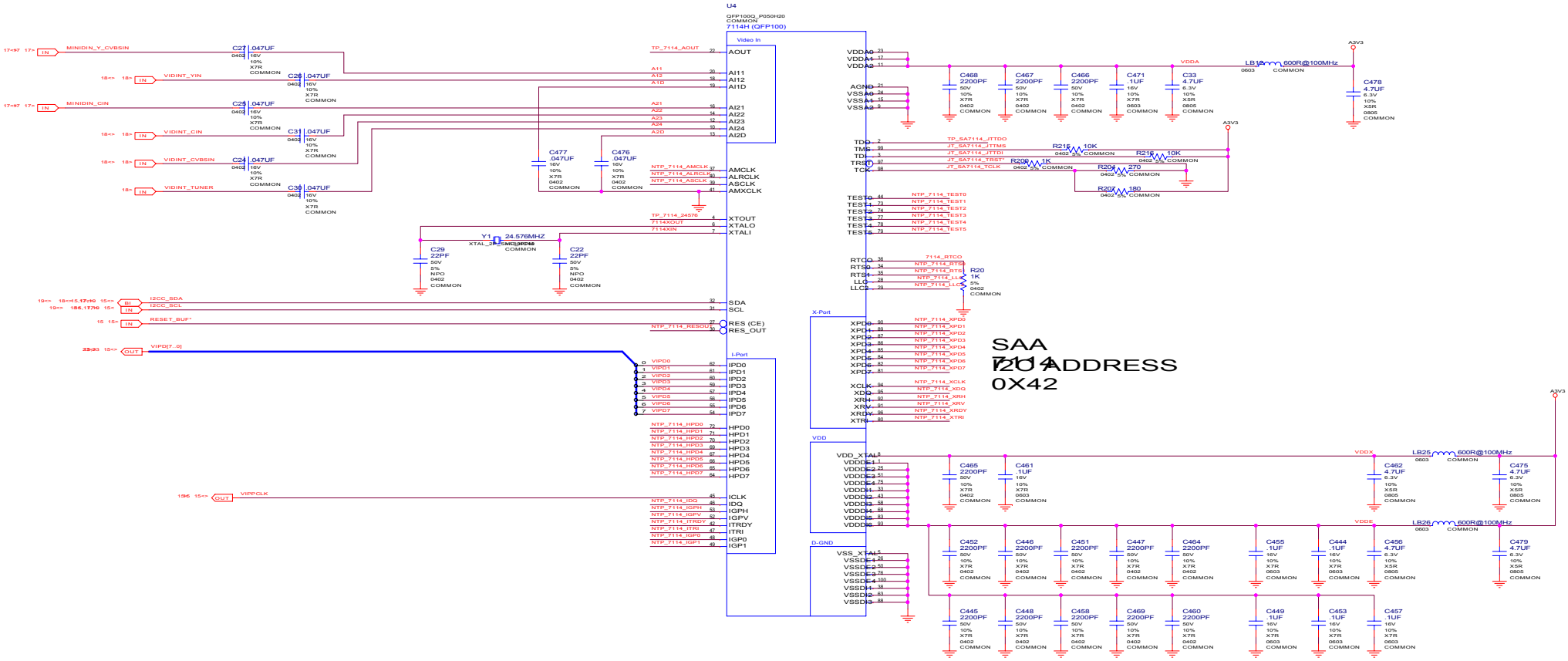


page15

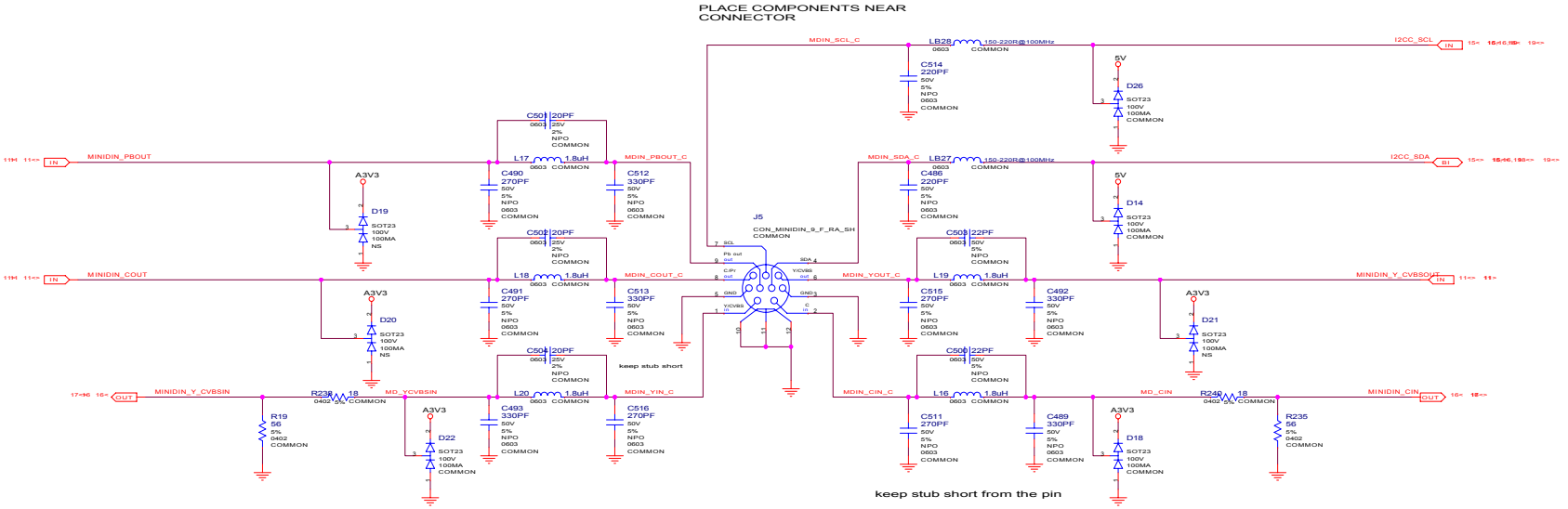
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE	AND BOM NOT FINAL
DETAIL	<edit here to insert page detail>

VIDEO CAPTURE



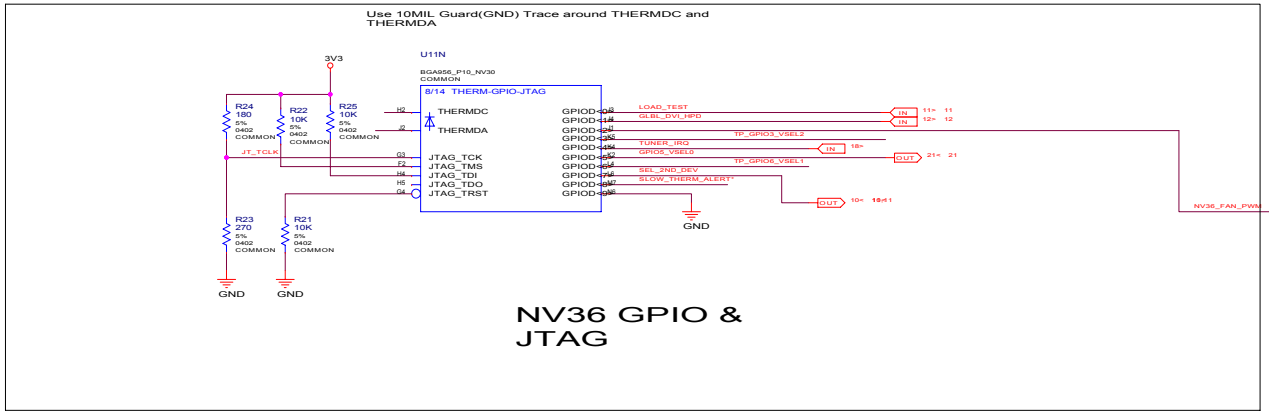
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Click here to insert page detail>

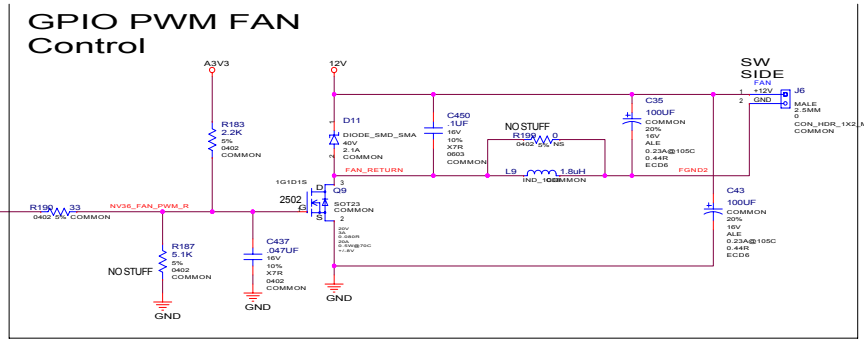
MiniDIN VIDEO IN/OUT CONNECTOR

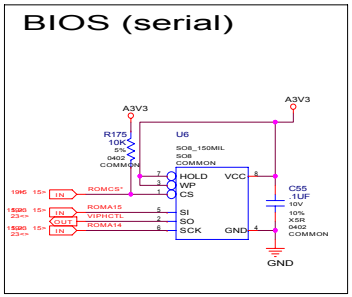


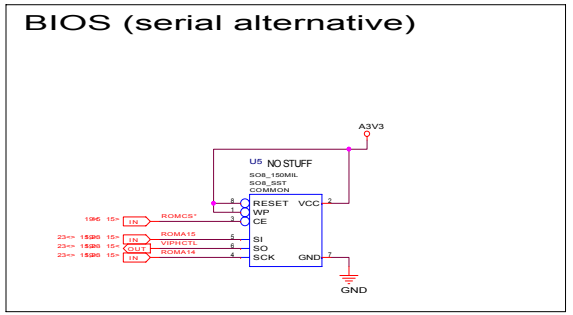
NET_NAME	NET_PHYSICAL_TYPE	IMPEDANCE_RULE	NET_SPACING_RULE
MINIDIN_Y_CVBSIN	BI		20MIL
MDIN_PBOUT_C	BI		20MIL
MDIN_COUT_C	BI		20MIL
MDIN_YIN_C	BI		20MIL
MDIN_YOUT_C	BI		20MIL
MDIN_CIN_C	BI		20MIL
MINIDIN_CIN	BI		20MIL
MD_PBOUT	BI		20MIL
MD_COUT	BI		20MIL
MD_YCVBSIN	BI		20MIL
MD_CIN	BI		20MIL
MD_YOUT	BI		20MIL
7104_BLUE_CVBS	BI		20MIL
7104_RED_COUT	BI		20MIL
7104_GREEN_YOUT	BI		20MIL

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AND BOM NOT FINAL <Click here to insert page detail>









NET NET_PHYSICAL_TYPEVOLTAGE

FAN_RETURN		12MIL_TRACE
THERMDC	BI	10MIL_TRACE
THERMDA	BI	10MIL_TRACE

NET NET_PHYSICAL_TYPE

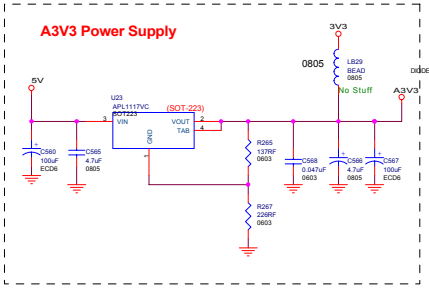
NV36_FAN_PWM	BI	20MIL
NV36_FAN_PWM_R	BI	20MIL

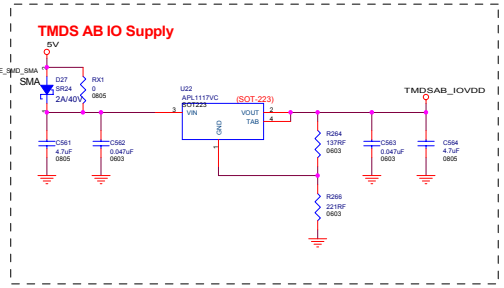
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE	<edit here to insert page detail>
PAGE#	

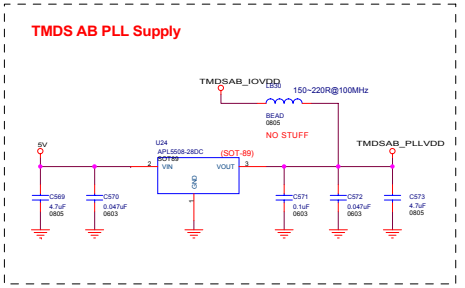
Power Supply ...
TMDS/A3V3/FBVDD

NET RULES

NET	PHYSICAL	VOLTAGE
A3V3	12MIL_TRACE	3.3V
FBVTT	12MIL_TRACE	0.9V
FBVDDQ	12MIL_TRACE	1.8V
NVVDD	12MIL_TRACE	1.2V
5V	12MIL_TRACE	5V
12V	12MIL_TRACE	12V
3V3	12MIL_TRACE	3.3V
AGPVDDQ	12MIL_TRACE	3.3V
GND	12MIL_TRACE	0V
TMDSAB_PLLVDD	12MIL_TRACE	2.8V
TMDSAB_IOVDD	12MIL_TRACE	2.8V
TMDSABPLL_ADJ	10MIL_TRACE	3.3V
TMDSABIO_ADJ	10MIL_TRACE	3.3V
6529_SW_12V	10MIL_TRACE	12V
6529_5V	12MIL_TRACE	5V
3V3_6529	16MIL_TRACE	3.3V
6529_SW_OUT	16MIL_TRACE	3.3V
6529_SW_COMP	10MIL_TRACE	3.3V
6529_SW_COMP_FB	10MIL_TRACE	3.3V
6529_SW_FB	10MIL_TRACE	2.5V
6529_SW_SOMP3_FB	10MIL_TRACE	3.3V
6529_SW_SNB	12MIL_TRACE	3.3V
6529_SW_DRHI	24MIL_TRACE	12V
6529_SW_DRLO	24MIL_TRACE	12V
6529_SW_SW	24MIL_TRACE	12V
6529_SW_CL	24MIL_TRACE	12V
6529_L_GATE	16MIL_TRACE	5V
6529_L_GATE_R	16MIL_TRACE	5V
6529_VDD_FB	10MIL_TRACE	2.5V
6529_GND_FB	10MIL_TRACE	3.3V
5V_LDO_IN	16MIL_TRACE	5V
6529_L_COMP	10MIL_TRACE	3.3V
6529_L_FB	10MIL_TRACE	3.3V



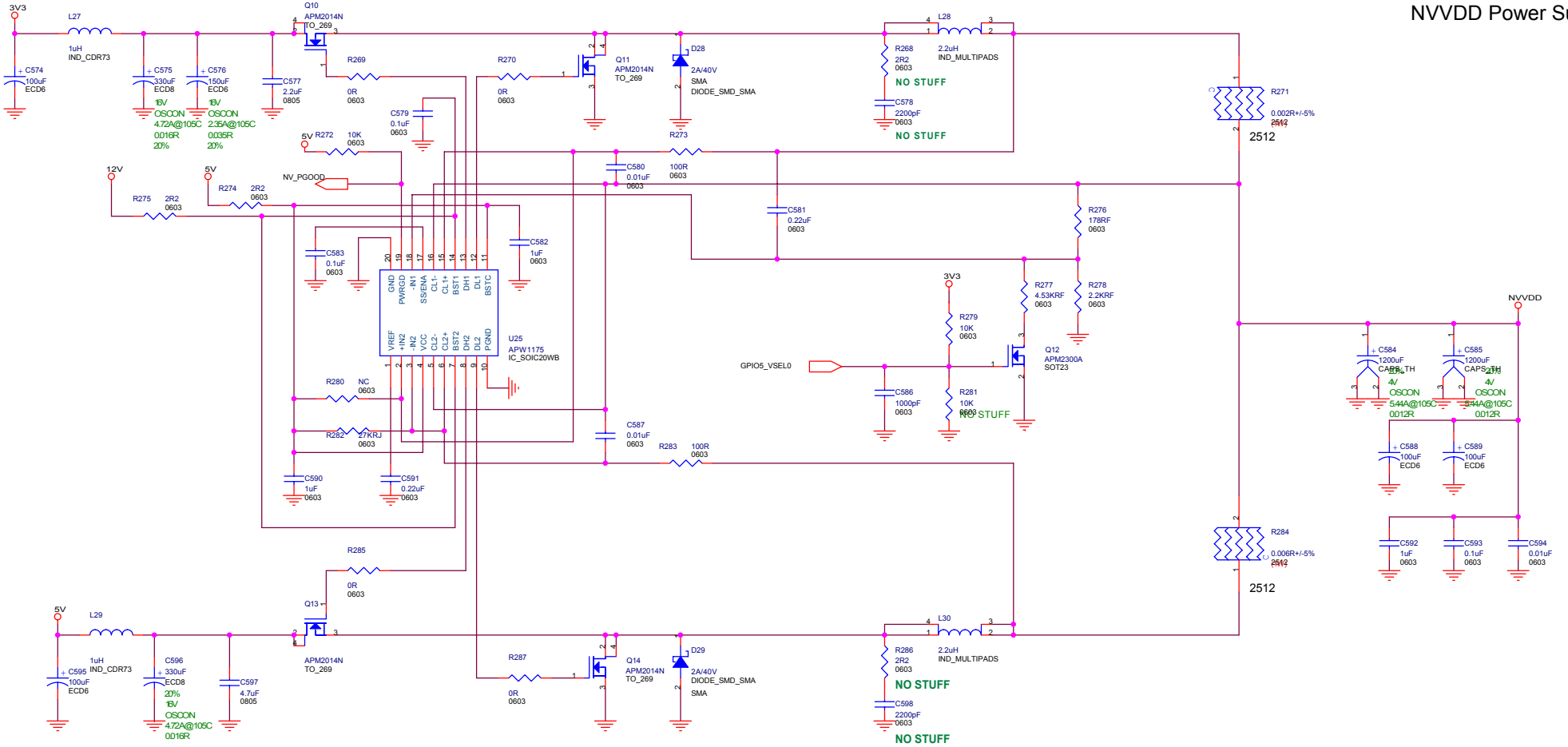




SP8836 C1.1

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES
PAGE DETAIL	AMD BGM1 MXM_EMIO <Click here to insert page detail>

NVVDD Power Supply

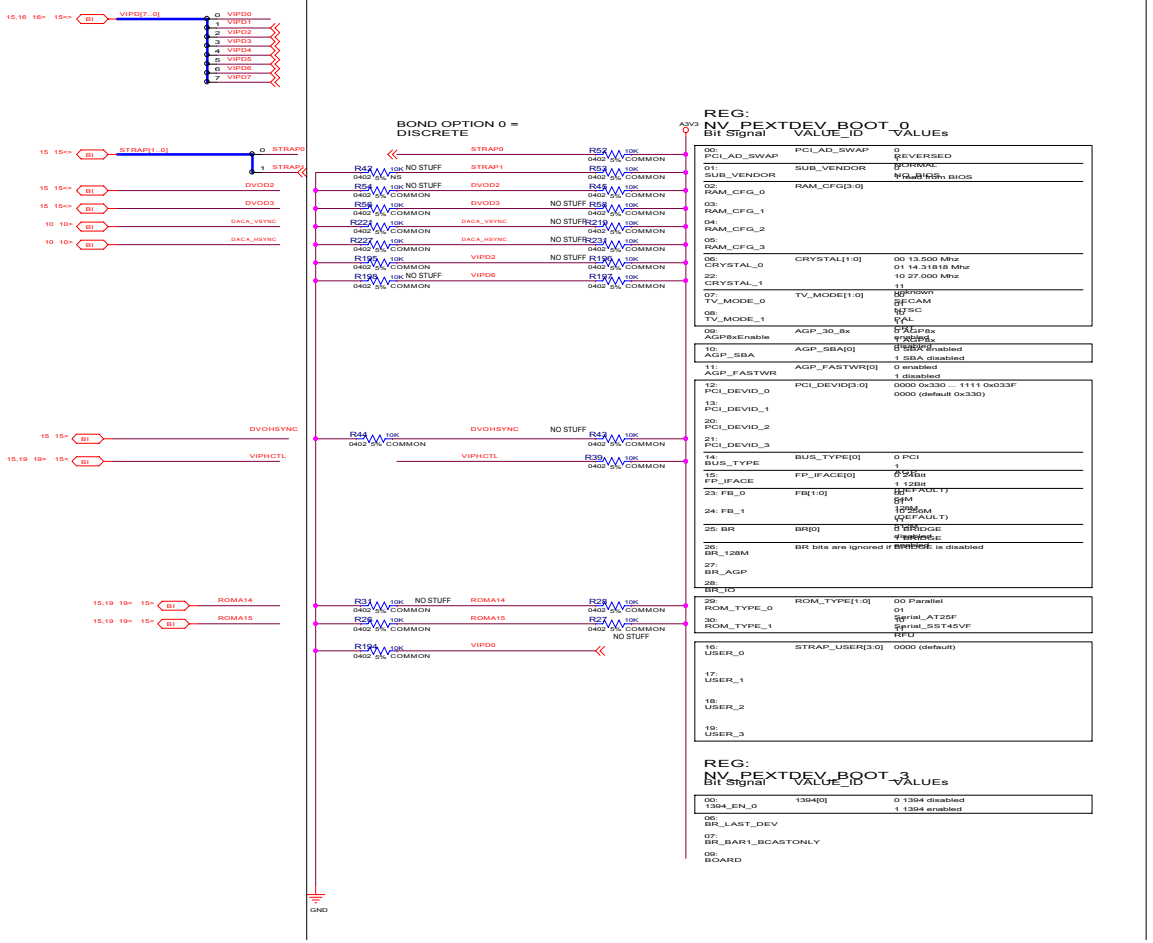


Title	NVVDD	
Size A3	Document Number <Doc>	Rev 0
Date: Friday, January 02, 2004	Sheet 20 of 22	

BIOS, Straps, Misc

Straps

Assembly:
BIOS



REG: NV_PEXTDEV_BOOT_0

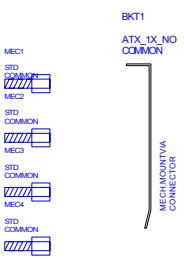
Bit	Signal	VALUE_ID	VALUEs
00: PCI_AD_SWAP	PCI_AD_SWAP	0	0 REVERSED
01: SUB_VENDOR	SUB_VENDOR	0	0 NORMAL
02: RAM_CFG_0	RAM_CFG[3:0]		1 Nvidia BIOS
03: RAM_CFG_1			
04: RAM_CFG_2			
05: RAM_CFG_3			
06: CRYSTAL_0	CRYSTAL[1:0]		00 13.500 Mhz 01 14.31818 Mhz
22: CRYSTAL_1			10 27.000 Mhz 11
07: TV_MODE_0	TV_MODE[1:0]		00 unknown 01 SECAM
08: TV_MODE_1			10 NTSC 11 PAL
09: AGPBxEnable	AGP_30_8x		0 AGP8x 1 AGP3x
10: AGP_SBA	AGP_SBA[0]		0 SBA enabled 1 SBA disabled
11: AGP_FASTWR	AGP_FASTWR[0]		0 enabled 1 disabled
12: PCI_DEVID_0	PCI_DEVID[3:0]		0000 0x330 ... 1111 0x033F 0000 (default 0x330)
13: PCI_DEVID_1			
20: PCI_DEVID_2			
21: PCI_DEVID_3			
14: BUS_TYPE	BUS_TYPE[0]		0 PCI 1
15: FP_IFACE	FP_IFACE[0]		0 24bit 1 12Bit
23: FB_0	FB[1:0]		00 (DEFAULT) 01 8M
24: FB_1			10 16M 11 32M (DEFAULT)
25: BR	BR[0]		0 BRIDGE 1 DISABLE
26: BR_128M	BR bits are ignored if BR[0] is disabled		
27: BR_AGP			
28: BR_IO			
29: ROM_TYPE_0	ROM_TYPE[1:0]		00 Parallel 01
30: ROM_TYPE_1			10 Serial_AT25F 11 Serial_SST45VF
16: USER_0	STRAP_USER[3:0]		RFU 0000 (default)
17: USER_1			
18: USER_2			
19: USER_3			

REG: NV_PEXTDEV_BOOT_3

Bit	Signal	VALUE_ID	VALUEs
00: 1394_EN_0	1394[0]		0 1394 disabled 1 1394 enabled
06: BR_LAST_DEV			
07: BR_BAR1_BCASTONLY			
09: BOARD			

Mechanical parts

Bracket will be corrected
when it becomes available in Agile (Tab-3)
and in the PTF file
SKU 600-10191-0000-000 will use bracket
151-10053-0000-000 V1.1
(north-to-south)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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