AL2230

Single Chip Transceiver for 2.4GHz 802.11b/g Applications

(AIROHA)

REVISION HISTORY

Version	Change Summary	Date	Author
0.80	Spec revised for Rev-B	11-Feb-04	KH Chen
0.81	Minor Change	12-Feb-04	KH Chen
0.82	Minor Change	12-Feb-04	KH Chen
0.90	Spec revised	24-Jun-04	KH Chen
0.91	Minor Change	20-Jul-04	KH Chen
0.92	Minor Change	26-Aug-04	KH Chen
1.00	Spec update to MP version	04-Oct-04	KH Chen
1.01	Minor changes	06-Oct-04	PY Chiu

Internal reference: DataSheetAL2230MPv101.doc

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TABLE

FIGURE

AL2230 – Single Chip Transceiver for 2.4GHz 802.11b/g

Applications

1 Features

- Highly integrated 2.4GHz band transceiver with Direct Conversion architecture
- Receiver with 40dB RF selectable gain range and 60dB baseband variable gain range
- Analog RSSI output with 60dB dynamic range
- Integrated baseband filters with programmable bandwidth for Transmitter and Receiver
- Three-wire control interface
- Integrate PA with 20dBm output power for 11b and 17dBm for 11g
- Integrate RF detector for APC
- Single-ended LNA input without the need of external balun
- On-chip DC offset correction
- Embedded IQ mismatch calibration
- Small QFN-48 package (7mm×7mm)

2 Description

AL2230 is a highly integrated RF transceiver IC for 2.4GHz band 802.11b/g applications, and combines all functions of the transceiver in a single chip. AL2230 also integrates on-chip PA and PLL to help you to minimize the use of external components to design an RF subsystem.

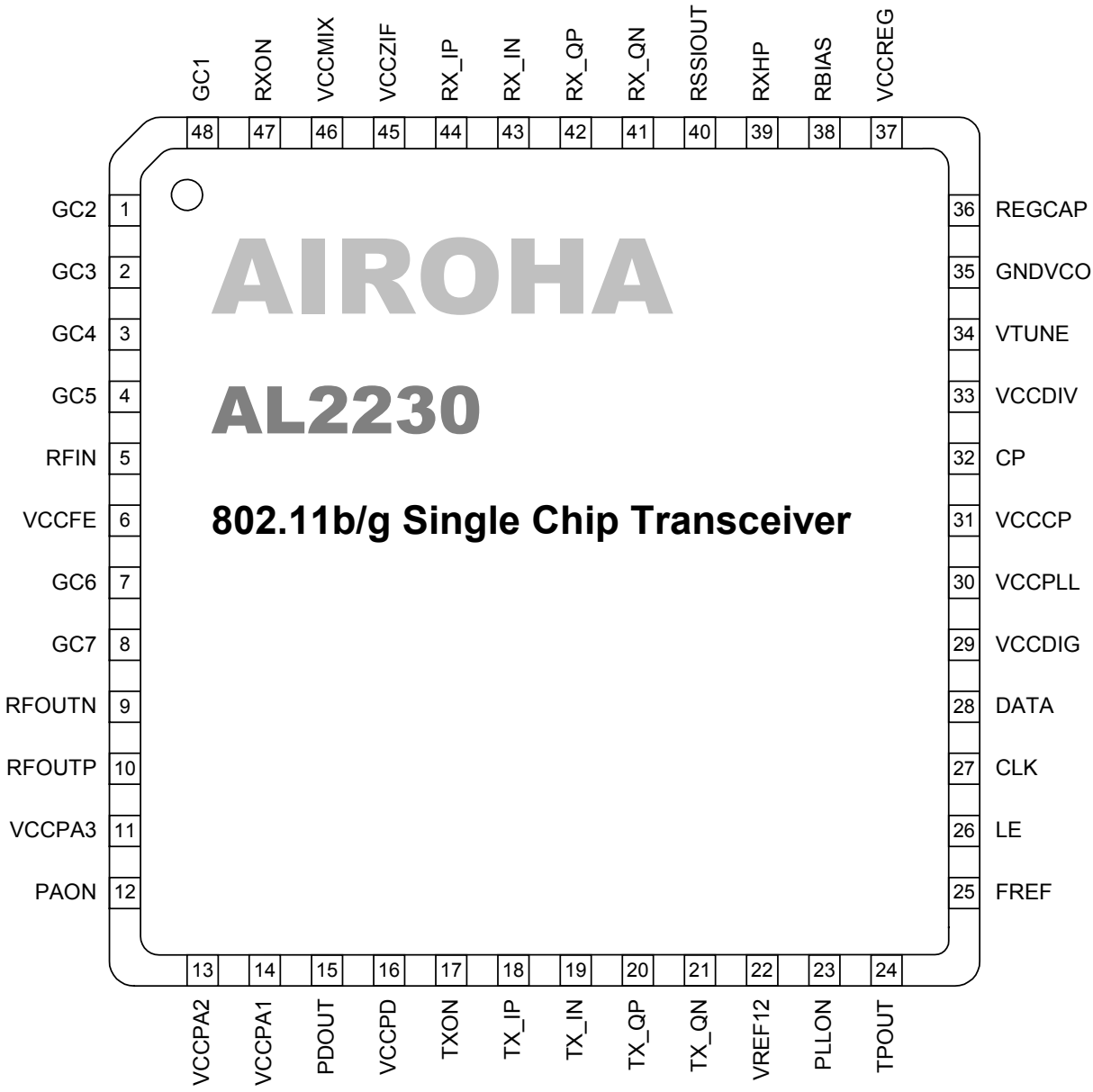
The receive path implements a direct down-conversion architecture to eliminate additional IF filters. It includes a single-ended input Low Noise Amplifier (LNA), a direct down-conversion mixer with DC-offset cancellation, and a variable gain amplifier with a baseband low-pass filter.

The transmitter consists of a direct up-conversion quadrature modulator with a baseband low pass filter, a variable gain amplifier, a power amplifier and a power detector to complete the whole transmit path function.

A power-on calibration procedure is established to correct the TX DC offset and filters mismatch.

These functions are housed in a 48-pin QFN package.

3 Pin Assignment/Functional Diagram



4 Pin Name Description

PIN	SIGANL	TYPE	DESCRIPTION
1	GC2	Input, Digital Control	RX BB AGC gain control / TX AGC gain control
2	GC3	Input, Digital Control	RX BB AGC gain control / TX AGC gain control
3	GC4	Input, Digital Control	RX BB AGC gain control / TX AGC gain control
4	GC5	Input, Digital Control	RX BB AGC gain control / TX AGC gain control
5	RFIN	Input, RF	LNA Input
6	VCCFE	Supply, 2.8V	Supply Voltage 2.8 Volts for RF front-end
7	GC6	Input, Digital Control	RX RF gain control / TX AGC gain control
8	GC7	Input, Digital Control	RX RF gain control
9	RFOUTN	Output, Differential RF	TX PA output
10	RFOUTP	Output, Differential RF	TX PA output
11	VCCPA3	Supply, 3.3V	Supply Voltage 3.3 Volts for power amplifier
12	PAON	Input, Digital Control	PA Timing Control
13	VCCPA2	Supply, 3.3V	Supply Voltage 3.3 Volts for power amplifier
14	VCCPA1	Supply, 3.3V	Supply Voltage 3.3 Volts for power amplifier
15	PDOUT	Output, Analog	Power Detector output
16	VCCPD	Supply, 2.8V	Supply Voltage 2.8 Volts for power detector
17	TXON	Input, Digital Control	TX Timing Control
18	TX_IP	Input, Differential Analog	TX BB input
19	TX_IN	Input, Differential Analog	TX BB input
20	TX_QP	Input, Differential Analog	TX BB input
21	TX_QN	Input, Differential Analog	TX BB input
22	VREF12	Output, 1.2V	Reference Voltage 1.2 Volts
23	PLLON	Input, Digital Control	PLL Timing Control
24	TPOUT	Output, Test	Test Pin
25	FREF	Input, Analog	Reference Clock input
26	LE	Input, Digital Control	3-wire Serial Interface
27	CLK	Input, Digital Control	3-wire Serial Interface
28	DATA	Input, Digital Control	3-wire Serial Interface
29	VCCDIG	Supply, 2.8V	Supply Voltage 2.8 Volts for digital circuits
30	VCCPLL	Supply, 2.8V	Supply Voltage 2.8 Volts for PLL

31	VCCCP	Supply, 2.8V	Supply Voltage 2.8 Volts for charge pump
32	CP	Output, Analog	Charge Pump Current Output
33	VCCDIV	Supply, 2.8V	Supply Voltage 2.8 Volts for divider
34	VTUNE	NC	Not Connected, Keep Floating
35	GNDVCO	Ground	Ground
36	REGCAP	Output, 2.4V	2.4V LDO output
37	VCCREG	Supply, 2.8V	Supply Voltage 2.8 Volts for internal regulator
38	RBIAS	Output, 100 μA	Reference Resister
39	RXHP	Input, Digital Control	RX DCOC control
40	RSSIOUT	Output, Analog	RX RSSI output
41	RX_QN	Output, Differential Analog	RX BB output
42	RX_QP	Output, Differential Analog	RX BB output
43	RX_IN	Output, Differential Analog	RX BB output
44	RX_IP	Output, Differential Analog	RX BB output
45	VCCZIF	Supply, 2.8V	Supply Voltage 2.8 Volts for zero-IF part
46	VCCMIX	Supply, 2.8V	Supply Voltage 2.8 Volts for mixer
47	RXON	Input, Digital Control	RX Timing Control
48	GC1	Input, Digital Control	RX BB AGC gain control / TX AGC gain control

5 Block Description

5.1 General Description

The AL2230 is a 2.4GHz-band transceiver for 802.11b/g applications. There are five main blocks – power amplifier, transmitter, receiver, synthesizer and three-wire interface.

The control pins: PLLON, TXON, RXON and PAON are responsible for the power control of the chip. The whole chip is powered up when PLLON is set to High, and the synthesizer is enabled at the same time. After the chip powered-up, the transmitter or receiver block is enabled when TXON or RXON being set to High, respectively. The PA block is controlled by the PAON pin independently, irrelative to the state of PLLON.

5.2 Receiver

The receiver implements a direct-conversion architecture, which is composed with two parts: RF front-end and Zero-IF baseband. The RF front-end part comprises a LNA and a quadrature mixer. The ZIF baseband part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a RSSI log amplifier for RSSI output.

At the RF front-end part, the LNA input is single-ended without the need of external balun. The front-end gain could be adjusted through control pins or 3-wire interface, and thus reduce the probability of bit errors caused by poor signal-to-noise ratio.

After the LNA is followed by a quadrature mixer that down-converts the RF signal directly to baseband signal. A direct-conversion architecture is implemented in order to eliminate the external SAW filters.

At the ZIF baseband part, the down-converted baseband signal is first low-pass filtered by the LPF, and then amplified by the VGA. The 3dB bandwidth of the LPF could be set from 7.5MHz to 20MHz through 3-wire interface.

The VGA provides variable gain with 60dB dynamic range, and could be controlled through control pins or 3-wire interface.

The RSSI log amplifier measures the received signal strength and converts to a voltage signal RSSI output. The dynamic range of RSSI is 60dB. The output range is selectable for HIGH range (max. output voltage 2.4V) and LOW range (max. output voltage 2.0V).

The RSSI output voltage is proportional to the input signal power level in decibel, and is irrelative to RXGC setting when GC<5:1>=31~7. However, when GC<5:1>=6~0, the RSSI output voltage would drop 0.34V (for High range) or 0.25V (for Low range) under the same input signal power level.

The Rx I/Q output are designed to be directly connected (DC-coupled) to I/Q ADC inputs of the baseband IC. The common voltage of RX I/Q outputs is 1.2V.

The RF front-end provides 5dB system noise figure, –17dBm IIP3, and a RF gain step of 22dB/18dB. The baseband provides 60dB gain range from maximum to minimum. The overall voltage gain control range is 100dB.

5.3 Transmitter

The transmitter implements a direct-up-conversion architecture, which comprises a LPF, a modulator and a VGA stage. The TX baseband I/Q interface is designed as differential analog inputs directly connected (DC-coupled) to the I/Q DAC outputs of the baseband IC.

A LPF is implemented to attenuate the second sidelobe of signal spectrum and unwanted oversampling clock or spurious signals. The 3dB bandwidth of the LPF could be set from 12MHz to 30MHz through 3-wire interface.

The VGA provides variable gain with 30dB dynamic range, and could be controlled through control pins or 3-wire interface.

5.4 PA

The gain of the power amplifier can be adjusted via bias current, which is controlled through 3-wire interface. Output power is +20dBm for 11b and +17dBm for 11g.

An on-chip power detector is integrated to measure the output power strength. Power detector samples the peak voltage of the output power and generates a voltage proportional to the output power.

5.5 Synthesizer

The AL2230 includes a fractional-N synthesizer. The reference frequency is fed from an external 20/40MHz oscillator.

6 Power-on Calibration

Power-on calibration procedure is necessary for AL2230. When AL2230 is turned on, several calibration steps including TX DCOC and Filter imbalance are processed and controlled by baseband controller via 3-wire interface.

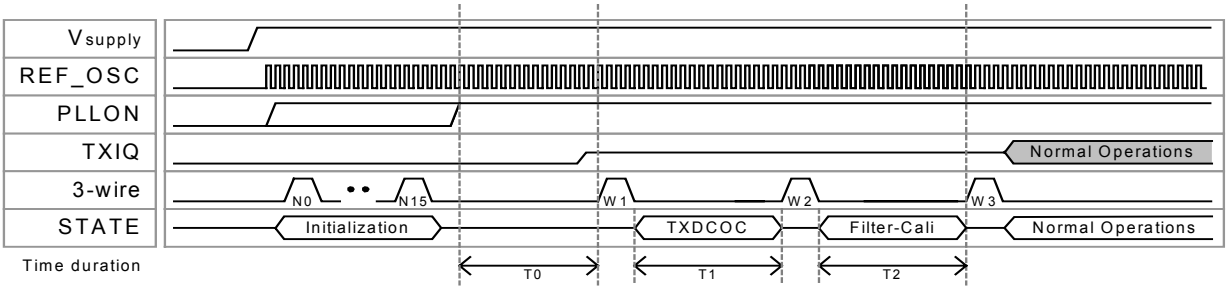


FIGURE 1 Power On Calibration Timing Diagram

As described in the figure above, the initialization process is taken after the supply voltage turned on. The default register values N0~N15 are fed via 3-wire interface. The PLLON could be either HIGH or LOW during the initialization procedure.

After the PLLON pulls HIGH, a PLL locking time T0 with at least 150us is required before the first calibration procedure. The TXIQ pins should be kept at common mode DC level (without modulated signal) during the calibration procedure. Then the calibration steps are executed with corresponding 3-wire data W1 and W2. Each step begins when the 3-wire data latched, and stops when the next 3-wire data loaded. The duration of each process should be longer than 30us, that is, T_K > 30us for K=1~2.

The last 3-wire data, W3, is loaded after the calibration steps, and AL2230 is then ready for normal operations.

Register Value for W1~W4		Minimum Settle Time for T0~T4	
W1	0x00D80F	T0	150 us
W2	0x00780F	T1	30 us
W3	0x00580F	T2	30 us

7 3-Wired Interface

The control kernel consists of registers and logic gates to control the transceiver. The signals of three wire serial interface, <CLK>, <DATA>, and <LE>, can communicate data in 20-bit words. MSB is transmitted first. The synchronic clock reference comes from <CLK>. After 20-bit data are streamed, <LE> is pulled high to latch the data while data streams out in parallel. Detailed timing, electrical parameters and the registers control table are shown as below.

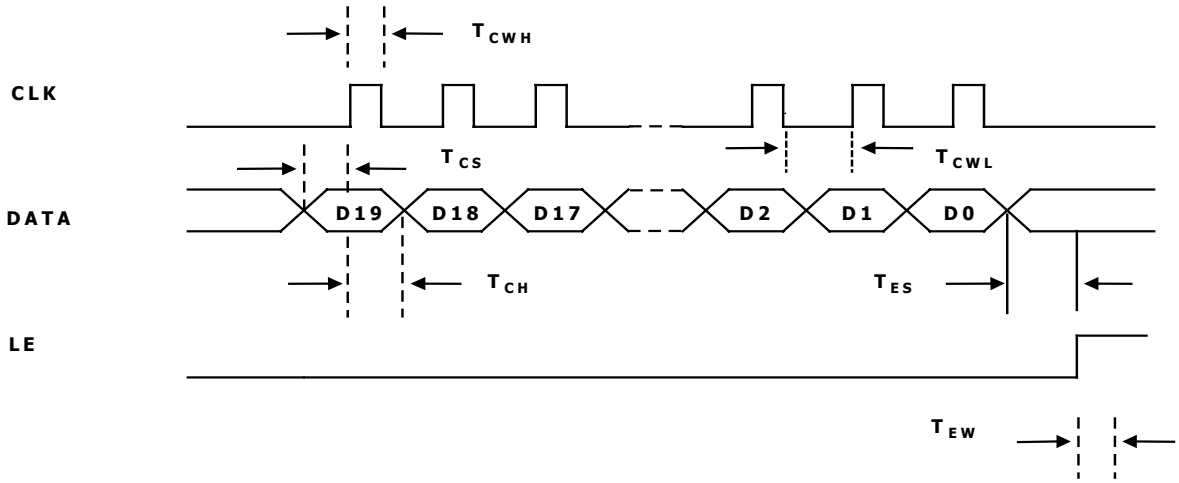


FIGURE 2 Serial Bus Data Timing Diagram

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_{CS}	Settling time	20			ns
T_{CH}	Hold time	10			ns
T_{CWH}	Pulse width (high)	20			ns
T_{CWL}	Pulse width (low)	20			ns
T_{ES}	Load enable setup time	20			ns
T_{EW}	Load enable pulse width	40			ns

TABLE 1 Serial Bus Parameters

9 Absolute Maximum Ratings

AL2230 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (Vcc)	-0.3V	4.0V
Pin voltage	-0.3V	Vcc + 0.3V
Maximum power dissipation	-	2W
Operating temperature	-40°C	+85°C
Storage temperature	-65°C	+150°C
LNA input level	-	+10 dBm
PA output load mismatch	-	10:1

TABLE 3 Absolute Maximum Ratings

9.1 DC Specifications

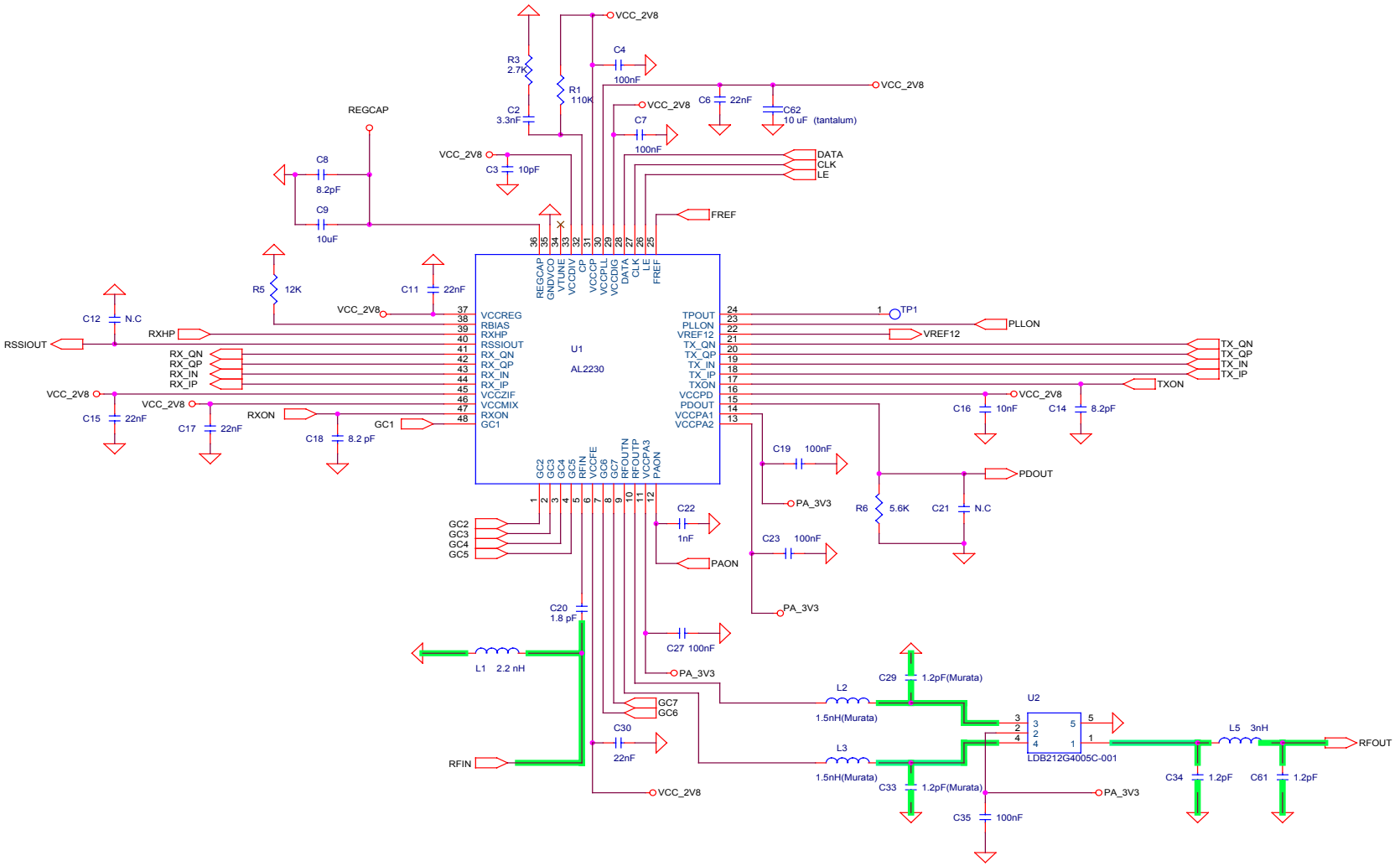
Typical values are at VCC=3.3V(PA)/2.8V(TRX), Ta=25 °C unless otherwise specified

Item	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Power Amplifier	3	3.3	3.6	V
	Transceiver (V_{DD})		2.8		
Digital input voltage	Logic High (V_{IH})	$0.7V_{DD}$		V_{DD}+0.3	V
	Logic Low (V_{IL})	-		$0.3V_{DD}$	
Shut down current	PLLON=L, PD1=PD2=1		5*		μA
	PLLON=L, PD1=PD2=0		800		
Standby current	PLLON=H		56		mA
Rx current	PLLON=RXON=H		94		mA
Tx current	PLLON=TXON=H		92		mA
	PLLON=TXON=PAON=H		276 / 298**		

TABLE 4 DC Specifications

*note: About 1ms recovery time is required when PD1 & PD2 is set from 1 back to 0.
**note：276mA under Pout 16dBm OFDM mode, 298mA under Pout 19dBm CCK mode.

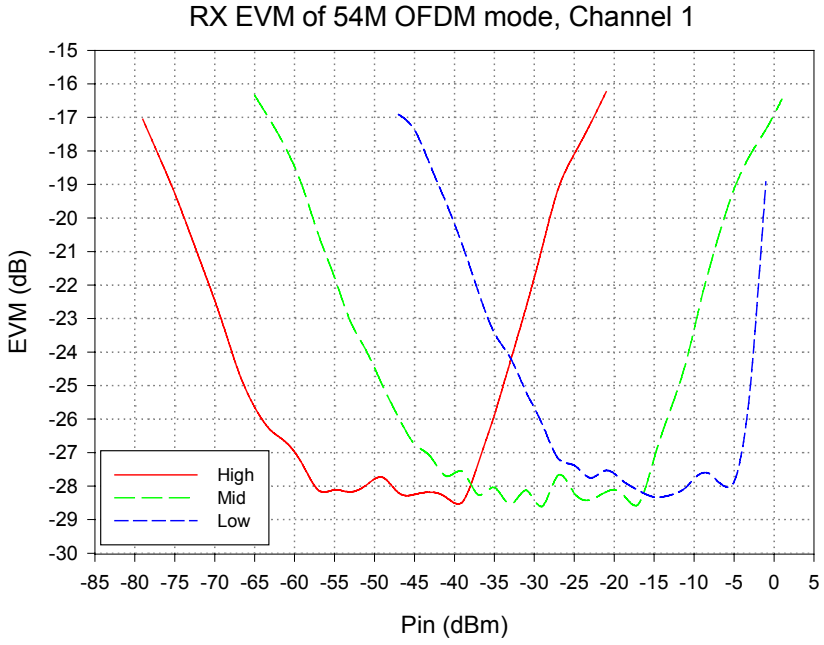
10 Application Circuit

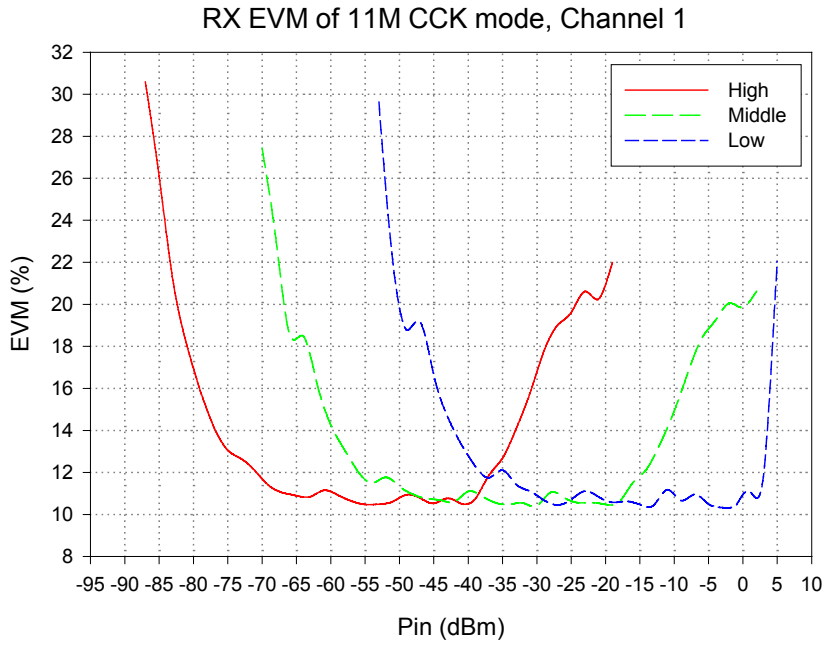

VCC_2V8
R3
2.7K
R1
110K
C4
100nF
C2
3.3nF
C6
22nF
C62
10 uF (tantalum)
C7
100nF
REGCAP
C8
8.2pF
C3
10pF
DATA
CLK
LE
C9
10uF
FREF
R5
12K
C11
22nF
C12
N.C
RSSIOUT
RXHP
RX_QN
RX_QP
RX_IN
RX_IP
C15
22nF
C17
22nF
RXON
GC1
C18
8.2 pF
U1
AL2230
VCCREG
RBIAS
RXHP
RSSIOUT
RX_QN
RX_QP
RX_IN
RX_IP
VCCIF
VCCMIX
RXON
GC1
REGCAP
GNDVCO
VTUNE
VCDIV
CP
VCCP
VCCPLL
VCCDIG
DATA
CLK
LE
FREF
TPOUT
PLLON
VREF12
TX_QN
TX_QP
TX_IN
TX_IP
TXON
VCCPD
PDOUT
VCCPA1
VCCPA2
TP1
PLLON
VREF12
TXON
C16
10nF
C14
8.2pF
C19
100nF
PA_3V3
R6
5.6K
C21
N.C
PDOUT
C23
100nF
PA_3V3
GC2
GC3
GC4
GC5
C22
1nF
PAON
C20
1.8 pF
L1
2.2 nH
C27
100nF
PA_3V3
GC7
GC6
C30
22nF
RFIN
L2
1.5nH(Murata)
C29
1.2pF(Murata)
L3
1.5nH(Murata)
C33
1.2pF(Murata)
C35
100nF
PA_3V3
U2
LDB212G4005C-001
L5
3nH
C34
1.2pF
C61
1.2pF
RFOUT

11 Measurement Data

RX :

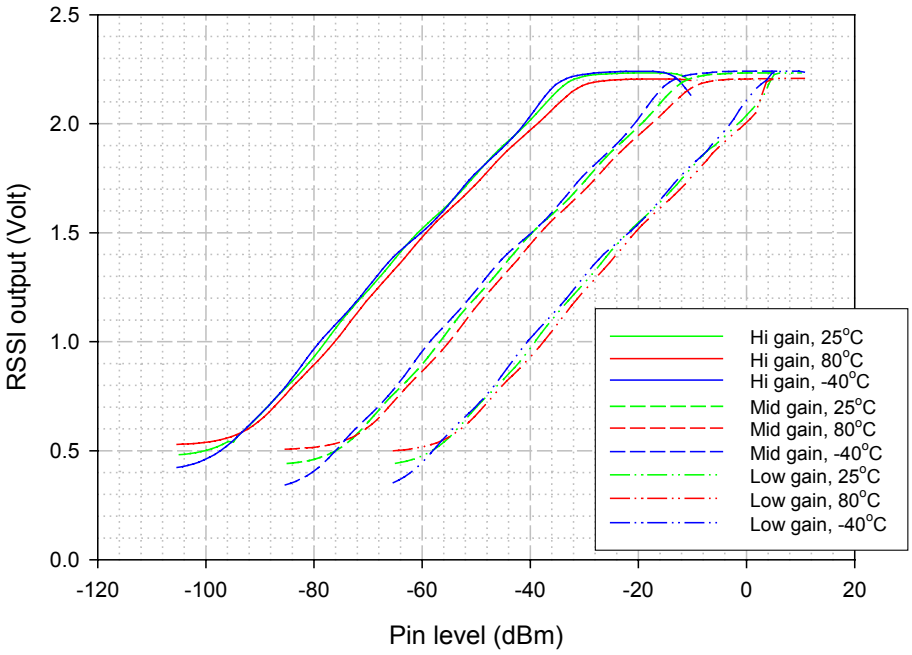
1. EVM vs. Input Power – The received signal's EVM vs. input power level is plotted with different LNA gain levels (High / Middle / Low gain).



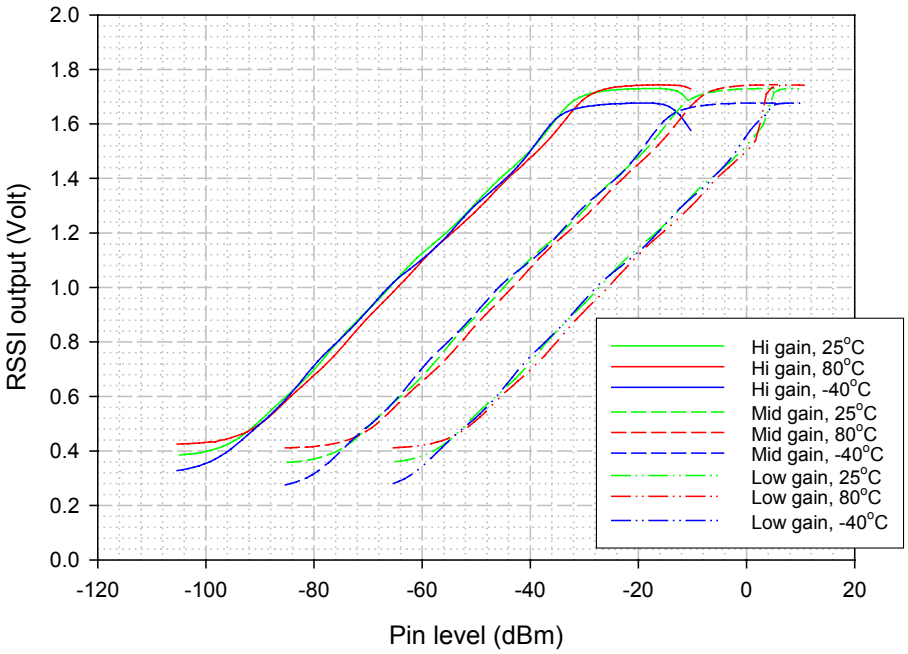


2. RSSI output voltage vs. Input Power – The RSSI voltage vs. input power level is plotted with different LNA gain levels (High / Middle / Low gain) and temperatures (85°C / Room Temp / -40°C). The RSSI output voltage range is selectable: High Range (max. output voltage 2.4V) and Low Range (max. output voltage 2.0V).

RSSI output voltage vs. Pin level, High Range



RSSI output voltage vs. Pin level, Low Range

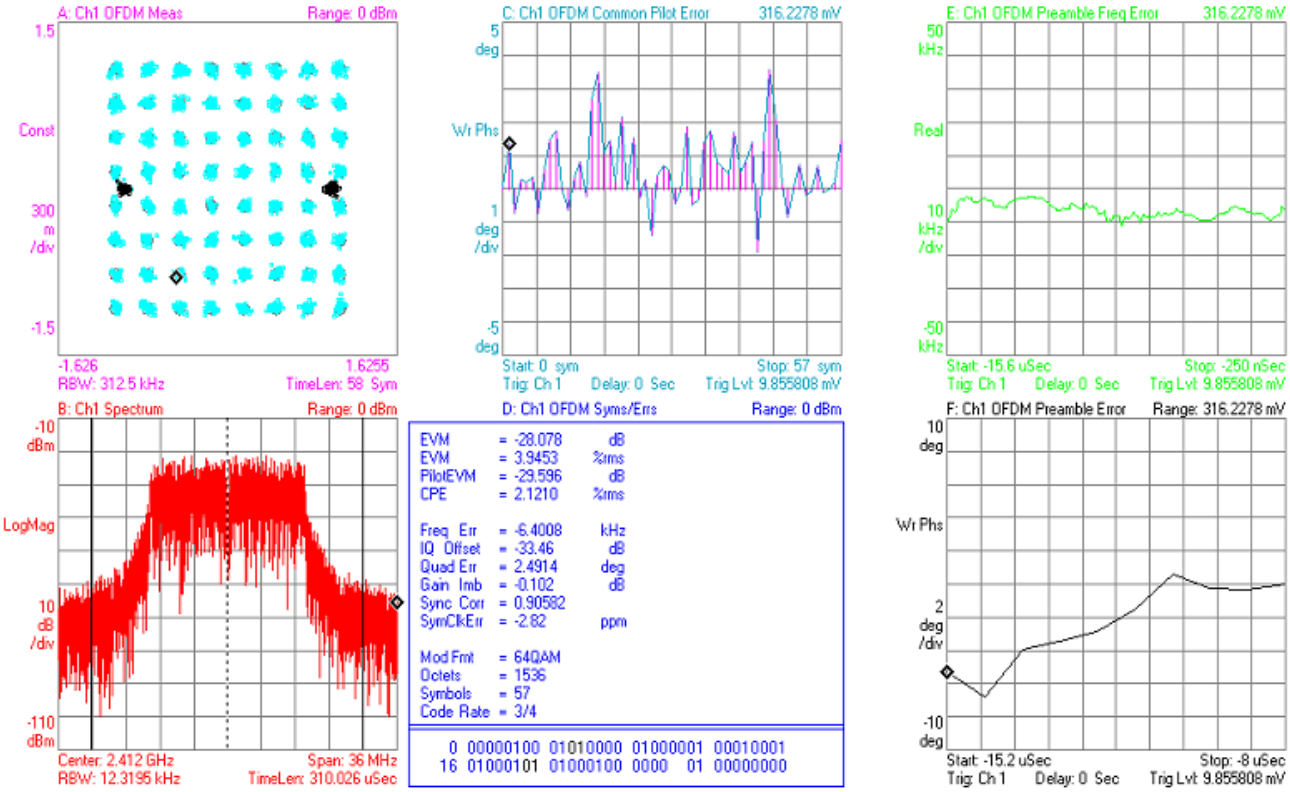


Note : The RSSI output voltage is proportional to the input signal power level in decibel, and is irrelative to RXGC setting when GC<5:1>=31~7. However, when GC<5:1>=6~0, the RSSI output voltage would drop 0.34V (for High range) or 0.25V (for Low range) under the same input signal power level. **The above RSSI curves are measured at GC<5:1>=7**.

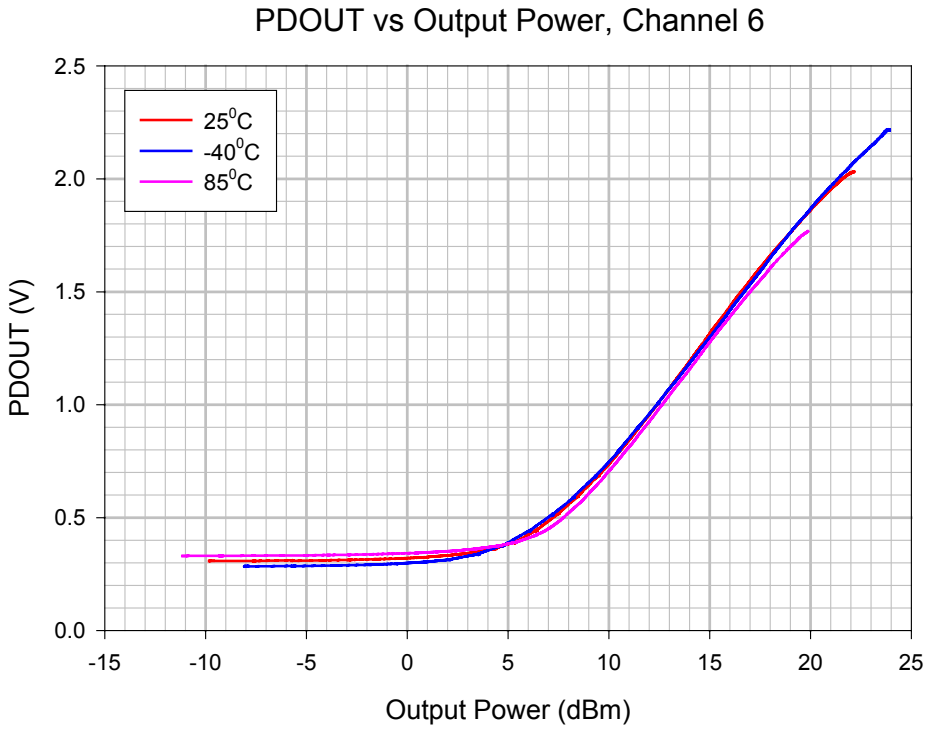
TX :

1. IQ constellation, Spectrum, EVM vs. Symbols, EVM measurements, Preamble Frequency Error and Preamble Phase Error (54 Mbps mode)

   Baseband TXIQ Input Level: 112mVrms(differential)
   Output Power Level: 16.1dBm
   EVM: -28.0dB (3.9%)

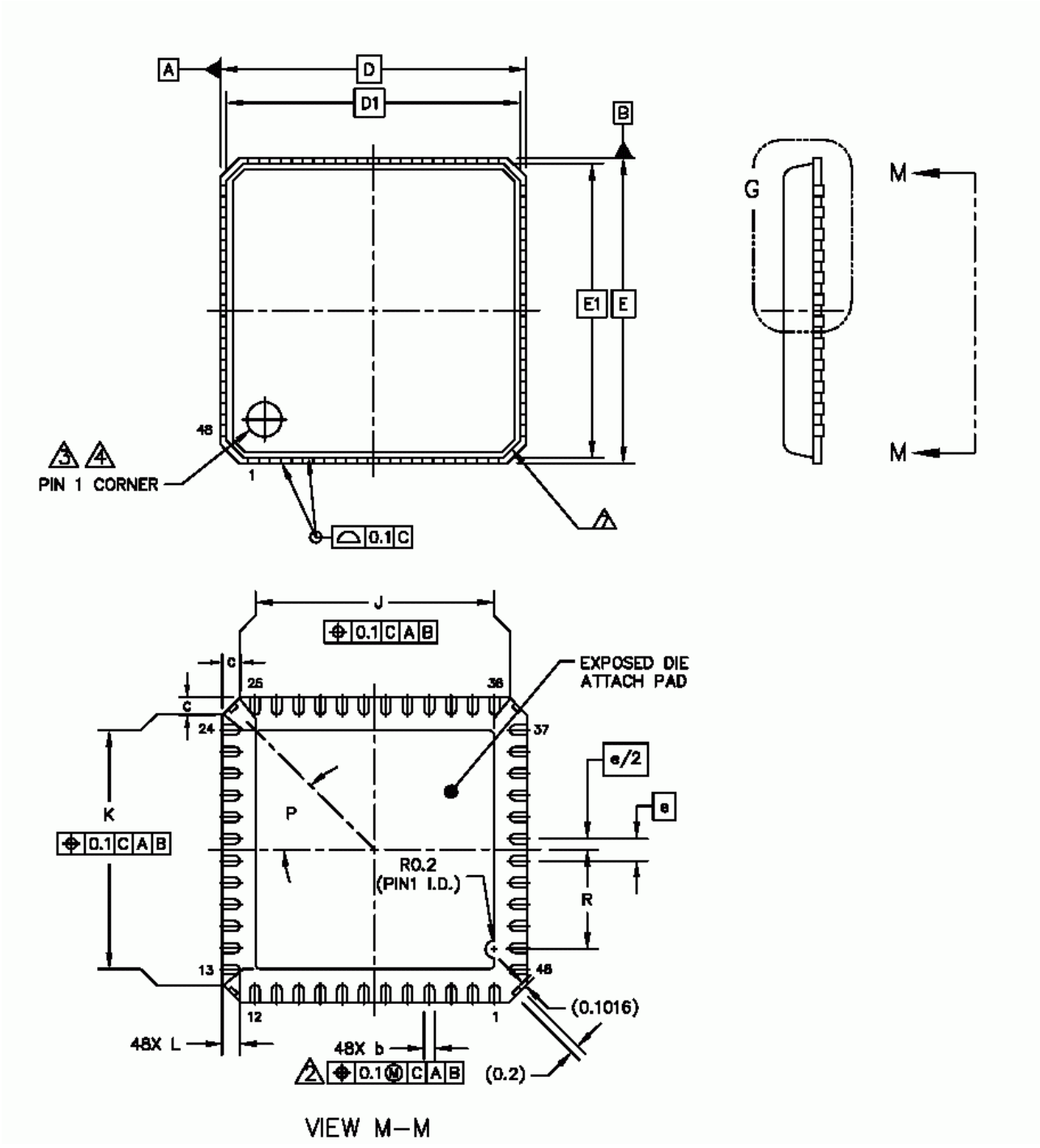


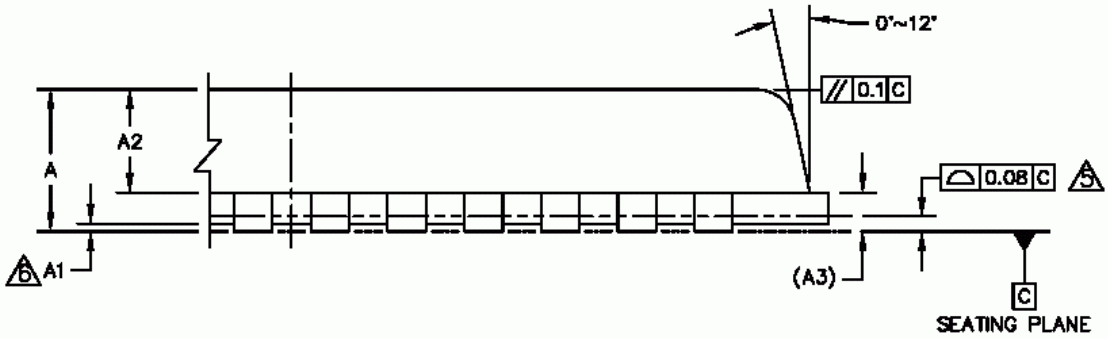
2. PDOut Voltage vs. Output Power



12 Package Dimensions

PUNCH QFN 48LD
7x7x0.9 PKG 0.5 PITCH POD





DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.576	0.615	0.654
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		7 BSC	
D1		6.75 BSC	
E		7 BSC	
E1		6.75 BSC	
e		0.5 BSC	
J	5.37	5.47	5.57
K	5.37	5.47	5.57
L	0.3	0.4	0.5
P		45° REF	
R	2.185	2.285	2.385

NOTES

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
6. APPLIED ONLY TO TERMINALS.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	JEDEC–MO–220–F