Technical Description

The Equipment Under Test (EUT), is a portable 2.4GHz Transceiver (Portable Controller Unit) for a RC monster. The operation frequency range is between 2423MHz and 2463MHz with following 4 channels used.

Channel	Frequency (MHz)
1	2423
2	2443
3	2458
4	2463

The EUT is powered by 3 x 1.5V AAA batteries.

After switching on the EUT, the monster will have sound function, recording function and walkie talkie function based on the switches pressed in the controller.

Antenna Type: Internal, Integral

The brief circuit description is listed as below:

1) U1 acts as MCU (GPCE4096A).
2) U2 acts as RF IC (UM2471).
3) Y1 (16.0MHz) acts as a crystal for U2.
4) U3 acts as Voltage regulator (GBY0029C).

Antenna Type: Internal antenna
Antenna Gain: 0dBi
Nominal rated field strength is 98.5 dBμV/m at 3m
Maximum allowed production tolerance: +/- 3dB

UM2471

Low Power 2.4 GHz Transceiver

Datasheet
DS-2471-01

Version: 0.4
Released Date: 2016/06/29

The content of this technical document is subject to change without notice. Please contact UBEC for further information.

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UM2471

Low Power 2.4 GHz Transceiver

Applications

- RF Remote Controller
- Interactive Wireless Toy and Game
- Wireless Audio/Video
- Wireless Consumer Electronics
- Wireless Keyboard Mouse

Introduction

The UM2471 is a 2.4 GHz Direct Sequence Spread Spectrum (DSSS) / Minimum-Shift Keying (MSK) RF transceiver with integrated baseband and MAC in a single chip. Targeting for the low cost and low power applications, the UM2471 is very suitable for toys, games, remote controller, PC peripherals and varieties of wireless consumer electronics.

The UM2471 supports multiple data rates of 125kbps OQPSK-DSSS, 250kbps OQPSK-DSSS, 1Mbps MSK, and 2Mbps MSK for flexible system design. For 125kbps OQPSK-DSSS, 250kbps OQPSK-DSSS, 1Mbps MSK and 2Mbps MSK, 16 MHz crystal is used. With the integrated medium access controller (MAC), UM2471 can largely reduce the loading of the host MCU and also reduce the development effort and time, especially for the wireless applications having more complicated network topology and large network nodes. The UM2471 is packaged in 3x3 mm^2 leadless 16-pin QFN package.

Features

RF/Analog

- Worldwide 2.4GHz ISM band operation
- -83 dBm sensitivity @ 2Mbps (MSK)
- -86 dBm sensitivity @ 1Mbps (MSK)
- -95 dBm sensitivity @ 250k (OQPSK-DSSS) (Packet error rate under 1%)
- -98 dBm sensitivity @ 125k (OQPSK-DSSS)
- 5 dBm maximum input level
- 6 dBm typical output power
- Integrated TX/RX switch
- 24 mA RX and 36 mA (6dBm output power) TX at 250k bps mode
- 0.9 uA at deep sleep mode
- 0.1 uA at power down mode
- Multiple data rates of 125Kbps/250Kbps with OQPSK-DSSS and 1Mbps/2Mbps with MSK
- 16-pin leadless QFN 3x3 mm^2 package

MAC/Baseband

- ❑ Automatic ACK with 2 byte programmable information
- ❑ **6 data pipes for 1:6 star networks**
- ❑ Trigger TX FIFO automatically after register wakeup
- ❑ Automatic FCS generation and FCS check
- ❑ Innovative and patented on-fly multi-rate detection
- ❑ 30-byte TX FIFO
- ❑ 32-byte RX FIFOs
- ❑ Various power saving modes
- ❑ Simple four-wire SPI interface

Table of Content

Abbreviations

ACK	Acknowledgement
ADC	Analog to Digital Converter
CCM	Counter Channel Mode
CRC	Cyclic Redundancy Check
DSSS	Direct Sequence Spread Spectrum
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
EVM	Error Vector Magnitude
FCF	Frame Control Field
FCS	Frame Check Sequence
FIFO	First In First Out
INT	Interrupt
ISM	Industrial Scientific and Medical
ITU-T	International Telecommunication Union - Telecommunication
I/O	Input / Output
I/Q	In-phase / Quadrature-phase
Kbps	Kilo bit per second
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit / Byte
MSB	Most Significant Bit / Byte
MAC	Medium Access Control
NA	Not Available
NC	Not Connected
O-QPSK	Offset-Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Locked Loop
QFN	Quad Flat No-lead Package
RF	Radio Frequency
RX	Receive
SPI	Serial Peripheral Interface
SFD	Start-of-Frame Delimiter
TBD	To Be Defined
TX	Transmit
VCO	Voltage Control Oscillator

Format Representations of Registers and Their Bits

1. SREG0xnn[m] or SREG0xnn[p:m]
   SREG: short register
   0xnn: register number
   nn: can be numerical numbers (for example:1, 2, or 3, etc) or alphabetical words (for example: A, B, or C, etc)
   [m]: the bit number
   [p:m]: bit m to bit p (for example: bit[7:5] means bit 7, bit 6, bit 5, and bit 4)

2. LREG0xnn[m] or LREG0xnn[p:m]
   LREG: long register
   0xnn: register number
   nn: can be numerical numbers (for example:1, 2, or 3, etc) or alphabetical words(for example: A, B, or C, etc)
   [m]: the bit number
   [p:m]: bit m to bit p (for example: bit[7:5] means bit 7, bit 6, bit 5, and bit 4)

1. Pin Configuration

1.1. Device Pin Assignments

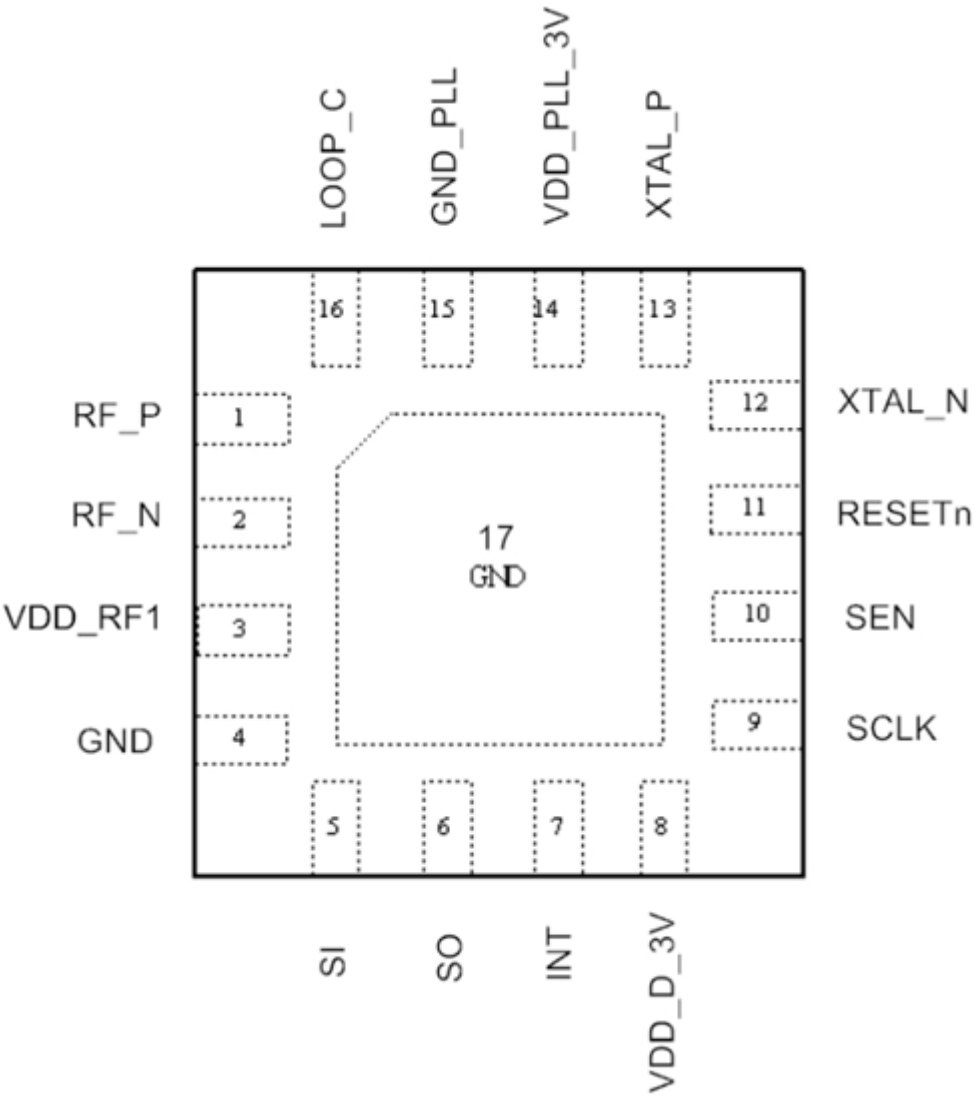


Figure 1. Pin Assignments (Top View)

1.2. Device Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, P = Power, I = Input, O = Output

Pin	Symbol	Type	Description
1	RF_P	AIO	Differential RF input/output (+)
2	RF_N	AIO	Differential RF input/output (-)
3	VDD_RF1	PI	RF power supply (1)
4	GND	Ground	Ground
5	SI	DI	Serial interface data input
6	SO	DO	Serial interface data output
7	INT	DO	Interrupt pin to the micro-processor
8	VDD_D_3V	PI	I/O PAD power supply (1)
9	SCLK	DI	Serial interface Clock
10	SEN	DI	Serial interface enable
11	RESETn	DI	Global hardware reset pin, active low
12	XTAL_N	AI	16 MHz Crystal (-)
13	XTAL_P	AI	16 MHz Crystal (+) (input for an external clock if needed)
14	VDD_PLL_3V	PI	RF power supply (1)
15	GND_PLL	Ground	Ground
16	LOOP_C	AI	PLL loop filter external capacitor. Connected to the external 39 pF capacitor.
17	IC Ground Pad	Ground	Backside ground plane. Must be connected to the ground.

Table 1. Pin Descriptions

* ***Caution***: ESD sensitive. Please refer to Section 2.5 for more information.

Note 1: Connecting bypass capacitor(s) to the pin as close as possible.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Storage temperature	**-40**	**+120**	℃
Supply voltage VDD pin to the ground	**-0.5**	**+3.6**	**V**
Voltage applied to inputs	**-0.5**	**VDD+0.5**	**V**
Short circuit duration, to GND, or VDD		**5**	**sec**

Table 2. Absolute Maximum Ratings

2.2. Recommended Operating Conditions

Test conditions: VDD = 3 V

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	**-20**		**+85**	℃
Supply Voltage for VDD	**2**	**3**	**3.6**	**V**
Logical high input voltage (for DI type pins)	**0.85 x VDD**			**V**
Logical low input voltage (for DI type pins)			**0.2 x VDD**	**V**

Table 3. Recommended Operating Conditions

2.3. DC Characteristics

Test conditions: T_A = 25℃, VDD_IO = 3 V

Parameter	Test Conditions	Min	Typ	Max	Unit
ACTIVE: TX	At 6 dBm output power (for all data rate)		36		mA
ACTIVE: RX	250K/2M bps Mode		24		mA
STANDBY	Sleep clock remains active. RF/MAC/BB, system clock shutdown.		2.0		uA
DEEP SLEEP	Registers and FIFOs remain active. All the other powers are shutdown		0.9		uA
Power down	Wake up circuit remains active. All power are shutdown. Register and FIFO data are not retained.		0.1		uA

2.4. ESD Characteristics

Human-body mode → All pins pass 2KV
Machine mode → All pins pass 200V

2.5. AC Characteristics

2.5.1. Receiver

Test conditions: TA = 25℃, VDD_IO = 3 V, LO frequency=2.445 GHz

Parameters	Test Conditions		Min	Typ	Max	Unit
RF frequency range			2400		2483.5	MHz
RF sensitivity	At antenna input signal PER≦1% (for 20 bytes paodload)	125Kbps		-98		dBm
		250Kbps		-95		dBm
		1Mbps		-86		dBm
		2Mbps		-83		dBm
Maximum RF input				5		dBm
Adjacent channel rejection	@+/-5 MHz, 250Kbps			20		dBc
Alternative channel rejection	@+/-10 MHz, 250Kbps			40		dBc

2.5.2. Transmitter

Test conditions: T_A = 25℃, VDD_IO = 3 V, LO frequency=2.445 GHz, 250 Kbps

Parameters	Test Conditions	Min	Typ	Max	Unit
RF frequency range		2400		2483.5	MHz
Maximum RF output power			6		dBm
Programmable output power range			20		dB
TX EVM for O-QPSK 125 / 250 Kbps modes			10		%

2.5.3. Synthesizer

Test conditions: T_A = 25℃, VDD = 3 V, LO frequency=2.445 GHz, 250 Kbps

Parameters	Test Conditions	Min	Typ	Max	Unit
PLL settle time			192		us
PLL programmable resolution			1		MHz

2.6. Power-on and External Reset Characteristics

The UM2471 has built-in power-on reset (POR) circuit which automatically resets all digital registers when the power is turned on. For stabilization of the complete circuit after the power-on reset, it is highly recommended to wait at least 3ms before starting the normal operation of the UM2471.

For external hardware reset (warm start), external reset pin RESETn is internally pulled high. The UM2471 will hold in reset state for around 20 us after RESETn is released from the low state.

2.7. Crystal Parameter Specifications

For 125kbps OQPSK-DSSS, 250kbps OQPSK-DSSS, 1Mbps MSK and 2Mbps MSK, 16 MHz crystal is used. The requirements of the crystal used by the 16 MHz crystal oscillator of UM2471 are listed in the table below.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		16		MHz
Frequency Offset	-40		40	ppm
*Load Capacitance			15	pF
*Recovery Time			350	usec

Table 4. Requirements for 16 MHz Crystal

*Notes: Different crystal vendor have different laod capacitance and different recovery time.

3. Functional Description

The UM2471 is composed of the following five blocks:

- PHY
- MAC
- Memory
- Power Management
- Interface

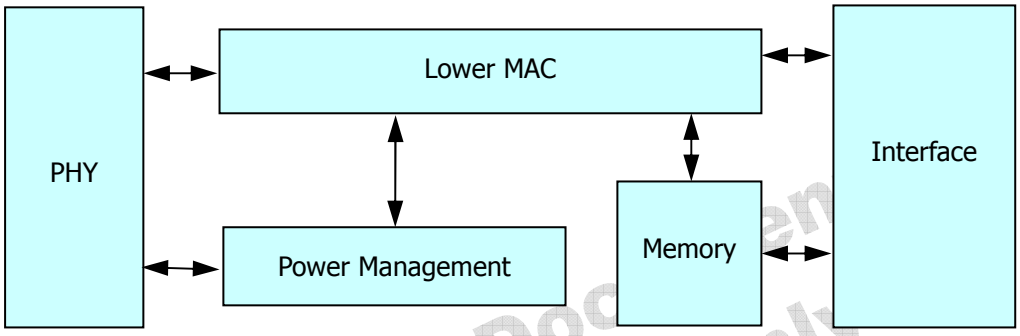


Figure 2. Block Diagram of UM2471

3.1. PHY

The architecture of PHY is shown in Figure 3.

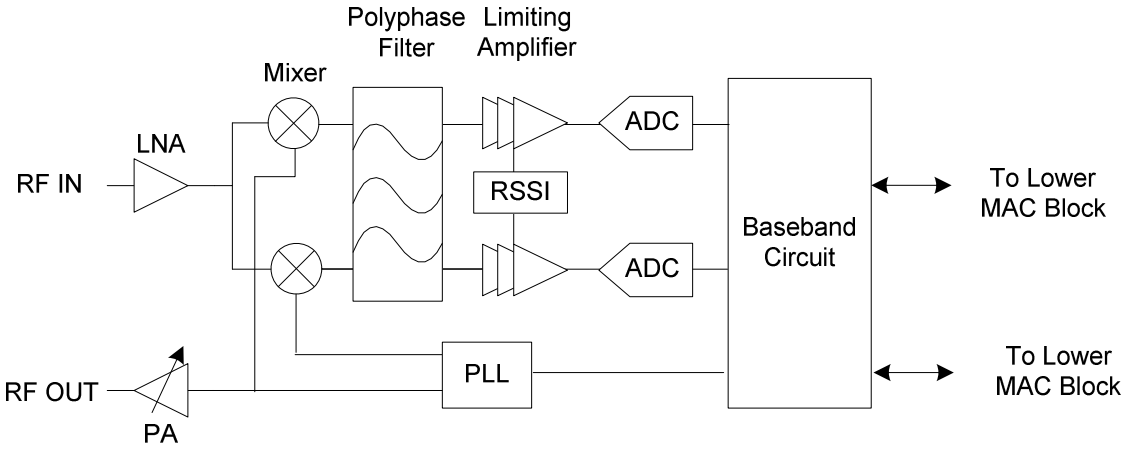


Figure 3. PHY Architecture

The key features of the UM2471 PHY are:

- RF frequency ranges from 2400 to 2483.5 MHz with 1MHz programmable resolution.
- Offset QPSK (O-QPSK) modulation with DSSS : 125kbps and 250kbps.
- Minimum-Shift Keying (MSK) : 1Mbps, and 2 Mbps
- Innovative and patented on-fly multi-rate detection

For all MSK modes, 4:32 spreading codes of DSSS are used for PHY header including preamble, SFD and Frame Length (FL) but no spreading codes are used for the PHY payload data. The transmission rate of the un-spreading PHY payload data bits is 8 times of PHY header. Thus the data rate of MSK modes is 8 times than OQPSK-DSSS modes.

The 125Kbps OQPSK-DSSS mode and the 1Mbps MSK mode have the same chip rate 1Mcps and occupy an RF channel bandwidth of 1MHz.The 250kbps OQPSK-DSSS mode and the 2Mbps MSK mode have the same chip rate 2Mcps and occupy an RF channel bandwidth of 2MHz.
The UM2471 PHY provides on-fly multi-rate detection function. The UM2471 PHY provides on-fly multi-rate detection function to permit multi-rate transmission and on fly detection of transmission rate. The UM2471 PHY comprises the transmitter configured to set a predetermined bit in the PHY header of the transmission frame to indicate whether the transmission frame is encoded by OQPSK-DSSS encoding mode or by MSK encoding mode and the receiver configured to decode the received transmission frame according to whether the predetermined bit in the PHR of the received transmission frame indicates the received transmission frame is encoded by OQPSK-DSSS encoding mode or by MSK encoding mode. The 8th digit bit of the frame length is used to identify which modulation is used in PHY payload data. By detecting whether the 8th digit bit of the frame length is a 0 or a 1 on the fly, the receiver distinguishes between the OQPSK-DSSS mode and the MSK mode and determines whether 4:32 spreading codes of DSSS is being used without predefining which mode is used.

The packet includes a 6-byte PHY header and a 6~31-byte PHY payload. The 6-byte PHY header includes 4 bytes of preamble, 1 byte of SFD, and 1 byte of frame length. Preamble and SFD are used for receiver packet detection and synchronization. The FL field specifies the length of the PHY payload. The length is valid from 6 to 31 bytes. The 8th bit of FL field is used for indicating OQPSK-DSSS mode when the 8th bit is a 0, and MSK mode when the 8th bit is a 1. The frame format is as below:

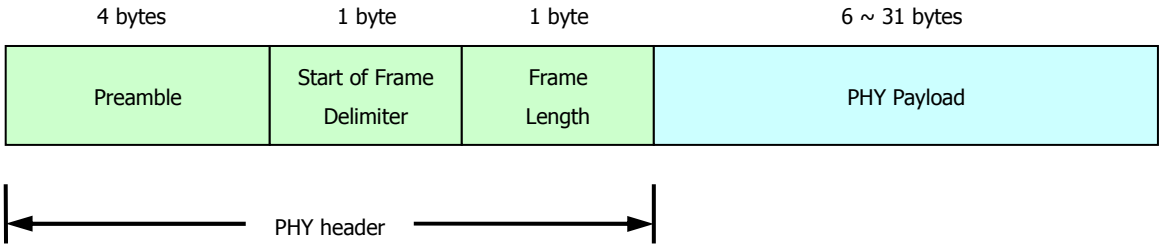


Figure 4. PHY Layer Frame Format

3.2. MAC

The UM2471 MAC provides plenty of hardware-assisted features to relieve the loadings of the host MCU. Not only providing the reliable wireless packet communication between two nodes, it also handles data and command transfer between the network layer and the physical layer automatically.

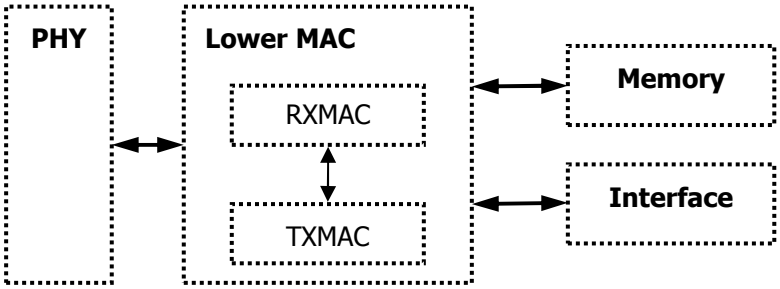


Figure 5. MAC Block Diagram

3.2.1. MAC Frame Format

Data Frame

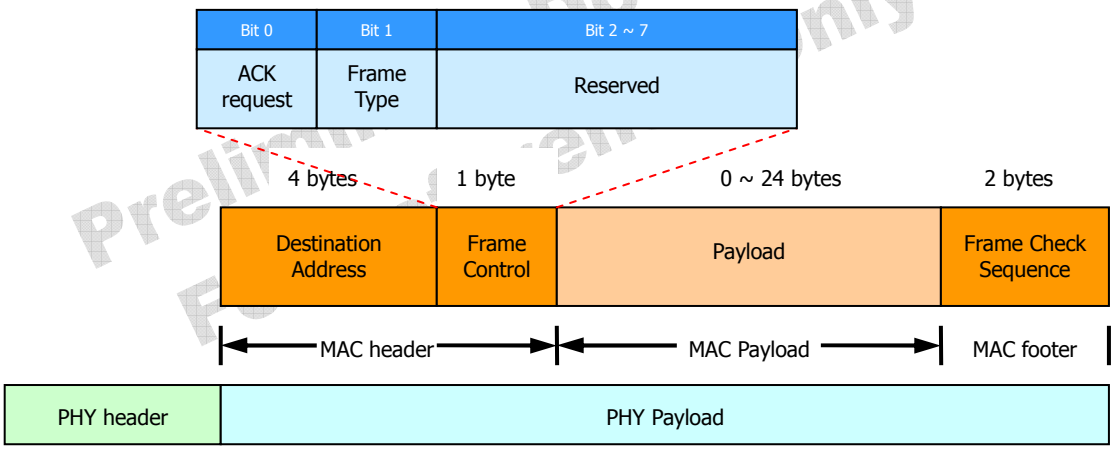


Figure 6. Data Frame Format

The address field contains the broadcast address (0xffff-ffff) or destination address. The bit 0 of frame control (FC) field is used for Ack-Request which specifies whether an acknowledgement is required from the recipient device. If the bit is '1', the recipient device shall send an acknowledgement frame back after determining that the received frame is valid. The bit 1 of FC field is '0' for data frame. The length of payload field is variable from 0 to 56 bytes. The frame check sequence (FCS) is calculated over the address field, FC field and the payload. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

Acknowledgement Frame

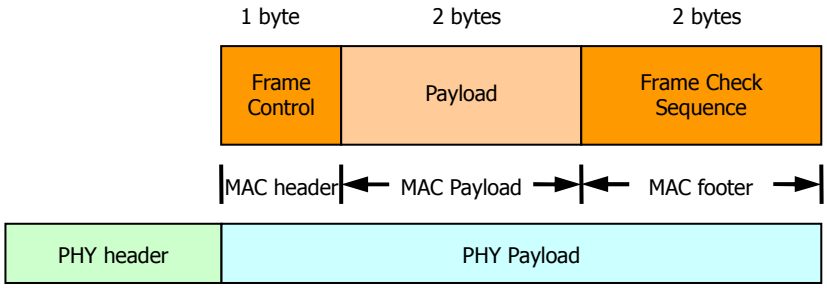


Figure 7. Acknowledgement Frame Format

The length of acknowledgement frame is always 5 bytes. Bit 1 of FC field is '1' for ACK frame. The payload field, containing user information of acknowledgement frame, can be configured by SREG0x03 and SREG0x04. The FCS is calculated over the FCS of the received packet, FC field and the payload field. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

3.2.2. Destination address

The destination address is 4-byte address for the receiver. An address ensures that the packet is detected by the target receiver. The RX device can open up to six data pipes to support up to six TX devices with unique addresses. All six TX device addresses are searched simultaneously. In RX side, the data pipes are enabled with the bits in the PIPEN(SREG0x1A) register.

By default only data pipe 0 and 1 are enabled. Each pipe can have up to 4 bytes configurable address. Data pipe 0 has a unique 4 byte address. Data pipes 1-5 share the 3 most significant address bytes. The LSB byte must be unique for all 6 pipes.

3.2.3. TXMAC

When the TXFIFO is triggered, the TXMAC gets the data from TXFIFO to generate a 16-bit FCS and sends the packet to the PHY layer of the TX immediately. TXMAC can also handle the retransmission when the acknowledgement packet is not received. The block diagram of the TXMAC is shown in Figure 8 below.

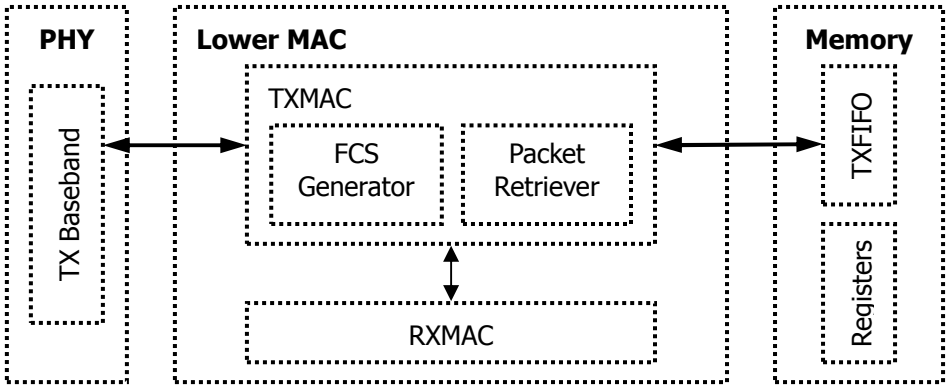


Figure 8. TXMAC Block Diagram

3.2.4. RXMAC

UM2471 RX PHY filters signals and tracks the synchronization symbols. If a packet passes the filtering, RXMAC performs frame type parsing, address recognition and FCS checking. If the destination address is broadcast address or matches its own identity, configured by SREG0x05 to SREG0x08, and the FCS check is passed, an interrupt is issued at SREG0x31[3] to indicate a valid packet is received. Meanwhile, the frame length field of PHY header and PHY payload will be stored in RXFIFO. Unqualified packets are skipped.

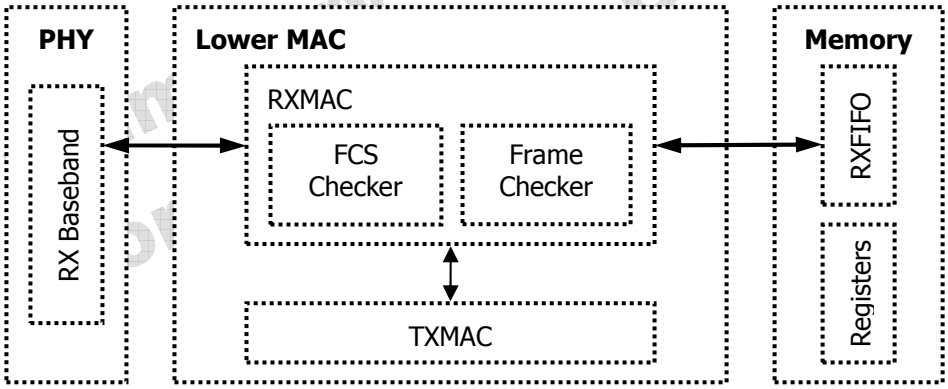


Figure 9. RXMAC Block Diagram

The contents of the RXFIFO can be flushed only by the following three ways: (1) the MCU host reads length field of RXFIFO and the last byte of the packet, (2) the host issues an RX flush, and (3) the software reset by SREG0x2A[0]. Note that RXFIFO is ready to receive next packet and all the data in RFIFO will be overwritten after RXFIFO flushed.

3.2.5. Auto Acknowledgement

The RXMAC supports automatically acknowledgement. If and only if the packet is successfully received and an Ack-Request bit, Bit 0, in the FC field of the received packet is set, RXMAC informs TXMAC to send an acknowledgement packet automatically. User should write the FC field correctly into the TX FIFO.

If an acknowledgement is requested and the replied ACK frame is not received, the transmitter automatically resends the packet until the maximum retransmission times, specified in SREG0x1B[7:4], are reached. To utilize the function properly, the corresponding registers of both transmitting and receiving sides need to be set correctly.

Auto-retransmission on TX Side

To automatically retransmit a packet when an ACK is not received, SREG0x1B[2] is required to be set to '1'.

Auto-acknowledgement on RX Side

To automatically reply an ACK packet when Ack-Request bit is set to '1', SREG0x00[5] should be set to '0'.

3.3. Memory

The memory block of the UM2471 is implemented by the SRAM. It is composed of registers and FIFOs, which can be accessed by the SPI interfaces. They are categorized into two kinds of address spaces. One is the short address space; the other is the long address space.

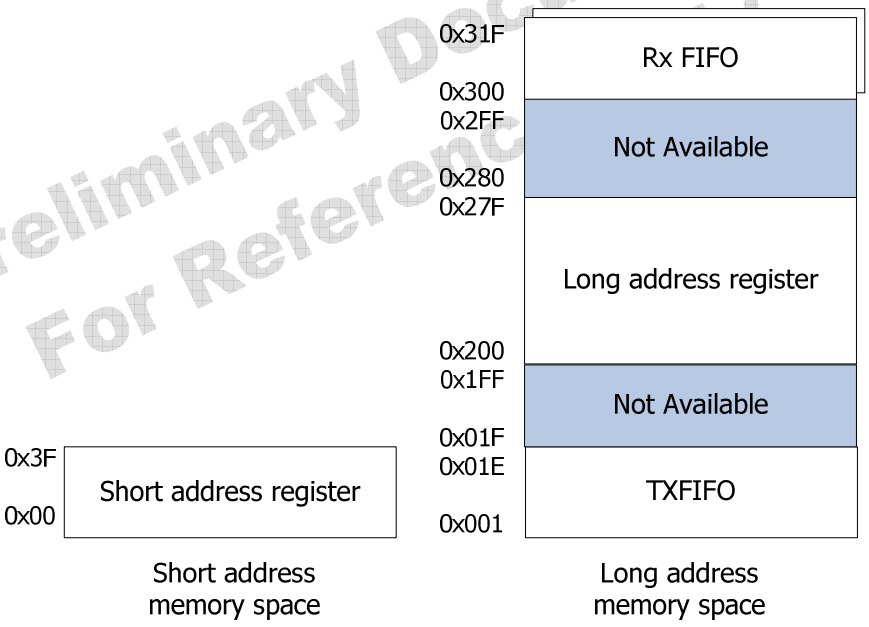


Figure 10. Memory Space Diagram

Registers

- Short address register (6-bit short addressing mode register)
- Long address register (10-bit long addressing mode register)

FIFOs

- TX FIFO – (30 bytes)

- RX FIFO – (32 bytes)

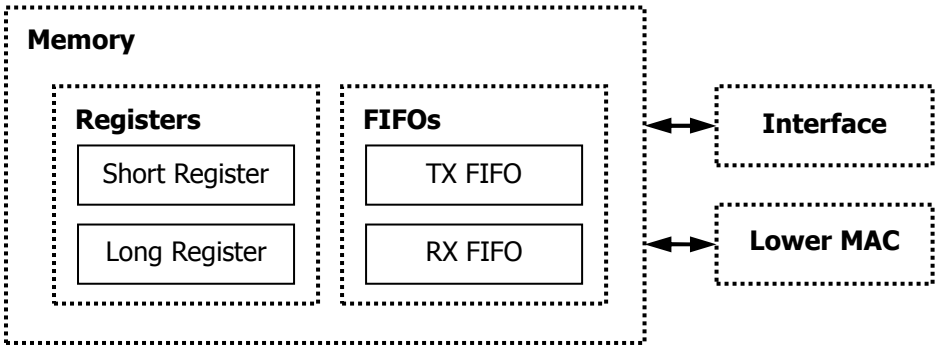


Figure 11. Memory Block Diagram

3.3.1. Registers

Registers provide control bits and status flags for the UM2471 operations, including transmission, reception, interrupt control, MAC/baseband/RF parameter settings …etc.

Short address registers are accessed by short addressing mode with valid addresses ranging from '0x00' to '0x3F'. Long address registers are accessed by long addressing mode with valid addresses ranging from '0x200' to '0x27F'. Short registers are accessed faster than long registers. Please refer to Section 3.5.1 for detailed addressing rules for SPI interface.

3.3.2. FIFOs

FIFOs serve as the temporary data buffers for data transmission and reception. Each FIFO holds only one packet at a time. TXFIFO, the transmission FIFO, is composed of 30-byte FIFO. RX FIFO, the receiving FIFO, is composed of a 32-byte FIFO.

TXFIFO

The TXMAC gets the to-be transmitted data from the 30-byte TXFIFO. The memory space of TXFIFO is from '0x001' to '0x01E' and contains a FL field, address field, FC field and payload field. The FL field indicates the length of the address field, FC field and the payload field. The valid value of frame length is from 5 to 29 bytes. The value of the FL field of PHY header is calculated by adding the above mentioned value and the length of FCS field of MAC frame, i.e. 2, up. Below figure shows the TXFIFO format.

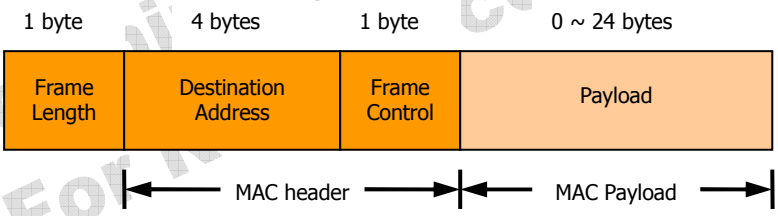


Figure 12. TXFIFO Format

RXFIFO

A RXFIFO is composed of a 32-byte FIFO to store the incoming packet. Each of them is designed to store one packet at a time. RXFIFO contains a FL field, address field, FC field, payload field and FCS field. The memory space of RXFIFO is from '0x300' to '0x31F'. The FL field, which is extracted from the PHY header, indicates the length of the address field, FC field, the payload field and FCS field. The valid value of frame length is from 7 to 31 bytes. Figure 13 shows the RXFIFO format.

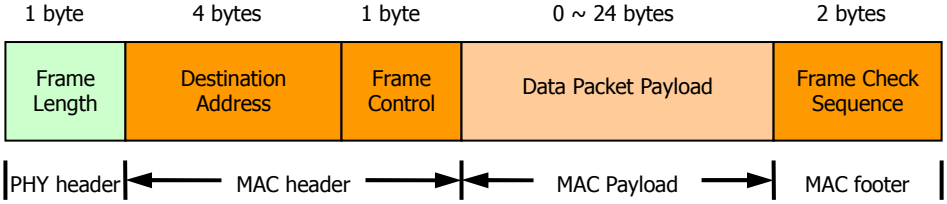


Figure 13. RXFIFO Format

3.4. Power Management

Almost all wireless sensor network applications require low-power consumption to lengthen battery life. Typical battery-powered device is required to be operated over years without replacing its battery. The UM2471 achieves low active current consumption of both the digital and the RF/analog circuits by controlling the supply voltage and using low-power architecture.

The UM2471 has four power saving modes that will be further described in Section 3.4.4. For ultra low-power operation, power-down mode is available which consumes around 1uA. All data stored in registers and FIFOs will be lost under power-down mode. In this mode, The UM2471 is able to wake up by an external reset (RESETn Pin11) signal. Except power-down mode, the data in the registers/FIFOs are retained during the other power saving modes.

3.4.1. Power Supply Scheme

The table below lists the recommended values of the external bypass capacitors for each power pin of the UM2471. For pin 1 and pin x, an extra bypass capacitor is needed for the decoupling purpose while the rest of the power pins require only one bypass capacitor. The path length between the bypass capacitors to each pin should be as short as possible.

Pin	Symbol	Bypass Capacitor 1	Bypass Capacitor 2
4	VDD_RF1	47 pF	10 nF
15	VDD_D_3V	10 nF	
18	VDD_PLL_3V	47 pF	

Table 5. Recommended External Bypass Capacitors

3.4.2. Battery Monitor

The UM2471 provides the function of monitoring the supply voltage so that the system can be alarmed when the supply voltage being lower than the threshold. The threshold can be configured by a four-bit register which is described in Section 4.9.

3.4.3. Power Saving Modes

Four power saving modes are supported by UM2471:

- STANDBY: RF/MAC/BB shutdown with the sleep clock and 16MHz clock remain active.
- DEEP_SLEEP: All powers are shutdown except the power to the digital circuits and register and FIFO data are retained.
- POWER_DOWN: All powers are shutdown. Register and FIFO data are not retained. An external reset signal is needed to wake up UM2471.

The difference between STANDBY mode and DEEP SLEEP mode is the power status of the sleep clock. To wake up UM2471, the host MCU has to control the time of sleep process.

The power management control is used for the low power operation of MAC and baseband modules. It manages to turn on and off the 16 MHz clock when the IC goes into power saving mode. By turning off the 16 MHz clock, the MAC and baseband circuits become inactive regardless whether their power supplies exist or not. All the digital modules are clock-gated automatically. That means only when a module is functioning, its clock would then be turned on. This approach efficiently decreases certain amount of the current consumption.

3.5. Interface

3.5.1. SPI

The slave SPI is supported for host MCU to read/write the control registers and FIFO of the UM2471. The features are as below:

- A simple 4-wire slave SPI (SO, SI, SCLK and SEN).
- Most significant bit (MSB) of all addresses and data transfers on the SPI is done first.

SPI Addressing Format

Bit 7 of addressing frame indicates the addressing mode of the packet. The length of address field is 6 or 10 bits for short and long addressing mode respectively. Bit 0 is a one-bit read/write indicator.

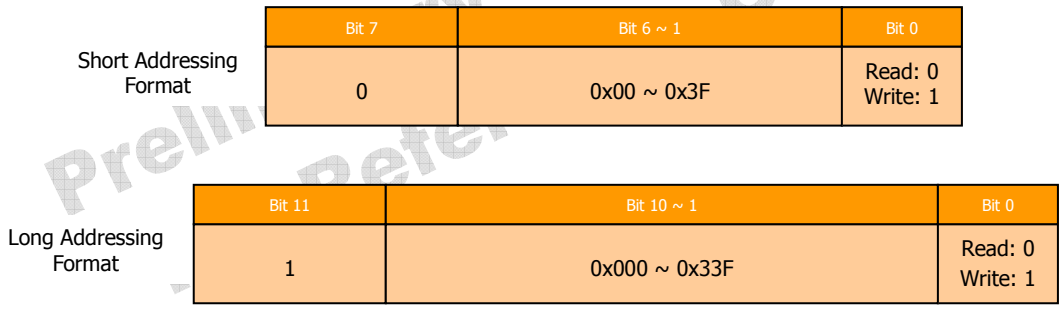


Figure 14. SPI Addressing Format

SPI Characteristics

Parameter	Symbol	Min	Max	Units	Conditions
***SCLK*, clock frequency**	F_{SCLK}		5	MHz	
***SCLK* low pulse duration**	t_{CL}	100		ns	The minimum time SCLK must be low.
***SCLK* high pulse duration**	t_{CH}	100		ns	The minimum time SCLK must be high.
***SEN* setup time**	t_{SP}	100		ns	The minimum time SEN must be low before the firs positive edge of SCLK.
***SEN* hold time**	t_{NS}	100		ns	The minimum time SEN must be held low after the last negative edge of SCLK.
***SI* setup**	t_{SD}	25		ns	The minimum time data must be ready at SI, before the positive edge of SCLK
***SI* hold time**	t_{HD}	25		ns	The minimum time data must be held at SI, after the positive edge of SCLK.
Rise time	t_{RISE}		25	ns	The maximum rise time for SCLK and SEN.
Fall time	t_{FALL}		25	ns	The maximum fall time for SCLK and SEN.

Table 6. SPI Characteristics

SPI Time Diagrams

Figure 15 and 16 shows the timing diagram for short and long addressing mode respectively. SPI master will initiate a read or write operation by asserting SEN to low, toggling SCLK and sent the address field by SI. The SEN should be high when a transaction is completed.

The SPI burst mode is provided for the access of long address memory space on a continuous basis. If SEN does not go high after the 8-bit write data and the SCLK continuously toggles, the followed 8-bit write data is written to next address field. Same for the read access, the data of the next address will be read. The SPI burst mode is only available for the long-address mode.

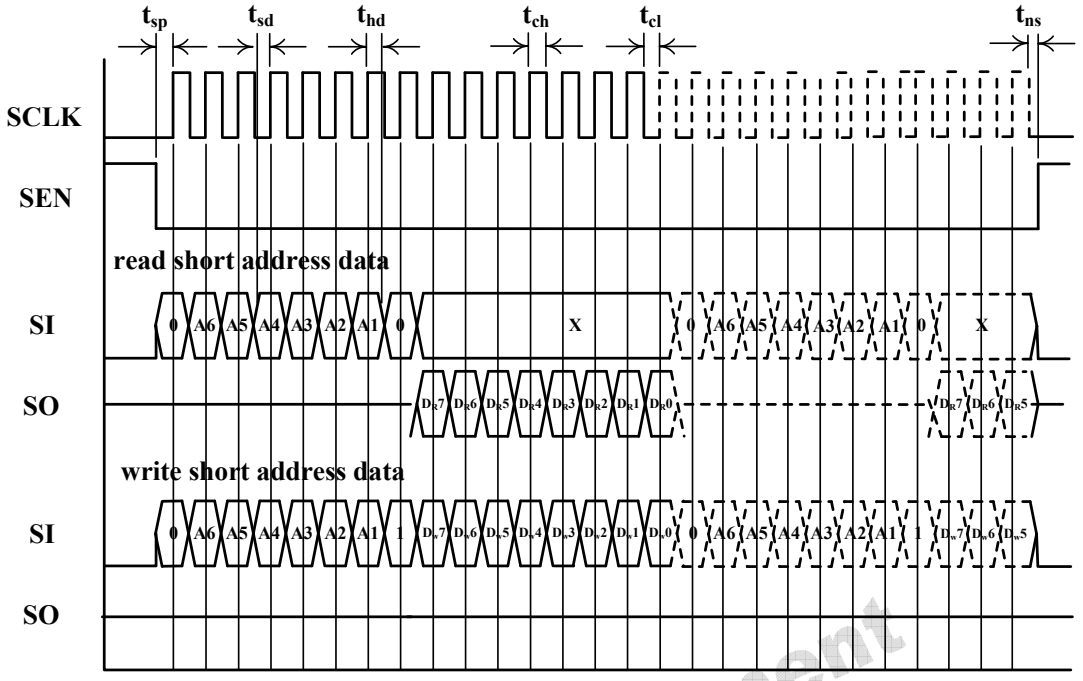


Figure 15. Timing Diagram of Short Addressing Mode

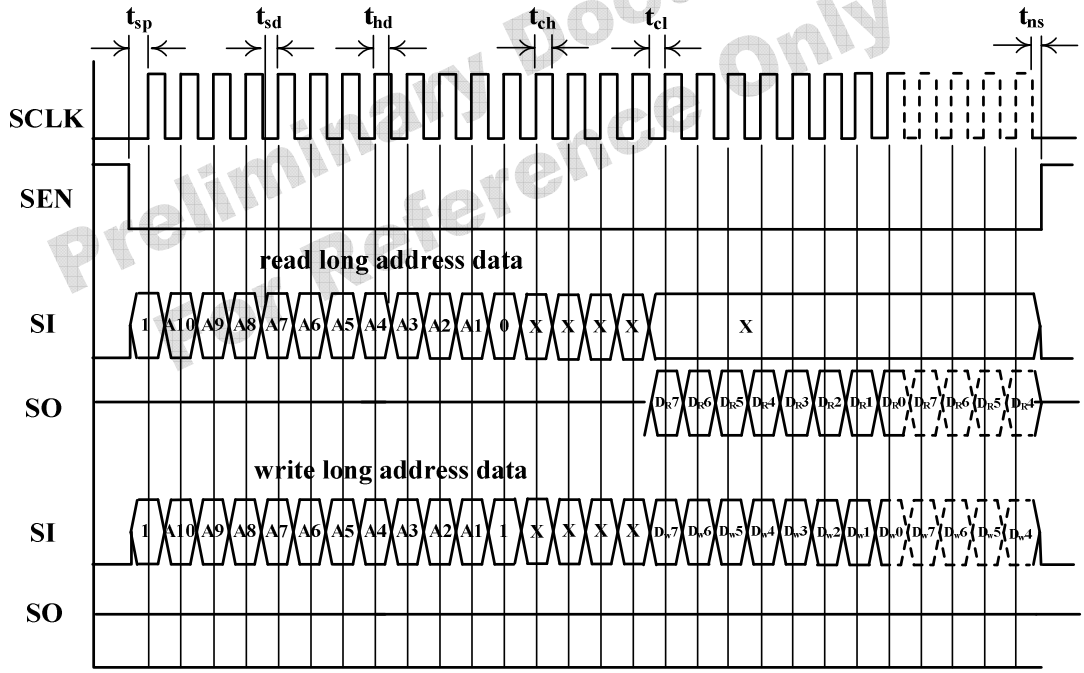


Figure 16. Timing Diagram of Long Addressing Mode

3.5.2. Interrupt Signal

The UM2471 provides an output interrupt pin (pin 6, INT) with selectable polarity. The UM2471 issues interrupts to the host MCU on three possible events. For each event, the UM2471 sets the corresponding status

bit in SREG0x31. If the corresponding interrupt mask in SREG0x32 is clear (i.e. equals '0'), an interrupt will be issued on pin 6. If it is set to '1' (masked), no interrupt will be issued, but the status is still present. Whenever SREG0x31 is read, the interrupt and the status are cleared. The three interrupt events are described as below:

Wake-up alert interrupt (WAKEIF)

Every time a wake-up event happens, the UM2471 issues the interrupt event.

Packet received interrupt (RXIF)

This interrupt is issued when an available packet is received in the RXFIFO. An available packet means that it passes an RXMAC filter, which includes frame type identifying, address filtering and FCS check.

TX FIFO release interrupt (TXNIF)

This interrupt can be issued in two possible conditions. The conditions are when a packet in TXFIFO is triggered and sent successfully, or when a packet is triggered and the retransmission is timed out.

4. Application Guide

4.1. Circuit Schematic

The reference circuit is shown as below figure 17-1 and figure 17-2.

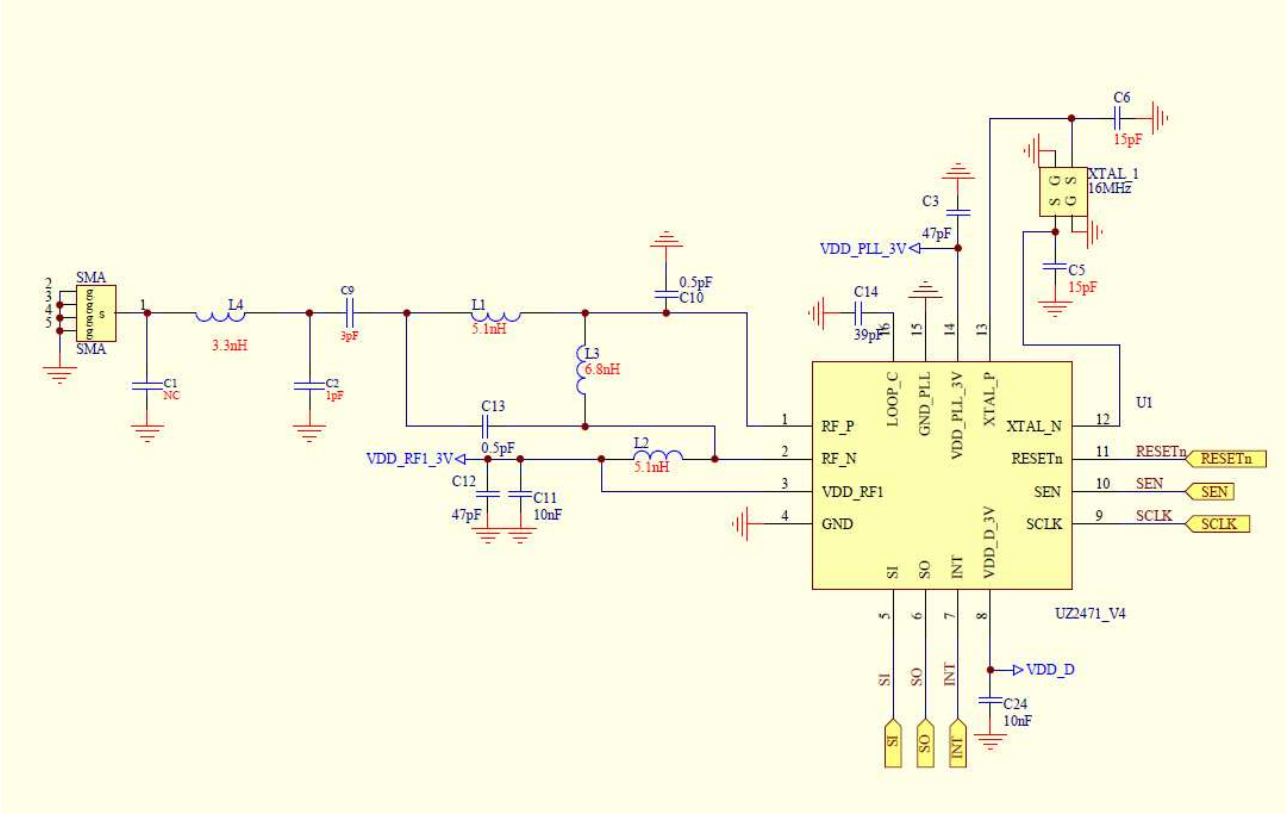


Figure 17-1. UM2471 Reference Circuit (#1)

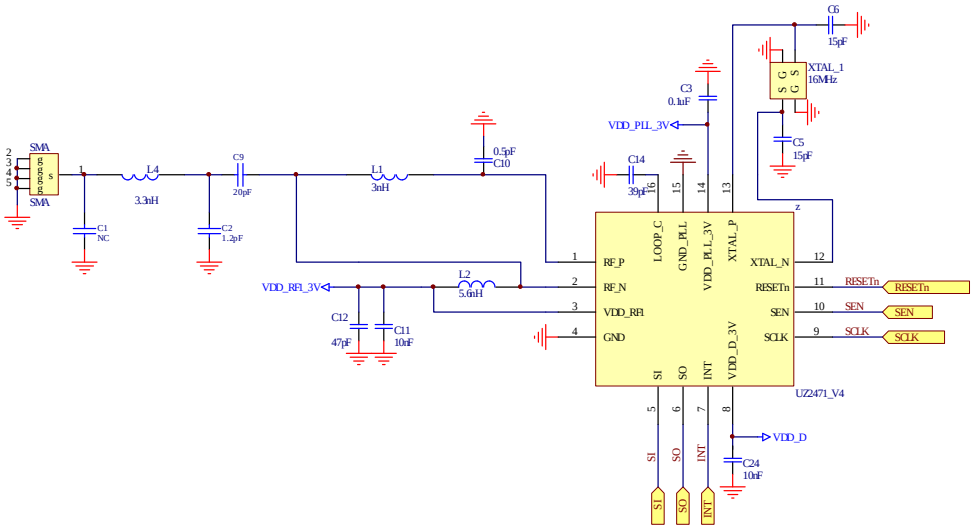


Figure 17-2. UM2471 Reference Circuit (#2)

4.2. Initialization

After UM2471 is powered on, some registers need to be configured before the data transmitting or reception. The procedure is described as below.

Mode	Address	Value(hex)	Descriptions	Note
SREG	0x2A	07		
SREG	0x38	80	Data Rate Select	125K bps
SREG	0x17	02	VCO Settling Time	
SREG	0x18	90	VCO Settling Time	
SREG	0x2E	C5	VCO Settling Time	
LREG	0x200	77	RF optimized control	6 dBm output
LREG	0x201	C3	RF optimized control	6 dBm output (125K)
LREG	0x207	D5	Loop Filter	
SREG	0x10	32	RF optimized control	2450MHz
SREG	0x32	00	Enable all interrupt	
SREG	0x35		16MHz clock recovery time	Ref 4.10.
LREG	0x259	58	RF optimized control	
LREG	0x22A	20	RF optimized control	
LREG	0x22B	10	RF optimized control	
Wait 110us				
LREG	0x200	F7	RF optimized control	
Wait **4ms**				
LREG	0x200	77	RF optimized control	
LREG	0x22B	00	RF optimized control	
LREG	0x22A	00	RF optimized control	
LREG	0x259	50	RF optimized control	

Different data rate setting as following table:

	Data rate			
Register	125K	1M	250K	2M
SREG0x38	0x80	0x81	0x82	0x83
LREG0x201	0xC3	0xC3	0xD3	0xD3
LREG0x206	0x70	0x70	0x72	0x72
LREG0x205	0x00	0x01	0x05	0x05

*Notes: If change data rate after initialization, it must do next calibration procedure.

Mode	Address	Register Name	Descriptions	Value(hex)	Note
LREG	0x259	RFCTL59	RF optimized control	58	
LREG	0x22A	RFCTL2A	RF optimized control	20	
LREG	0x22B	RFCTL2B	RF optimized control	10	
Wait 110us					
LREG	0x200	RFCTL00	RF optimized control	F7	
Wait **4ms**					
LREG	0x200	RFCTL00	RF optimized control	77	
LREG	0x22B	RFCTL2B	RF optimized control	00	
LREG	0x22A	RFCTL2A	RF optimized control	00	
LREG	0x259	RFCTL59	RF optimized control	50	

4.3. Change Channel

Set RF operation channel by configuring SREG0x10. UM2471 will go to RX state after 192us.

4.4. Interrupt

The UM2471 issues a hardware interrupt at pin 6 to the host MCU. There are two related registers that need to be set correctly. All the interrupts are masked (disabled) by default. The interrupt mask should be removed by setting SREG0x32 in advance. By default, the interrupt signal is sent to the host MCU as a falling edge after mask removed. The polarity can be configured by LREG0x211. The interrupt status can be read from SREG0x31 when it is triggered.

4.5. TX

For TX operation, the TXMAC of UM2471 automatically generates the preamble, Start-of-Frame delimiter and the FCS. The host MCU needs to write all other frame fields into TXFIFO. To send a packet in TX FIFO, there are several steps to follow:

Step 1.
Fill necessary data in TXFIFO. The format of TXFIFO is as follows:

Step 2.
Set Ackreq by SREG0x1B[2], if an acknowledgement / retransmission is required. The UM2471 automatically retransmits the packet till the number of the Max trial times specified in SREG1B[7:4] is reached, if there is no acknowledgement received.

Step 3.
By triggering SREG0x1B[0], the TXMAC will send the packet immediately. This bit will be automatically cleared.

Step 4.
Wait for the interrupt status shown in SREG0x31[0]. If retransmission is not required, SREG0x31[0] indicates the packet is successfully transmitted.

Step 5.
Check SREG0x24[0] to see if transmission is successful. SREG0x24[0]=0 means transmission successful and the ACK was received. The number of times of the retransmission can be read at SREG0x24[7:4]. SREG0x24[0]=1 means transmission failed and ACK was not received.

4.6. RX

When a valid packet is received, an interrupt is issued at SREG0x31[3]. The MCU host can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the frame length field and the last byte of RXFIFO are read, or when the host triggers a RX flush by SREG0x0D[0]. The format of RXFIFO is as follows:

4.7. Power Saving

Standby, Deep-Sleep and Power-Down modes are designed for UM2471. It is only allowed to switch between power saving modes and active mode. The following settings are effective in active mode only.

STANDBY Mode:

Shutdown RF/MAC/BB, while the voltage regulator, partial 16 MHz clock and sleep clock remains active.

- Set LREG0x277[5:4] to '00' to select for Standby mode
- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit

DEEP SLEEP Mode:

All power is shutdown except the power to the digital circuits and sleep clock. Register and FIFO are retained.

- Set LREG0x277[5:4] to '01' to select for Deep Sleep mode
- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit

POWER DOWN Mode:

All power is shutdown. Register and FIFO data are not retained. Initialization is needed after UM2471 back to active mode. Set LREG0x277[5:4] to '11' to select for Power Down mode

- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit
- Set LREG0x253[6:5] to '11' to connect the FIFO power and digital circuit power to ground

After the necessary settings mentioned above are configured, user can set SREG0x35[7]=1 to place UM2471 to power saving mode. After set SREG0x35[7]=1, the SEN Pin need to set to low (ground).

4.8. Wake-up

After entering into power saving mode, UM2471 could be waked up from STANDBY and DEEP_SLEEP modes by simply setting SREG0x22[7:6]='11'. UM2471 will issue wake-up interrupt SREG0x31[6] after wakeup operation completion. For POWER_DOWN mode, UM2471 can be waked up by using external reset pin (PIN11:RESETn).

Configure Clock Recovery Time

WAKECNT, used to calculate for recovery time of 16 MHz clock of UM2471, should be set in advance. User shall follow the following two steps to configure WAKECNT.

Step 1. Calculate the period of sleep clock:

Set LREG0x20B[4] to '1', then keep polling LREG0x20B[7] until the value becomes '1'. After the value of LREG0x20B[7] becomes '1', LREG0x20B[3:0], LREG0x20A, LREG0x209 form a 20-bit value C. Then the period of the sleep clock ($P_{sleepclock}$) can be calculated by the following equation:

$$P_{sleepclock} = \frac{62.5 \times C}{16}(ns)$$

Step 2. Configure WAKECNT to set the recovery time of 16 MHz clock to 350 us.

Set WAKECNT, { SREG0x37[7:0], SREG0x35[6:0]}, to (1000*350) / $P_{sleepclock}$. For example, the period of the sleep clock, $P_{sleepclock}$, is 10000 ns. Set { SREG0x37[7:0], SREG0x35[6:0]} to 0x23

4.9. Battery Monitor

Step 1.

Set the battery monitor threshold value at LREG0x205[7:4].

Step 2.

Enable the battery monitor by setting the LREG0x206[4] to the value '0'.

Step 3.

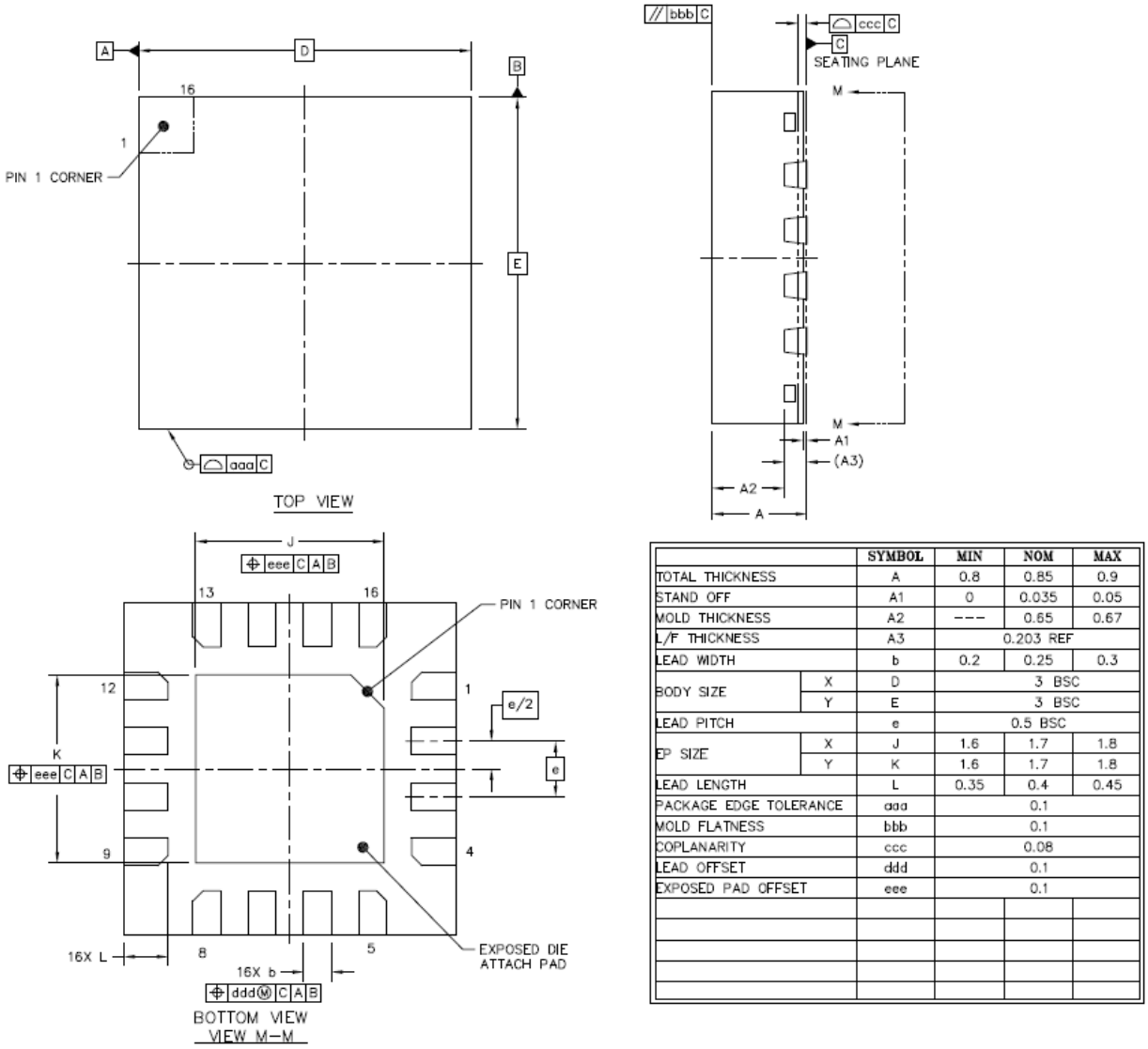
Read the battery-low indicator at SREG0x34[5]. If this bit is set, it means that the supply voltage is lower than the threshold.

5. Package Information

5.1. Package Drawing

The QFN-16 package outline is given below.

QFN-16, 3x3mm²



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	1.6	1.7	1.8
	Y	K	1.6	1.7	1.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

5.2. Package Soldering

5.2.1. Background

The UM2471 is housed in a small 16-pin lead-free QFN 3x3 mm^2 package. The packaged part passes the Level 3 pre-condition testing.

5.2.2. Reference Reflow Temperature Profile

Figure 18 is the reference temperature profile for the SMD IR reflow. Different equipments may have different optimized reflow conditions for maximum yield.

Pb-free SMD Package IR Reflow Profile

Step#	Profile Feature	Condition / Duration
Step 1	Ramp-up rate	1.5-3℃ /sec
Step 2	Preheat : 150~ 200℃ (Ta-Tb)	t1-t2: 60~80 sec
Step 3	Ramp-up rate (T_L to T_P)	1.5-3℃ /sec
	Temperature maintained above 220℃ (T_L)	t_L : 80~150 sec
Step 4	Peak temperature (T_P)	260+0/-5℃
	Time within 5℃ of actual peak temperature	30±10 sec
Step 5	Ramp-down rate	6℃/sec. Max.
Note1: Time 25℃ to peak temperature: 8 minutes max. Note2: The time between reflows shall be 5 minutes minimum and 60 minutes maximum.		

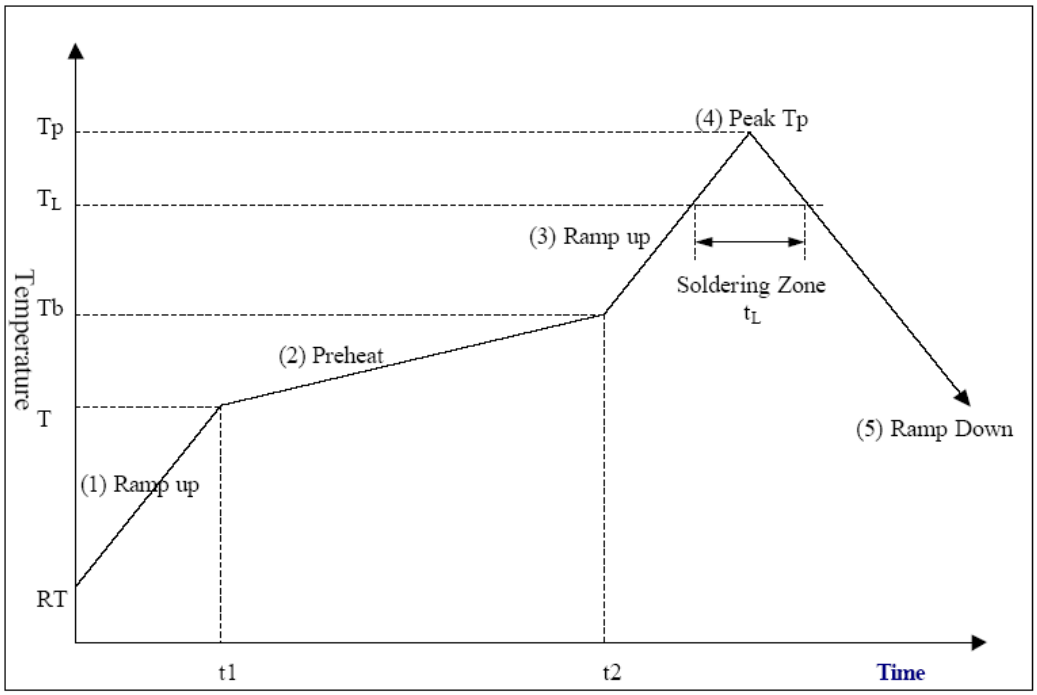


Figure 18. Reference SMD Package IR Reflow Profile

Appendix A. TX Power Configuration

Default output power is 6 dBm. Different output power settings are listed in the table below.
(TBD)

LREG0x201 [7]	LREG0x200 [2-0]	Reference Power
0b'1'	0b'111'	Default Power (dBm)
	0b'110'	Default Power-0.7 (dBm)
	0b'101'	Default Power-1.6 (dBm)
	0b'100'	Default Power-3.0 (dBm)
	0b'011'	Default Power-5.0 (dBm)
0b'0'	0b'111'	Default Power-6.0 (dBm)
	0b'110'	Default Power-7.0 (dBm)
	0b'101'	Default Power-8.5 (dBm)
	0b'100'	Default Power-10 (dBm)
	0b'011'	Default Power-12 (dBm)
	0b'010'	Default Power-14 (dBm)
	0b'001'	Default Power-16 (dBm)
	0b'000'	Default Power-20 (dBm)

Appendix B. Register Descriptions

Register Types

Register Type	Description
R/W	Read/Write register
WT	Write 1 to trigger register, automatically cleared by hardware
RC	Read to clear register
R	Read-only register
R/W1C	Read/Write '1' to clear register

B.1 Short Registers (SREG0x00~SREG0x36)

0x00	RXMCR	**0x0D**	RXFLUSH	**0x22**	WAKECTL	**0x30**	RXSR
0x03	AUINFL	**0x10**	RFCH	**0x24**	TXSR	**0x31**	ISRSTS
0x04	AUINFH	**0x12**	ACKTO	**0x26**	GATECLK	**0x32**	INTMSK
0x05	P0ADDR_0	**0x13**	MMIX	**0x2A**	SOFTRST	**0x34**	BATRXF
0x06	P0ADDR_1	**0x1A**	PIPEN			**0x35**	SLPACK
0x07	P0ADDR_2	**0x1B**	TXTRIG			**0x36**	RFCTL
0x08	P0ADDR_3	**0x1C**	P2ADDR				
0x09	P1ADDR_0	**0x1D**	P3ADDR				
0x0a	P1ADDR_1	**0x1E**	P4ADDR				
0x0b	P1ADDR_2	**0x1F**	P5ADDR				
0x0c	P1ADDR_3						

SREG0x00: RXMCR

RECEIVE MAC CONTROL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
r	**r**	**NOACKRSP**	**r**	**r**	**r**	**r**	**r**
R-0	**R-0**	**R/W-0**	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **NOACKRSP**: Automatic Acknowledgement Response

0: (default) Enables automatic acknowledgement response

1: Disables automatic acknowledgement response

Bit 4-0 **Reserved**: Maintain as '0b00000'

SREG0x03: AUINFL

ACKNOWLEDGEMENT USER INFORMATION LOW BYTE							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
AUINF7	AUINF6	AUINF5	AUINF4	AUINF3	AUINF2	AUINF1	AUINF0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AUINF[7:0]**: 16-bit User Information of Acknowledgement frame, Low Byte

SREG0x04: AUINFH

ACKNOWLEDGEMENT USER INFORMATION HIGH BYTE							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
AUINF15	AUINF14	AUINF13	AUINF12	AUINF11	AUINF10	AUINF9	AUINF8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AUINF[15:8]**: 16-bit User Information of Acknowledgement frame, High Byte

SREG0x05: **P0ADDR_0**

PIPE0 ADDRESS 0							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P0ADDR7	P0ADDR6	P0ADDR5	P0ADDR4	P0ADDR3	P0ADDR2	P0ADDR1	P0ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[7:0]**: Pipe0 address[7:0]

SREG0x06: **P0ADDR_1**

PIPE0 ADDRESS 1							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P0ADDR15	P0ADDR14	P0ADDR13	P0ADDR12	P0ADDR11	P0ADDR10	P0ADDR9	P0ADDR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[15:8]**: Pipe0 address[15:8]

SREG0x07: P0ADDR_2

PIPE0 ADDRESS 2							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P0ADDR23	P0ADDR22	P0ADDR21	P0ADDR20	P0ADDR19	P0ADDR18	P0ADDR17	P0ADDR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[23:16]**: Pipe0 address[23:16]

SREG0x08: P0ADDR_3

PIPE0 ADDRESS 3							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P0ADDR31	P0ADDR30	P0ADDR29	P0ADDR28	P0ADDR27	P0ADDR26	P0ADDR25	P0ADDR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P0ADDR[31:24]**: Pipe0 address[31:24]

SREG0x09: **P1ADDR_0**

PIPE1 ADDRESS 0							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P1ADDR7	P1ADDR6	P1ADDR5	P1ADDR4	P1ADDR3	P1ADDR2	P1ADDR1	P1ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[7:0]**: Pipe1 address[7:0]

SREG0x0a: **P1ADDR_1**

PIPE1 ADDRESS 1							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P1ADDR15	P1ADDR14	P1ADDR13	P1ADDR12	P1ADDR11	P1ADDR10	P1ADDR9	P1ADDR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[15:8]**: Pipe1 address[15:8]

SREG0x0b: P1ADDR_2

PIPE1 ADDRESS 2							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P1ADDR23	P1ADDR22	P1ADDR21	P1ADDR20	P1ADDR19	P1ADDR18	P1ADDR17	P1ADDR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[23:16]**: Pipe1 address[23:16]

SREG0x0c: P1ADDR_3

PIPE1 ADDRESS 3							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P1ADDR31	P1ADDR30	P1ADDR29	P1ADDR28	P1ADDR27	P1ADDR26	P1ADDR25	P1ADDR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P1ADDR[31:24]**: Pipe1 address[31:24]

SREG0x0D: RXFLUSH

RECEIVE FIFO FLUSH							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
r	**r**	**r**	**r**	**r**	**r**	**r**	**RXFLUSH**
R-0	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**	**WT-0**

Bit 7-1 **Reserved**: Maintain as '0b0000000'

Bit 0 **RXFLUSH**: Flush the RX FIFO

1: Flush RX FIFO. RX FIFO data is not modified. If Ping-pong FIFO is enabled (SREG0x34[0]=1), both FIFOs are flushed at the same time. Bit is automatically cleared to '0' by hardware.

SREG0x10: RFCH (Connected to LREG0x251 PLL3)

RF CHANNEL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
1MCSEN	**1MFRCH6**	**1MCSCH5**	**1MCSCH4**	**1MCSCH3**	**1MCSCH2**	**1MCSCH1**	**1MCSCH0**
R/W-0	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-1**	**R/W-0**	**R/W-1**

Bit 7 **1MCSEN**: 1 MHz Channel Spacing Enable

0: Disable (0000101: 2405 MHz default)

1: Enable When SREG0x10[7]=1, RF channel can be selected by SREG0x10[6:0].

Bit 6-0 **1MCSCH**: 1 MHz Channel Spacing Channel Number

SREG0x10[6:0] only works when SREG10[7]=1.

0000000: 2400 MHz	0100001: 2433 MHz	1000010: 2466 MHz
0000001: 2401 MHz	0100010: 2434 MHz	1000011: 2467 MHz
0000010: 2402 MHz	0100011: 2435 MHz	1000100: 2468 MHz
0000011: 2403 MHz	0100100: 2436 MHz	1000101: 2469 MHz
0000100: 2404 MHz	0100101: 2437 MHz	1000110: 2470 MHz
0000101: 2405 MHz	0100110: 2438 MHz	1000111: 2471 MHz
0000110: 2406 MHz	0100111: 2439 MHz	1001000: 2472 MHz
0000111: 2407 MHz	0101000: 2440 MHz	1001001: 2473 MHz
0001000: 2408 MHz	0101001: 2441 MHz	1001010: 2474 MHz
0001001: 2409 MHz	0101010: 2442 MHz	1001011: 2475 MHz
0001010: 2410 MHz	0101011: 2443 MHz	1001100: 2476 MHz
0001011: 2411 MHz	0101100: 2444 MHz	1001101: 2477 MHz
0001100: 2412 MHz	0101101: 2445 MHz	1001110: 2478 MHz
0001101: 2413 MHz	0101110: 2446 MHz	1001111: 2479 MHz
0001110: 2414 MHz	0101111: 2447 MHz	1010000: 2480 MHz
0001111: 2415 MHz	0110000: 2448 MHz	1010001: 2481 MHz
0010000: 2416 MHz	0110001: 2449 MHz	1010010: 2482 MHz
0010001: 2417 MHz	0110010: 2450 MHz	1010011: 2483 MHz
0010010: 2418 MHz	0110011: 2451 MHz	1010100: 2484 MHz
0010011: 2419 MHz	0110100: 2452 MHz	1010101: 2485 MHz
0010100: 2420 MHz	0110101: 2453 MHz	1010110: 2486 MHz
0010101: 2421 MHz	0110110: 2454 MHz	1010111: 2487 MHz
0010110: 2422 MHz	0110111: 2455 MHz	1011000: 2488 MHz
0010111: 2423 MHz	0111000: 2456 MHz	1011001: 2489 MHz
0011000: 2424 MHz	0111001: 2457 MHz	1011010: 2490 MHz
0011001: 2425 MHz	0111010: 2458 MHz	1011011: 2491 MHz
0011010: 2426 MHz	0111011: 2459 MHz	1011100: 2492 MHz
0011011: 2427 MHz	0111100: 2460 MHz	1011101: 2493 MHz
0011100: 2428 MHz	0111101: 2461 MHz	1011110: 2494 MHz
0011101: 2429 MHz	0111110: 2462 MHz	1011111: 2495 MHz
0011110: 2430 MHz	0111111: 2463 MHz	1100000: Undefined
0011111: 2431 MHz	1000000: 2464 MHz	...
0100000: 2432 MHz	1000001: 2465 MHz	1111111: Undefined

SREG0x12: ACKTO

ACKNOWLEDGEMENT TIMEOUT							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	MATOP6	MATOP5	MATOP4	MATOP3	MATOP2	MATOP1	MATOP0
R-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6-0 **MATOP[6:0]**: Maximum Acknowledgement Timeout Period

0000000: 0 (default)

…

0111001: 57

…

1111111: 127

SREG0x13: MMIX

TRANSMIT FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
DISATR	r	r	r	r	r	r	r
R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7 **DISATR**:

1: disable trigger FIFO after register wakeup (default)

0: enable

Bit 6-0 **Reserved**: Maintain as '0b0000000'

SREG0x1A: PIPEN

PIPE ENABLE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6 **PIPEN6**: Broadcasting frame enable

Bit 5 **PIPEN5**: Pipe5 enable

Bit 4 **PIPEN4**: Pipe4 enable

Bit 3 **PIPEN3**: Pipe3 enable

Bit 2 **PIPEN2**: Pipe2 enable

Bit 1 **PIPEN1**: Pipe1 enable

Bit 0 **PIPEN0**: Pipe0 enable

SREG0x1B: TXTRIG

TRANSMIT FIFO CONTROL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
TXRTYN3	**TXRTYN2**	**TXRTYN1**	**TXRTYN0**	**r**	**TXACKREQ**	**r**	**TXTRIG**
R/W-0	**R/W-0**	**R/W-1**	**R/W-1**	**R-0**	**R/W-0**	**R-0**	**WT-0**

Bit 7-4 **TXRTYN**: Maximum TX Retry Times
0000: 0
…
0011: 3 (default)
…
1111: 15

Bit 3 **Reserved**: Maintain as '0b0'

Bit 2 **TXACKREQ**: TX FIFO Acknowledgement Request bit
Transmit a packet with Acknowledgement request. If Acknowledgement is not received, the UM2471 retransmits up to xx times.
0: (default) No Acknowledgement packet requested
1: Acknowledgement packet requested

Bit 1 **Reserved**: Maintain as '0b0'

Bit 0 **TXTRIG**: Transmit Frame in TX FIFO bit
1: Transmit the frame in the TX FIFO. Bit is automatically cleared to '0' by hardware.

SREG0x1C: **P2ADDR**

PIPE2 ADDRESS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P2ADDR7	P2ADDR6	P2ADDR5	P2ADDR4	P2ADDR3	P2ADDR2	P2ADDR1	P2ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P2ADDR[7:0]**: Pipe2 address[7:0]

SREG0x1D: **P3ADDR**

PIPE3 ADDRESS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P3ADDR7	P3ADDR6	P3ADDR5	P3ADDR4	P3ADDR3	P3ADDR2	P3ADDR1	P3ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P3ADDR[7:0]**: Pipe3 address[7:0]

SREG0x1E: **P4ADDR**

PIPE4 ADDRESS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P4ADDR7	P4ADDR6	P4ADDR5	P4ADDR4	P4ADDR3	P4ADDR2	P4ADDR1	P4ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P4ADDR[7:0]**: Pipe4 address[7:0]

SREG0x1F: **P5ADDR**

PIPE5 ADDRESS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
P5ADDR7	P5ADDR6	P5ADDR5	P5ADDR4	P5ADDR3	P5ADDR2	P5ADDR1	P5ADDR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **P5ADDR[7:0]**: Pipe5 address[7:0]

REG0x22: WAKECTL

WAKE CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	r	r	r	r	r	R
R/W-0	WT-1	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7 **IMMWAKE**: Immediate Wake-up Mode Enable
0: (default) Disable Immediate Wake-up mode
1: Enable Immediate Wake-up mode

Bit 6 **REGWAKE**: Register Triggered Wake-up Signal
1: To wake UM2471 up. Bit is automatically cleared to '0' by hardware.

Bit 5-0 **Reserved**: Maintain as '0b000000'

SREG0x24: TXSR

TX STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY3	TXRETRY2	TXRETRY1	TXRETRY0	r	r	r	TXNS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-4 **TXRETRY[3:0]**: TXFIFO Retry Times
Maximum number of retries of the most recent TXFIFO transmission.
0000: 0 (default)
...
1111: 15

Bit 3-1 **Reserved**: Maintain as '0b000'

Bit 0 **TXNS**: Normal FIFO Release Status
0: (default) Succeeded
1: Fail, retry count exceed

SREG0x2A: SOFTRST

SOFTWARE RESET							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	RSTBB	RSTMAC
R-0	R-0	R-0	R-0	R-0	R-0	WT-0	WT-0

Bit 7-2 **Reserved**: Maintain as '0b000000'

Bit 1 **RSTBB**: Baseband Reset
1: Reset baseband circuitry. Initialization is not needed after **RSTBB** reset. Bit is automatically cleared to '0' by hardware.

Bit 0 **RSTMAC**: MAC and Short/Long Address Registers Reset
1: Reset MAC circuitry and Short/Long Address Registers. Initialization is needed after **RSTMAC** reset. Bit is automatically cleared to '0' by hardware.

SREG0x30: RXSR

RX MAC STATUS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
RXFFFULL	**WRFF1**	**r**	**RXFFOVFL**	**RXCRCERR**	**r**	**r**	**R**
R-0	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**	**R-0**

Bit 7 **RXFFFULL**: RX FIFO Full
0: (default) RX FIFO available for data receiving
1: RX FIFO not available for data receiving

Bit 6 **WRFF1**: RX FIFO Status
0: (default) Packet is ready in RX FIFO 0
1: Packet is ready in RX FIFO 1

Bit 5 **Reserved**: Maintain as '0b0'

Bit 4 **RXFFOVFL**: RX FIFO Overflow
0: (default) Not overflow
1: Overflow

Bit 3 **RXCRCERR**: RX CRC Error
0: (default) RX CRC correct
1: RX CRC error

Bit 2-0 **Reserved**: Maintain as '0b00'

SREG0x31: ISRSTS

INTERRUPT STATUS							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
r	**WAKEIF**	**r**	**r**	**RXIF**	**r**	**r**	**TXNIF**
R-0	**RC-0**	**R-0**	**R-0**	**RC-0**	**R-0**	**R-0**	**RC-0**

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6 **WAKEIF**: Wake-up Alert Interrupt (1)
0: (default) No wake-up alert interrupt occurred
1: A wake-up interrupt occurred

Bit 5-4 **Reserved**: Maintain as '0b00'

Bit 3 **RXIF**: RX FIFO Reception Interrupt (1)
0: (default) No RX FIFO reception interrupt occurred
1: An RX FIFO reception interrupt occurred

Bit 2-1 **Reserved**: Maintain as '0b00'

Bit 0 **TXNIF**: TX Normal FIFO Transmission Interrupt (1)
0: (default) No TX Normal FIFO transmission interrupt occurred
1: TX Normal FIFO transmission interrupt occurred

Note 1: Interrupt bits are cleared to '0b0' when the register is read.

SREG0x32: INTMSK

INTERRUPT MASK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	WAKEMSK	r	r	RXMSK	r	r	TXNMSK
R-1	R/W-1	R-1	R-1	R/W-1	R-1	R-1	R/W-1

Bit 7 **Reserved**: Maintain as '0b0'
Bit 6 **WAKEMSK**: Wake-up Alert Interrupt Mask
0: Enable the wake-up alert interrupt
1: (default) Disable the wake-up alert interrupt
Bit 5-4 **Reserved**: Maintain as '0b00'
Bit 3 **RXMSK**: RXFIFO Reception Interrupt Mask
0: Enable the RXFIFO reception interrupt
1: (default) Disable the RXFIFO reception interrupt
Bit 2-1 **Reserved**: Maintain as '0b00'
Bit 0 **TXNMSK**: TXFIFO Transmission Interrupt Mask
0: Enable the TXFIFO transmission interrupt
1: (default) Disable the TXFIFO transmission interrupt

SREG0x34: BATRXF

BATTERY AND RX FIFO CONTORL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	BATIND	r	r	r	r	R
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'
Bit 5 **BATIND**: Battery Low Indicator
0: Battery voltage higher than threshold voltage (1)
1: (default) Battery voltage lower than threshold voltage
Bit 4-0 **Reserved**: Maintain as '0b00000'

Note 1: Threshold voltage is set by LREG0x205[7:4]

SREG0x35: SLPACK

SLEEP ACKNOWLEDGEMENT AND WAKE-UP COUNTER							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
SLPACK	**WAKECNT6**	**WAKECNT5**	**WAKECNT4**	**WAKECNT3**	**WAKECNT2**	**WAKECNT1**	**WAKECNT0**
WT-0	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**

Bit 7 **SLPACK**: Sleep Acknowledgement
Place the UM2471 to Power Saving Mode. Bit is automatically cleared to '0' by hardware.

Bit 6-0 **WAKECNT[6:0]**: System Clock Recovery Time
WAKECNT is a 15-bit value. The WAKECNT[14:7] bits are located in SREG0x37
0000000: (default)

SREG0x36: RFCTL

RF MODE CONTROL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
r	**r**	**r**	**r**	**r**	**RFRST**	**r**	**R**
R-0	**R-0**	**R-0**	**R-0**	**R-0**	**R/W-0**	**R-0**	**R -0**

Bit 7-3 **Reserved**: Maintain as '0b00000'

Bit 2 **RFRST**: RF State Machine Reset [1]
0: (default) Normal operation of RF state machine
1: Hold RF state machine in Reset

Bit 1-0 **Reserved**: Maintain as '0b00'

Note 1: Perform RF reset by setting RFRST = 1 and then RFRST = 0. Delay at least 192 us after performing to allow RF circuitry to calibrate.

SREG0x38 BBREG0

BASEBAND REGISTER 0							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
r	**r**	**r**	**r**	**CONT_TX**	**BBMODE2**	**BBMODE 1**	**BBMODE 0**
R -1	**R-0**	**R-0**	**R-0**	**R/W-0**	**R/W-0**	**R/W-1**	**R/W-0**

Bit 7-4 **Reserved**: Maintain as '0b0'

Bit 3 **CONT_TX**: Continuously TX

0: (default) Normal TX operation

1: Continuously send modulated random data

Bit 2-0 **BBMODE [2:0]**: Turbo Mode Select

000: 125kbps DSSS-OQPSK

001: 1Mbps MSK

010: 250kbps DSSS-OQPSK (default)

011: 2Mbps MSK

100~111 : Undefined

B.2 Long Registers (LREG0x200~LREG0x25B)

0x200	TX_1	**0x211**		**0x250**	PLL_2
0x201	TX_2			**0x251**	PLL_3
0x202				**0x252**	
0x203				**0x253**	
0x204				**0x254**	DIG_LDO
0x205	BTM			**0x255**	
0x206	CRYSTAL			**0x256**	
0x207	PLL_1			**0x257**	
0x208				**0x258**	
0x209				**0x259**	PLL_4
0x20A				**0x25A**	
0x20B				**0x25B**	XTAL

LREG0x200: TX_1

TX 1							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
FDCSS	**WXTLPABUF1**	**WXTLPABUF0**	**LOBUFDUM**	**CMOD4M**	**ICTLPA2**	**ICTLPA1**	**ICTLPA0**
R/W-0	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-0**	**R/W-1**	**R/W-1**	**R/W-1**

Bit 7 **FDCSS**: Frequency Deviation Calibration Start Signal
0: OFF (default)
1: ON

Bit 6-5 **WCTLPABUF[1:0]**: PA Buffer Current Option
00: 0.8mA
01: 2.4mA
10: 3.9mA
11: 5.1mA (default)

Bit 4 **LOBUFDUM**: LO Buffer Dummy Enable @ TX Mode
0: Enable
1: Disable (default)

Bit 2-0 **ICTLPA[2:0]**: PA Reference Current Iref Option
000: 50uA
001: 75uA
010: 100uA
011: 125uA
100: 150uA
101: 175uA
110: 200uA
111: 225uA (default)

Note 1: Turn ON for 4M Fdev calibration.

LREG0x201: TX_2

TX 2							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
PC3V	**SPIPH**	**DFO1**	**DFO0**	**LORX1**	**LORX0**	**LOTX1**	**LOTX0**
R/W-1	**R/W-1**	**R/W-0**	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**

Bit 7 **PC3V**: 3V PA Output Power Control option
0 : 0 dBm
1 : 6 dBm (default)

Bit 6 **SPIPH**: SPI/Wake-up Pin Pull High Control
0: Disable
1: Pull high (default)

Bit 5-4 **DFO[1:0]**: Delta Frequency Offset
00: 800KHz
01: 1600KHz (default)
10: 3200KHz
11: N/A

Bit 3-2 **LORX[1:0]**: RX_LO Buffer Current Boost Option
00: 1250uA
01: 1500uA
10: 1750uA
11: 2000uA (default)

Bit 1-0 **LOTX[1:0]**: TX_LO Buffer Current Boost Option
00: 1250uA
01: 1500uA
10: 1750uA
11: 2000uA (default)

LREG0x205: BTM

BATTERY MONITOR							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
BATTH3	**BATTH2**	**BATTH1**	**BATTH0**	**RXFBW1**	**RXFBW0**	**DIGV1**	**DIGV0**
R/W-0	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**

Bit 7-4 **BATTH[3:0]**: Battery Monitor Threshold
0000: 1.8 V (default)
0001: 1.9 V
0010: 2.0 V
0011: 2.1 V
0100: 2.2 V
0101: 2.3 V
0110: 2.4 V
0111: 2.5 V
1000: 2.6 V
1001: 2.7 V
1010: 2.8 V
1011: 2.9 V
1100: 3.0 V
1101: 3.3 V
1110: 3.4 V
1111: 3.6 V

Bit 3 **BATON**: Battery monitor on or off
0: OFF (default)
1: ON

Bit 3-2 **RXFBW[1:0]**: RX Filter Bandwidth Option
00: 1.4MHz (default)
01: 2.3MHz
10/11: 4.6MHz

Bit 1-0 **DIGV[1:0]**: Digital Regulator Output Voltage
00: 1.8V (default)
01: 1.65V
10: 1.5V
11: 1.45V

LREG0x206: CRYSTAL

CRYSTAL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
STDB	**32MXAL**	**FDC**	**BATON**	**XTAL**	**DATAR1**	**DATAR0**	**MVCO**
R/W-0	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**

Bit 7 **STDB**: 32MHz Crystal Oscillator Standby Mode
0: Disable (default)
1: Enable

Bit 6 **32MXAL**: Start-Up Circuit of 32MHz Crystal Oscillator
0: Disable
1: Enable (default)

Bit 5 **FDC**: Frequency Deviation Calibration
Set LREG0x206<5>=0
Chip Version
Set LREG0x206<5>=1 (default)
Frequency Deviation Calibration Result

Bit 4 **BATON**: Battery monitor on or off
1: OFF (default)
0: ON

Bit 3 **XTAL**: Xtal Selection
0: 16MHz (default)
1: 32MHz

Bit 2-1 **DATAR[1:0]**: Data Rate for *Direct Modulation*, *VGA* and *VCO Calibration* Block
00: 125K/1Mbps (default)
01: 250K/2Mbps
10: 4Mbps
11: Forbidden

Bit 0 **MVCO**: VCO Sub-band Manual
0: Disable (default)
1: Enable

LREG0x207: PLL_1

PLL 1							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
CPIB1	**CPIB0**	**LF3R2**	**LF3R1**	**LF3R0**	**XTALST1**	**XTALST0**	**LOCK**
R/W-1	**R/W-0**	**R/W-1**	**R/W-1**	**R/W-0**	**R/W-1**	**R/W-0**	**R/W-1**

Bit 7-6 **CPIB[1:0]**: Charge Pump Current
- 00: 250uA
- 01: 200uA
- 10: 150uA (default)
- 11: 100uA

Bit 5-3 **LF3R[2:0]**: Loop Filter R3 Resistance
- 000: 25K ohm
- 001: 35K ohm
- 010: 45K ohm
- 011: 55K ohm
- 100: 70K ohm
- 101: 85K ohm
- 110: 100K ohm (default)
- 111: 115K ohm

Bit 2-1 **XTALST [2:1]**: XTAL Start-up pulse width
- 00: 0.5uS
- 01: 1.5uS
- 10: 3uS
- 11: 6uS

Bit 0 **LOCK**: Lock Detector Enable 0→1, detect

LREG0x250: PLL_2

PLL 2							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
CAPADJ	**VCOBD3**	**VCOBD2**	**VCOBD1**	**VCOBD0**	**LP1C2**	**LP1C1**	**LP1C0**
R/W-0	**R/W-0**	**R/W-0**	**R/W-1**	**R/W-0**	**R/W-1**	**R/W-1**	**R/W-1**

Bit 7 **CAPADJ**: Cap-Switch Value Adjustment
0: Nothing (default)
1: +1

Bit 6-3 **VCOBD**: VCO Band to Band Interval Reference Value
0010 (default)

Bit 2-0 **LF2R[2:0]**: Loop Filter R2 Resistance
000: 7K ohm
001: 10.5K ohm
010: 14K ohm
011: 17.5K ohm
100: 21K ohm (default)
101: 28K ohm
110: 35K ohm
111: 59K ohm

LREG0x251: PLL3 (Connected to SREG0x10: RFCH)

LREG0x253: DIG_LDO

DIGITAL LDO							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
PWRT	**FIFO**	**DIG**	**RXHPF1**	**VCOBAND3**	**VCOBAND2**	**VCOBAND1**	**VCOBAND0**
R/W-0	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-1**	**R/W-0**

Bit 7 **PWRT**: Digital Regulator Manually Shut-down in Active Mode
0: Disable (default)
1: Enable

Bit 6 **FIFO**: **a.** FIFO Power in Active Mode @power_test=1
0: Regulator (default)
1: GND
b. FIFO Power in Sleep Mode
0: VDD_Wake (default)
1: GND

Bit 5 **DIG**: **a.** Digital Power in Active Mode @power_test=1
0: Regulator (default)
1: GND
b. Digital Power in Sleep Mode
0: VDD_Wake (default)
1: GND

Bit 4-0 **VCOBAND[4:0]**: VCO Sub-band Control
00000: Highest band
…
00010: (default)
…
11111: Lowest band

LREG0x259: PLL_4

PLL 4							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
VCORX1	**VCORX0**	**VCOTX1**	**VCOTX0**	**VCOCP**	**MDCS**	**PSI1**	**PSI0**
R/W-0	**R/W-1**	**R/W-0**	**R/W-1**	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-0**

Bit 7-6 **VCORX[1:0]**: RX VCO Current Boost Option
00: 2475uA
01: 2250uA (default)
10: 2925uA
11: 2700uA

Bit 5-4 **VCOTX[1:0]**: TX VCO Current Boost Option
00: 2475uA
01: 2925uA (default)
10: 2250uA
11: 2475uA

Bit 3 **VCOCP**: CP for VCO Test
0: Enable (default)
1: Disable

Bit 2 **MDCS**: Manual Deviation Capacitor Setting
0: Auto (default)
1: Manual

Bit 1-0 **PSI[1:0]**: Pre-scalar Current Boost Option
00: (default)

LREG0x25B: XTAL

XTAL							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit1**	**Bit 0**
SDCN5	**SDCN4**	**SDCN3**	**SDCN2**	**SDCN1**	**SDCN0**	**VBGL1**	**VBGL0**
R/W-0	**R/W-0**	**R/W-0**	**R/W-0**	**R/W-1**	**R/W-0**	**R/W-0**	**R/W-0**

Bit 7-2 **SDCN[7:2]**: Set Deviation Capacitor Number
Number of Cmod (Do not set MSB=1)
000000: Minimum frequency deviation
…
000010: (default)
…
011111: Maximum frequency deviation

Bit 1-0 VBGL **[1:0]**: Low Output Voltage from Bandgap
00: 1.096V (default)
01: 1.018V
10: 0.939V
11: 0.861V

Revision History

Revision	Date	Description of Change
0.0	2013/10/07	Initial preliminary version.
0.1	2014/11/01	1. Change TX output power 2. Change package as QFN 4*4 20-pin
0.2	2016/02/23	Revise RF Long Address Registers Description Change package as QFN 3*3 16-PIN Change HW schematic 64-Byte TX FIFO reduced to 32-Byte 64-Byte RX FIFO reduced to 32-Byte Dual RX FIFO reduced to single RX FIFO 6 data pipes for 1:6 star networks Combine register wakeup and trigger command Trigger TX FIFO automatically after register wakeup Remove external wakeup function Revise Baseband control registers
0.3	2016/4/18	Change Initialization Change HW schematic Add GainTable
0.4	2016/6/29	Update the initialization Update Figure 17-2.schematic Add SREG0x13 Update battery monitor setting Revise standby/deep power down current

Contact UBEC:

Headquarters
Address: 6F-1, No. 192, Dongguang Rd., Hsinchu, 300 Taiwan
Tel: +886-3-5729898
Fax:+886-3-5718599
Website: http://www.ubec.com.tw

Sales Services
Tel: +886-3-5729898
Fax:+886-3-5718599
E-mail: sales@ubec.com.tw

FAE Services
Tel: +886-3-5729898
Fax: +886-3-5718599
E-mail: fae@ubec.com.tw

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