EXHIBIT 9

THEORY OF OPERATION

Theory of Operation

1. Introduction

LAWNIIP is an improved version of LAWNII, which is a wireless RS-232 radio modem. Each LAWNII contains a packet engine and a radio engine. LAWNII provides transparent RS-232 connections for any equipment that has a RS-232 port.

LAWNII was designed for indoor applications. It uses an internal monopole and with a maximum transmit power of 50mW. LAWNIIP is designed for outdoor applications. It has a polycarbonate housing that can be mounted on the mast of the antenna. The LAWNIIP can be used with various antennas, Yagi or omni-directional with gain up to 13db. The user must interface the LAWNIIP through a 50' RS-232 cable. This cable also supplies the power to the LAWNIIP. The transmit power of the LAWNIIP is only 20mW.

2. Block diagram

Please refer to the attached block diagram.

3. Transmitter

The transmitter circuits include a VCO, two stage class A amplifier and a low pass filter, receiver/ transmitter switch and a bandpass filter. The VCO is a Colpitts type oscillator and its frequency is controlled by a Phase Lock Loop. The output of the VCO is about +18 dbm. The two medium power amplifier provide 25 db isolation from the antenna port to the VCO so that the VCO will not be pulled by the antenna load variations. The output of the power amplifiers is fed to a T/R switch and then the printed low pass filter and the band pass filter. The cutoff frequency of the low pass filter is 1 Ghz and the bandpass filter has a -3db bandwidth of 40 Mhz. These two filters attenuate most of the high order harmonics to as low as -70dbc.

4. Receiver

The receiver share the frontend filter and T/R switch with the transmitter. The total loss of the frontend circuits is about 4 db. The frontend is followed by two stages of small signal amplifiers and an active mixer. The mixer has an LO amplifier built-in so that it requires a low driving signal as low as -5 dbm. The mixer has an conversion gain of 1 db. The receiver Local Oscillator is similar to the transmitter VCO. The mixer generates the low frequency IF frequency at 54 Mhz. The IF frequency is amplified by the IF gain block and filters to remove unwanted out-of-band spurious and then is fed to the demodulator. An high-speed, wide-bandwidth, IC demodulator (MC13055) is used as the demodulator.

5. Frequency synthesizer

The receiver local oscillator stays on all the time. It not only provides the LO drive to the receiver mixer, it also beats with the transmitter VCO to generate a low frequency oscillation signal to be used to synthesize the transmitter frequency. The beating mechanism provides a low frequency version of the transmitter frequency without using a divider which will adversely slow down the response time of the phase lock loop. As a result, the keyup time of the transmitter is normally below 300 usec.

6. Packet engine

LAWNIIP use a Zilog 84C15 processor to build the packet for the transmitter and valid the packet for the receiver. The packet protocol follows the industry standard of AX.25 with some minor modifications. The standard packet has 256 bytes of data and 21 bytes of overhead and some pre-amble for the receiver to synchronize. A 9.8304 Mhz crystal is used as the system clock. The baud rate over the air is a constant speed of 76.8 Kbaud. The maximum serial port baud rate is 38.4 Kbaud. LAWNIIP utilizes the CSMA/CD technology to prevent packet collision.

7. ASIC

The OCI-100 ASIC contains the synthesizers for the receiver and transmitter PLL's and the spreading and dispreading for the chips. Each data bit is spreaded into 16 data chips for the transmitter. As for the despreading, a state machine is used to detect, acquire and lock the local chips to the incoming chips. The ASIC can detect and lock the incoming chips in less than 50 usec.

8. Battery Backup

A lithium battery is used to keep the containss of the RAM alive when the unit is powered off.. To protect the RAM from being disturbed during abnormal operating conditions, a Maxim 691 chip is used to monitor the power line and protect the Chip Enable line of the RAM.

9. Power Supply

A low dropoff voltage regulator is used to provide a clean 5 Volt to the whole system. The recommended power supply voltage input is 8V DC.

10. LED Display

The status of the LAWNIIP is shown through the four LEDs that indicates the condition of power, traffic, transmitter and link connection. These four LEDs provide an easy way for system debugging.

11. Processing Gain

Since the LAWNIIP used post-IF despreading technique for chip despreading, the processing gain of the despreader can only be measured indirectly by measuring the jamming margin. According to the

Dixon's book " Spread Spectrum Systems", the processing gain can be calculated as follows,

PG = JM +S/N + SL

where PG is the processing gain, JM is the jamming margin, S/N is the required S/N and SL is the system loss.

The test equipment setup for measuring the jamming margin is show as the attached figure. A LAWNIIP with the transmitter locked on and placed inside a completely sealed tin can is used as the test signal. This test signal is then combined with the jamming signal from a signal generator to become the composite test signal which is then splitted into two signals, one for the Unit Under Test (UUT) and the other is sent to the spectrum analyzer for monitoring.

The test signal level used for the testing is fixed to -32 dbm to simulate the pass loss for about 50 feet indoors. The jamming signal's level and frequency are adjustable. During the test, the jamming signal's level at each test frequency will be increased until the error rate of the UUT exceeds the minimum requirement of 10^{-4}. The level difference between the test signal and the jamming signal for causing 10^{-4} error rate is the desired jamming margin at that frequency.

The frequency of the jamming signal has to cover the whole -6db bandwidth of the spectrum with 50 Khz steps. Since the LAWNIIP's -6 db spectrum bandwidth is 2.6 Mhz, there are 53 frequencies to be measured. The Channel 2 (center at 914.8Mhz) of the LAWNIIP is used as the test channel and the jamming frequency starts at 913.5 Mhz and stops at 916.1 Mhz.

The jamming margin of each of the test frequency is shown as follows,

Frequency(Mhz)	Jamming Margin(dB)	
913.5	+0.2	
913.55	-0.2	
913.6	-2.0	
913.65	-2.4	
913.7	-0.9	
913.75	-1.3	
913.8	-2.0	
913.85	-1.4	
913.9	-1.2	
913.95	-2.0	
914	-2.9	(#5)
914.05	-2.5	(#10)
914.1	-4.0	(#1)
914.15	-3.2	(#3)
914.2	-2.9	(#4)
914.25	-2.4	
914.3	-3.3	(#2)
914.35	-2.8	(#8)
914.4	-2.2	
914.45	-1.2	

914.5	-0.2	
914.55	-0.5	
914.6	-0.9	
914.65	-1.0	
914.7	-1.0	
914.75	-1.2	
914.8	-1.2	
914.85	-1.2	
914.9	-1.3	
914.95	-1.4	
915.	-1.9	
915.05	-1.6	
915.1	-2.0	
915.15	-2.4	
915.2	-2.1	
915.25	-2.8	(#7)
915.3	-2.0	
915.35	-2.9	(#6)
915.4	-1.8	
915.45	-2.0	
915.5	-1.0	
915.55	-1.7	
915.6	-1.1	
915.65	-2.6	(#9)
915.7	-1.9	
915.75	-1.9	
915.8	-1.8	
915.85	-0.8	
915.9	-0.2	
915.95	+0.5	
916	+0.6	
916.05	-0.9	
916.1	-0.9	

Since 80% of the test frequencies have a jamming margin better than -2.5 db, the jamming margin of the LAWNIIP is measured as -2.5 db.

Since the LAWNIIP uses the FSK demodulator that requires 13 db S/N for an error rate of 10^{-4} and consider a moderate system loss of 2 db, the processing gain of the LAWNIIP is calculated as

PG = -2.5 +13 +2 = 12.4 db