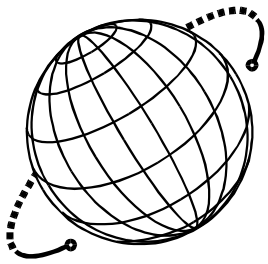

Actiontec

Expanding Your World of Data Communications

802.11A WIRELESS ACCESS POINT (AP) FUNCTIONAL SPECIFICATION

Serial # 802AA
Revision 0.1
11/9/2001

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Preface

This document describes functional details for an IEEE 802.11 wireless LAN access point (AP) reference design.

About this Document

The document consists of the following chapters:

Part 1	Architecture---Describes the system architecture reference design for developing an IEEE 802.11 compatible AP.
Part 2	Software---Describe the operating system use for the AP reference design.
Part 3	Performance---Provides detailed performance specifications for the AP reference deign.
Part 4	Electrical Characteristics---Provides electrical specifications for the AP reference deign.
Part 5	Physical Characteristics---Provide s physical characteristics and environmental requirements for the AP reference design.
Part 6	Regulatory Compliance---Describes the U.S., Canadian, and Japanese regulatory compliance requirements for the AP reference design.

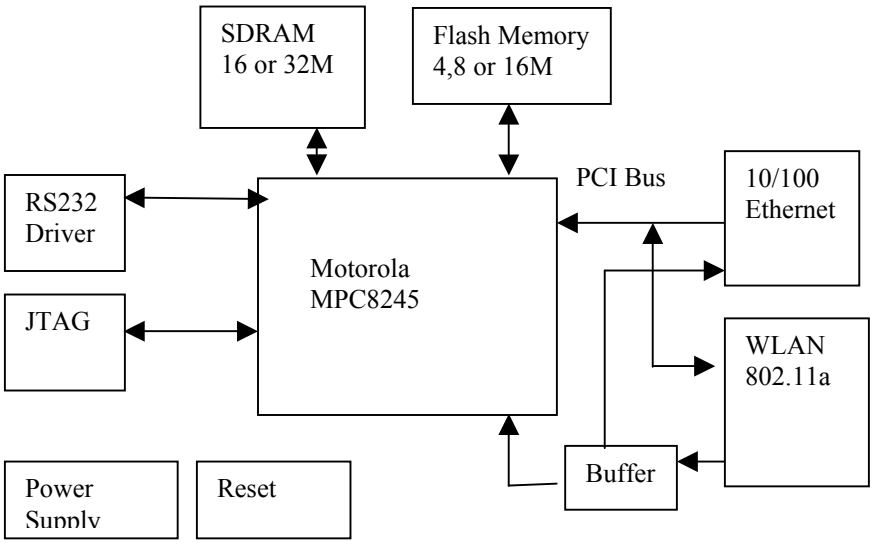
Architecture

Figure 1 is a block diagram of the overall access point (AP) reference design. There are three distinct subsystems within the reference deign:

1. MPC8245 processor subsystem
2. 802.11 wireless LAN subsystem
3. 10/100 Mbps Ethernet LAN subsystem

Each of thee blocks is describe d in the following sections.

802.11 Wireless AP Block Diagram

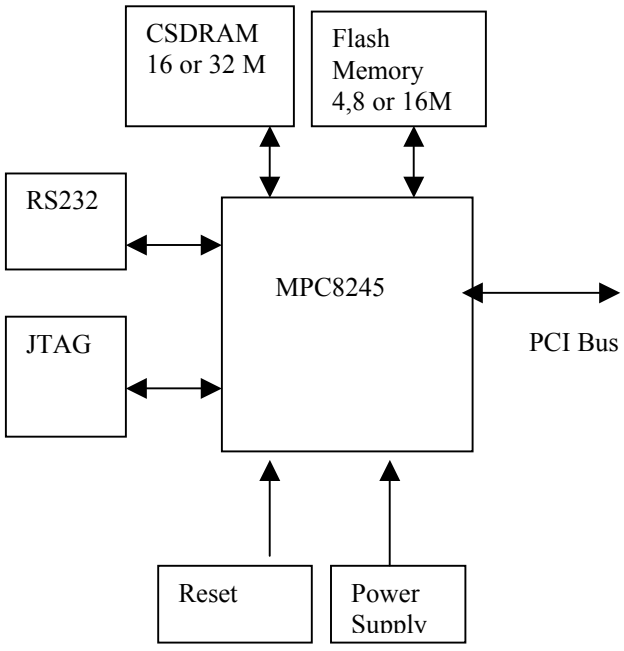


MPC8245 Processor Subsystem

The processor subsystem include the Motorola MPC8245 integrated processor, which combine powerful power PC 603e core with peripheral blocks that provide functionality common to most embedded applications. This subsystem of the overall access point design include:

- MPC8245 integrated processor
- Flash memory: The 4, 8 or 16 MB of Flash memory contains the real-time operating system code board support software for the overall AP and power up parameters for the processor, as well as wireless and Ethernet LAN subsystems
- SDRAM: The16 or 32 MB of SDRAM provide memory for buffering wireless and Ethernet LAN packets, and space for copying operating system software from the on board Flash device to get faster execution from the SDRAM
- PCI bus host functions for embedded peripheral interfacing
- RS232 serial interface is provide for configuring the access point from terminal device
- JTAG interface for test and debug
- Functions that are common to other sections of the overall access point reference design such as power supply and reset circuit

Figure 2. MPC8245 Processor Subsystem Block Diagram



Processor

The Motorola MPC8245 is an integrated processor that combines the Power PC 603e core with peripheral logic block. The peripheral logic block implements functionality that is common to large number of embedded applications.

TheMPC8245's integrated peripheral logic block provide the following functionality:

- A PCI bridge with an integrated bus arbitrator that allows seamless attachment of predesigned PCI functional blocks to the processor. This interface allows the connection of up to five PCI devices through a set of dedicated request, grant, and interrupt line.
- An integrated high performance memory controller that supports various types of DRAMs and ROMs.
- A DMA controller.
- An integrate SDRAM clock generation capability.
- An interrupt controller.
- An I2O message controller.
- An I2C controller.

The Power PC 603e core is full-featured high performance processor with the following functionality:

- floating point support
- memory management
- 16 Kbyte instruction cache
- 16 Kbyte data cache
- power management features

TheMPC8245 contains an internal 60x Power PC bus that interfaces the Power PC 603e core to the system logic. The core is capable of operating at variety of frequencies allowing the designed to make performance and power consumption trade offs. The processor core is clocked from a separate PLL which is referenced to the system logic PLL. This allows separate frequency selection between the processor and the system logic, while maintaining synchronous bus interface. The Actiontec access point reference design currently operates the processor core at clock frequency of 250 MHz. The processor provides an interface to 64 bit data and 32 bit address bus, long with control signals that optimize performance of the interface between the processor and core logic.

Flash Memory

The AP reference deign has an 8 bit Flash deice The footprint for the Flash device can accommodate 4, 8, or 16 MB 3.3 V Intel strata Flash deice without any layout change. The default configuration for the AP reference deign is 8 MB of Flash memory, and component stuffing changes are required to use higher or lower density Flash devices. The Flash device can have an access time as slow as 120 ns. The access point operating system software is store in the Flash memory and is copied to the SDRAM at power up for faster execution. Besides the AP operating system software, the Flash device also stores the power up configuration for the processor, and the wireless and Ethernet subsystems.

Table 11. Flash Memory Address Map

Flash Memory Part Number	Capacity	Organization	Address Range
E28F320J3A120	4 MB	4 M x 8 bits	FF00 0000 -- FF3F FFFF
E28F640J3A120	8 MB	8 M x 8 bits	FF00 0000 -- FF7F FFFF
E28F128J3A120	16 MB	16 M x 8 bits	FF00 0000 -- FFFF FFFF

SDRAM Memory

The access point reference deign has provision for either 16 or 32 Mbyte of SDRAM, organized in 2 M x 64 bit or 4 M x 64 bit configuration. The SDRAM system is implemented using two parts each of either MT48LC2M32B2TG7 or MT48LC4M32B2TG7 available from Micron Technology, Inc. Internally, three SDRAM deice reorganizes 512 K x 32 bits x 4 banks or 1 M x 32 x 4 banks. Two separate bank select lines provide access to one of four internal banks. A 12-bit interface provides row and column addresses for the SDRAM, and eight separate DQM signals provide byte selections.

TheMPC8245 processor provide the following control signals for the SDRAM operation:

- write enable
- column address strobe
- row address strobe
- memory clock enable
- eight bi-directional d t parity signals
- clock for synchronous operation

The clock is in-phase and at the same frequency as the memory bus clock. In the Actiontec access point reference deign, the SDRAM memory bus runs at 96 MHz; therefore, the parts are required to support clock frequency of 100 MHz or more The previously mentioned part numbers from Micron can support clock speeds of up to 143 MHz.

Table 12. SDRAM Memory Address Map

Memory type	Capacity	Organization	Address Range
MT48LC2M32B2TG7	16 MB	2 M x 64 bits	0000 0000 -- 00FF FFFF
MT48LC4M32B2TG7	32 MB	4 M x 64 bits	0000 0000 -- 01FF FFFF

PCI Bus

The AP reference design supports a PCI 2.2 compliant 32 bit wide PCI bus, and has two PCI peripherals (an 802.11 wireless LAN deice and an 802.3 10/100 Mbps Ethernet LAN) attached to it. The PCI bus is clocked to 32 MHz in the current deign, but the MPC8245 supports PCI bus speeds of up to 66 MHz. The reason for clocking the PCI bus at 32 MHz instead of the standard 33 MHz is to reduce cost. The 32 MHz clock is readily available from the Actiontec 802.11 wireless LAN subsystem. The 32 MHz clock coming from the AR5110 chip is buffered and fed into three parallel buffers. The output of two of three buffers is used as the PCI clock for 802.11 wireless LAN and Ethernet LAN subsystems. The output of the third buffer is provided to the system clock input of the PC8245. This approach saves an extra oscillator. The output of these three filters is filtered to reduce emissions.

Both the wireless and Ethernet LAN subsystems operate at 3.3 V. The MPC8245 processor acts as the host on this bus and provides all necessary PCI functions, including the bus arbitration function through five pairs of dedicated request and grant line. (Only two of three are used for the Ethernet LAN and wireless LAN).

RS232 Interface

An RS232 interface capable of 115 kbps operation is provided to configure the AP through terminal interface, and connect to external device such as analog modems. The modem is supported as reference design feature for residential gateway applications. The MPC8245 provides one integrated full- function universal synchronous receiver/transmitter (UART) with RX, TX, RTS, and CTS signaling, or two integrated UARTs with only RX/TX sign ling. The Actiontec access point reference design implements one full function UART (RX, TX, CTS, RTS).

The UART module is an integrated part of the MPC8245 and consists of the following:

- serial communication channel
- sixteen bit counter for Baud rate generation
- internal channel control logic
- interrupt control logic

This UART enable the software selectable serial interface data format to allow selection of the number of start, stop, data, and parity bits.

A MAX3232 transceiver is use to convert voltage lees for proper RS232 signaling. Because of the built-in charge pumps, this transceiver is powered by a 3.3 V supply that is readily available on the board.

JTAG Interface

A JTAG interface is provided for connecting an in-circuit emulator for software development. One such in circuit emulator is EST/WindRiver's Vision ICE. The JTAG interface can also be used during manufacturing flow for production testing and debug of the access point.

System Reset

An on-board MAX6713 reset circuit provides reset to processor, memory, and PCI deice. This circuit generates a fixed reset pulse of at least 140 ms whenever the supply voltage falls below a preset threshold level. A manual push button reset option provides for easy generation of the reset signal without cycling power to the access point.

System Power Supply

The AP reference design gets its power from regulate 3.3 V DC power supply wall mount unit. The power supply design also use one adjustable low dropout (LDO) linear regulator for 2.0 V. The input to this 2.0 V LDO comes from the3.3 V regulated wall mount power supply.

The 2.0 V power is provided to run the MPC8245 processor core, and the 3.3 V power is use for the reset of the access point, including SDRAM, Flash, RS232 drives, discrete gate logic, and wireless and Ethernet LAN subsystems. The wireless LAN subsystem, describe in the following section, provide further detail on how it derives its internal power supplies from the 3.3 V power source. Protection diodes are provided to ensure proper power sequencing. The estimated worst -case current draw from the 2.0 V linear regulator is about 1.5A.

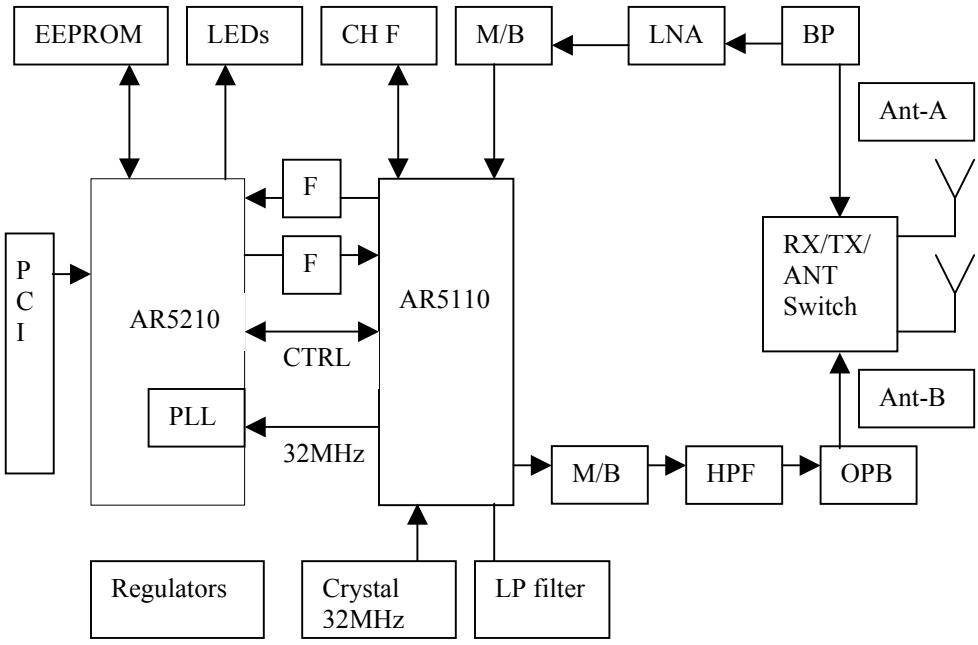
ActionTec 802.11AA Wireless LAN Subsystem

The ActionTec AP uses AR5000 chipset from Atheros as the main component of the wireless LAN subsystem. The chipset consists of the following:

- AR5210: An IEEE 802.11 MAC, b send processor, and PCI bus interface.
- AR5110: An all CMOS single chip radio transceiver with integrated power amplifier that converts input signals from 5 GHz to the 20 to 40 MHz range used by the AR5210.

The AR5000 chipset provides a highly integrated IEEE 802.11a solution, as shown in Figure 4. The following sections describe the functionality for each block in Figure 4.

AR5210: ActionTec MAC/BBP for IEEE 802.11a 5-GHz Wireless LANs
196 BGA plastic package
AR5110: ActionTec Radio-on-a-Chip for 5-GHz Wireless LANs
64-pin leadless plastic chip carrier package



MAC/Baseband Processor (AR5210)

The AR5210 chip is an IEEE 802.11 compliant, highly integrate ASIC containing a PCI interface DMA engine protocol control unit (PCU) which provides time critical media access control [MAC] functions, and a baseband processor (PLCP/PHY). TheAR5210 runs on 2.5 V (digital and analog) core and 3.3 V I/O. TheAR5210 is packaged in 15x15x1.5 mm 196 plastic ball grid array (PBGA).

PCI Front End (AR5210)
The PCI front end of theAR5210 is PCI 2.2 and PC Card 7.1 compliant. In the access point reference design, this front end seamlessly interfaces to the PCI bus provided by the MPC8245 integrated processor.

DMA Engine (AR5210)
The DMA engine is 32 bits wide and feds d t from the PCU to the PCI bus. The DMA engine coordinates transfers between the PCU and the host through DMA descriptors. These linked descriptors point to data segments being sent or received. They communicate control information from the host to the DMA engine, and status information from the DMA engine to the host.
The software is responsible for building these linked descriptor lists. For details on DMA functionality and descriptor lists, refer to theAR5210 MAC/Baseband processor for IEEE 802.11a 5 GHz Wireless LAN data sheet.

Protocol Control Unit (PCU -- AR5210)
The PCU, or MAC state machine, buffers transmit and receive frames for the DMA engine in independent 4 kB FIFOs. The PCU also contains the state machine logic for implementing wire equivalent privacy (WEP) and CRC capabilities. The AR5210 internal registers are used to configure the PCU. For a listing of these registers, refer to the AR5210 MAC/Baseband processor for IEEE 802.11a 5 GHz Wireless LAN data sheet.

Baseband Processor (PHY -- AR5210)
The baseband processor either transfers data from the PCU and builds the frame that the RF subsystem (AR5110) transmits, or receives frames coming from the RF subsystem and decodes the frame for transmission to the PCU. The frame format is constructed with short and long training symbols intermixed with the data and rate /length information.

The baseband processor is responsible for the following frame functions:

- Scramble
- encode
- puncture
- pad
- interleave
- map to constellations
- scale

The baseband processor runs an iFFT on groups of 48 subcarriers and 4 pilots. Next, the processor sends the resulting time-domain waveform, including the guard interval, through the digital filter, up-sampler, and DAC. The AR5210 supports the following modulations:

- BPSK
- QPSK
- 16 QAM
- 64 QAM

The baseband processor self-calibrates each time it is powered on. Registers can also be programmed to force calibration. The interface between the AR5110 and AR5210 is the DAC for the transmit path, and an ADC for the receive path. For further information on the AR5210 base band processor, refer to the AR5210 MAC/Baseband processor for IEEE 802.11a 5 GHz Wireless LAN data sheet.

Phase Locked Loop (PLL -- AR5210)
The PLL take the base 32 MHz clock frequency from theAR5110 and deliver
The following core frequencies:

- 40 MHz
- 80 MHz
- 160 MHz

The baseband processor and the ADC and DAC use these clocks.

ADC (AR5210)
The ADC provide 9 bits of resolution and runs at 80 mega samples per second. It takes the analog received signal on the I and Q channels from the AR5110, through the anti-aliasing filter, and converts the signal to digital data for processing by the baseband and subsequent blocks within theAR5210.

DAC (AR5210)
The DAC is 9 bit and runs at 160 mega samples per second. It takes the digital data coming from the baseband and converts it to analog signals that go to AR5110 through external reconstruction filter.

ADC Filter

External anti-aliasing filters are used between the AR5110 receive in-phase/quadrature—phase (I/Q) outputs and the ADC inputs of the AR5210. The ADC 20 MHz antialiasing filter prevents aliasing by attenuating differential RX in-phase and quadrature-phase signals above the Nyquist frequency. The filters are differential for both the quadrature--phase and in-phase components. The third order elliptical filter operates in current mode and bandlimits the input signals with a 3 dB corner frequency of 35 MHz. This filter attenuates out-of-band spectral components and wideband noise. Refer to the AR5110 data sheet for further information on the anti-aliasing filter.

DAC Filter

External reconstruction filters are used between the AR5110 transmit I/Q inputs and the DAC outputs of the AR5210. The DAC uses a lowpass, 20 MHz reconstruction filter to remove spectral images and out-of-band quantization noise. The filters are differential for both the quadrature-phase and in-phase components. The third-order, current mode, Butterworth filter has a 3 dB corner frequency of 40 MHz. The load is an on-chip current mirror that is internally biased. An internal RC filter provides additional attenuation beyond the self-resonance frequency of the external inductor. Refer to the AR5110 data sheet for further information on the reconstruction filter.

Single-Chip Radio Transceiver (AR5110)

The AR5110 chip is an integrated 5 GHz CMOS radio transceiver that supports the IEEE 802.11 standard. The chip includes an integrated power amplifier, and supports connection to an external output booster for higher performance The transceiver core, digital logic, and VCO are powered by 2.5 V. The tolerances on the 2.5 V supply need to be +/ 5%. The I/Os are powered by 3.3 V. The AR5110 is packaged in 64pin, 9x9x1 mm lead-less plastic chip carrier (LPCC).

TheAR5110 chip supports the IEEE 802.11 5 GHz UNII frequencies listed in Table 3. The external output booster improves performance for operation up to 20 dBm.

Table 13. Supported U-NII Frequencies

UNII Frequencies	Number of Usable Channels
5.15 to 5.25 GHz (indoor only)	Four 20 MHz channels
5.25 to 5.35 GHz (indoor and outdoor)	Four 20 MHz channels

The AR5110 supports tuning to all eight channels between 5.15 and 5.35 GHz, leaving two 20 MHz channels unused as guard band. The 20 MHz channels are divided into 52 carries; 48 are used to carry data and 4 are pilot signals. All 52 carriers are always used. Varying modulation and error-correction coding supports standard IEEE 802.11 data rates that range from 6 to 54 Mbps. Each of the carries is ~300 kHz wide, resulting in raw data rates that range from 125 kbps to 1.5 Mbps.

The AR5110 also supports tuning to the Japan allocated 5 GHz frequency band from 5.17 to 5.23 GHz.

Turbo Mode

In addition to the IEEE 802.11 standard data rates, theAR5000 chipset provides an enhanced turbo mode with higher data rates. Channel size in the Turbo Mode TM changes from 20 to 40 MHz, creating three available channels with twice the data bandwidth. The maximum supported data rate in turbo mode is 72 Mbps. Figure 4 shows the three turbo channels in the 5.15 to 5.35 GHz range that the AR5000 chipset supports.

The AR5110 supports the following methods of power conservation:

- power down the TX chain through the AR5210
- power down the RX chain through the AR5210
- enter sleep mode, so that only the clock oscillator is active

The programming interface on the AR5110 is controlled through a serial bus between the AR5210 and AR5110. Registers inside the AR5110 control the following:

- RX chain
- TX chain
- synthesizer
- bias control

Thee registers are controlled by software to perform the following functions using the AR5210 and are loaded during initialization.

- gain setting
- offset adjustment
- operating frequency
- power save /activity: transmit, receive, idle, sleep

Special FCC 15.407 Requirements

Frequency Stability (15.407 (g))

FCC 15.407(g) states: "Manufacturers of U-NII devices are responsible for ensuring frequency stability such that an emission is maintained within the band of operation under all conditions of normal operation as specified in the users manual."
The device uses 8 channels between 5.18GHz and 5.32GHz. The carrier is 20MHz wide centered at these frequencies. IE: Channel 6 (5.18GHz) would have the fc centered at 5.18GHz with a band width of 20Mhz or 5.17 to 5.19 GHz. This provides a guard band of 20 MHz (5.17 GHz - 5.15 GHz).
The device also requires a +/- 20 ppm XTAL over temperature and with aging. This is required per the 802.11a specification. Based on the tolerance of the XTAL and the 20 MHz guard band between 5.15GHz and 5.35 GHz the device will maintain emissions within the UNII 1 and 2 bands under normal operating conditions specified in the user manual.

Insuring Indoor Use in 5.15-5.25 GHz Band (15.407 (e))

FCC 15.407(e) states: "Within the 5.15-5.25 GHz band, U-NII devices will be restricted to indoor operations to reduce any potential for harmful interference to co-channel MSS operations."
The user manual includes the following statement:

> "Radio Frequency interference requirements: This device is restricted to indoor use only. Industry Canada and FCC requires this product to be used indoors due to its operation in the frequency range 5.15 to 5.25 GHz"

Discontinue Transmitting with absence of Data or operational failure (15.407 (c))

FCC 15.407(e) states: "*The device shall automatically discontinue transmission in case of either absence of information to transmit or operational failure. These provisions are not intended to preclude the transmission of control or signaling information or the use of repetitive codes used by certain digital technologies to complete frame or burst intervals. Applicants shall include in their application for equipment authorization a description of how this requirement is met*."

Data transmission is always initiated by software, which is then passed down through the MAC, through the digital and analog baseband, and finally to the RF chip. Several special packets (ACKs, CTS, PSPoll, etc...) are initiated by the MAC. These are the only ways the digital baseband portion will turn on the RF transmitter, which it then turns off at the end of the packet. Therefore, the transmitter will be on only while one of the aforementioned packets is being transmitted.

802.11AA Wireless AP SUMMARY

I. Features

- IEEE 802.11a compatible
- 5.15 to 5.35 GHz U-NII frequency band operation for North America
- 5.17 to 5.23 GHz frequency band operation for Japan
- Orthogonal Frequency Division Multiplexing (ODFM) scheme
- Modulation scheme: BPSK, QPSK, 16QAM & 64 QAM
- Data Rates: 6, 9, 12, 18, 24, 36, 48 and 54 Mbps
- Turbo mode offering up to 72-Mbps data rate
- Full Implementation of the MAC Protocol Specified in IEEE Standards 802.11-1999 and 802.11a
- Internal Encryption Engine Executes IEEE802.11 WEP
- 128-bit WEP encryption, backward compatible with 64-bit solutions.
- Support BSS (Infrastructure mode) and IBSS (Ad hoc mode).
- On-board Diversity Antenna Switch

Specification Compliance

- IEEE 802.11a
- PC Card standard 7.1

Modulation Methods

Date Rate (Mbps)	Supported	IEEE 802.11a Standard Rate	Turbo Mode	Modulation and Encoding Rate
6	Yes	Yes	-	BPSK, R1/2
9	Yes	Yes	-	BPSK, R3/4
12	Yes	Yes	-	QPSK, R1/2
18	Yes	Yes	-	QPSK, R3/4
24	Yes	Yes	-	16 QAM, R1/2
36	Yes	Yes	-	16 QAM, R3/4
48	Yes	Yes	-	64 QAM, R2/3
54	Yes	Yes	-	64 QAM, R3/4
12	Yes	-	Yes	BPSK, R1/2
18	Yes	-	Yes	BPSK, R3/4
24	Yes	-	Yes	QPSK, R1/2
36	Yes	-	Yes	QPSK, R3/4
48	Yes	-	Yes	16 QAM, R1/2
72	Yes	-	Yes	16 QAM, R3/4

Channel Assignment

For North American

This wireless function supports eight 20MHz channels between 5.15 and 5.35 GHz leaving two 20MHz channels unused as guard band. The 20 MHz channels are divided into 52 carriers; 48 carry data, 4 are pilot signals.

Many countries and regions are currently revising the channel assignment.

For Japan
4 channels are supported from 5.17 to 5.23 GHz.

Security (WEP Key)

Wired equivalent privacy (WEP) supports modes that have 40, 104 and 128 bit keys. With the concatenation of the 24 bit IV, these keys become 64, 128, and 152 bit. These supported modes and key will be available through Windows network properties.

PCI PME & Vaux

There is no standard specification of Wakeup-on-WirelessLAN defined. Therefore, PME pin is not necessary. The PME pin on PC Card bus is not connected to this device.

RF Characteristics

Frame Error Rate

This design will meet the 802.11a specification of less than 10% frame error rate.

Data rate

Date Rate (Mbps)	Supported	IEEE 802.11a Standard Rate	Turbo Mode	Modulation and Encoding Rate
6	Yes	Yes	-	BPSK, R1/2
9	Yes	Yes	-	BPSK, R3/4
12	Yes	Yes	-	QPSK, R1/2
18	Yes	Yes	-	QPSK, R3/4
24	Yes	Yes	-	16 QAM, R1/2
36	Yes	Yes	-	16 QAM, R3/4
48	Yes	Yes	-	64 QAM, R2/3
54	Yes	Yes	-	64 QAM, R3/4
12	Yes	-	Yes	BPSK, R1/2
18	Yes	-	Yes	BPSK, R3/4
24	Yes	-	Yes	QPSK, R1/2
36	Yes	-	Yes	QPSK, R3/4
48	Yes	-	Yes	16 QAM, R1/2
72	Yes	-	Yes	16 QAM, R3/4

Transmit Power Specification

Modulation Scheme	Transmit Power in dBm (typical)
BPSK, R1/2	14
BPSK, R3/4	14
QPSK, R1/2	14
QPSK, R3/4	14
16 QAM, R1/2	14
16 QAM, R3/4	12
64 QAM, R2/3	9.5
64 QAM, R3/4	7.5

Maximum Input Level

Maximum received signal strength allowed at the antenna.

Modulation/Rate	Maximum Input Level in dBm
BPSK, R1/2 (6Mbps)	-14
BPSK, R3/4 (9Mbps)	-14
QPSK, R1/2 (12Mbps)	-14
QPSK, R3/4 (18Mbps)	-14
16 QAM, R1/2 (24Mbps)	-14
16 QAM, R3/4 (36Mbps)	-18
64 QAM, R2/3 (48Mbps)	-20
64 QAM, R3/4 (54Mbps)	-20
BPSK, R1/2 Turbo (12Mbps)	-14
BPSK, R3/4 Turbo (18Mbps)	-14
QPSK, R1/2 Turbo (24Mbps)	-14
QPSK, R3/4 Turbo (36Mbps)	-14
16 QAM, R1/2 Turbo (48Mbps)	-14
16 QAM, R3/4 Turbo (72Mbps)	-18

Blocker Performance

Modulation Scheme	Adjacent Blocker (n + 1 channel)	Alternate Blocker (n + 2 channel)
BPSK, R1/2 (6Mbps)	-81	-81
BPSK, R3/4 (9Mbps)	-80	-80
QPSK, R1/2 (12Mbps)	-79	-79
QPSK, R3/4 (18Mbps)	-78	-76
16 QAM, R1/2 (24Mbps)	-75	-73
16 QAM, R3/4 (36Mbps)	-70	-72
64 QAM, R2/3 (48Mbps)	-67	-66
64 QAM, R3/4 (54Mbps)	-63	-63

Note: Testing setup is different from the spec.
- set adjacent channel to -63dBm. (or alternate channel to -47dBm).
- lower the desired channel output until FER=10%.

Receive Sensitivity

Modulation/Rate	Typical dBm	IEEE 802.11a requirement dBm
BPSK, R1/2 (6Mbps)	-84	-82
BPSK, R3/4 (9Mbps)	-83	-81
QPSK, R1/2 (12Mbps)	-82	-79
QPSK, R3/4 (18Mbps)	-80	-77
16 QAM, R1/2 (24Mbps)	-77	-74
16 QAM, R3/4 (36Mbps)	-73	-70
64 QAM, R2/3 (48Mbps)	-68	-66
64 QAM, R3/4 (54Mbps)	-64	-65
BPSK, R1/2 Turbo (12Mbps)	-81	-
BPSK, R3/4 Turbo (18Mbps)	-80	-
QPSK, R1/2 Turbo (24Mbps)	-79	-
QPSK, R3/4 Turbo (36Mbps)	-77	-
16 QAM, R1/2 Turbo (48Mbps)	-74	-
16 QAM, R3/4 Turbo (72Mbps)	-70	-

Note: The sensitivity number is based on Frame error rate of 10%.

LED Indicator

There are two LED indicator on the extension of PC Card.

LED	MiniPCI signal	MiniPCI pin number		
LED0 (positive)	LED1_GRNP	11		
LED0 (negative)	LED1_GRNN	13		
LED1 (positive)	LED2_YELP	12		
LED1 (negative)	LED2_YELN	14		

LED Functionality

LED0 (Power)	LED1 (Netowrk)	Meaning	Comments
Slow-rate blink	OFF	Power save mode (default from power up or reset)	
ON	OFF	Awake	The hardware automatically enter this state after exit from power save mode before any other activity. Changes from power save mode to this state might not be visible on the LEDs if the software assumes control of the LED blinking by writing to the PCI configuration register.
Alternate blink	Alternate blink	Looking for network association	Power LED goes ON; Network LED is OFF; then Power LED goes OFF and Network LED goes ON
Slow-rate blink	Slow-rate blink	Associated or joint with network; no activity	
Fast-rate blink	Fast-rate blink	Associated or joint with network; blink rate increases with activity on the network over the air or locally on the network device based on setting of the PCI configuration register	
OFF	OFF	No power applied to the card	

Regulation

US FCC part 15B
Canada TBD
Europe TBD
Japan Telec
Others upon requested

Interoperability

Actiontec is an active member of Wireless Ethernet Compatibility Alliance (WECA).
All Actiontec 802.11a Wireless product will be certified by WECA Wi-fi test to assure interoperability between vendor's of 802.11a.

Operating Conditions

TBD

Dimension

TBD