HM28NA-001

HMC LTE CAT4 NAD MODULE

User Manual V1.2 for certification

FCC ID: LHJ-HM28NA001
IC: 2807E-HM28NA001

Change History

Rev	Date	Change Description	Owner (s)
1.0	04.18.23	Initial.	Liu Pujia
1.1	05.04.23	Add max antenna gain.	Liu Pujia
1.2	05.05.23	Add test antenna info.	Liu Pujia

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Terms and Acronyms

CDMA	Code Division Multiple Access
DCM-TCU	Data Connectivity Module
DRX	Discontinuous Reception
ES	Engineering Sample
FDD	Frequency Division Duplex
GLONASS	GLOBalnaya NAVigatsionnaya Sputnikovaya Sistema
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GSM	Global System for Mobile
HU	Head Unit
HSIC	High Speed Inter-Chip
LTE	Long Term Evolution
LTE-A	LTE Advanced
MP	Mass Production
NAD	Network Access Device
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PHY	Physical Layer
SIM	Subscriber Identity Module
TDD	Time Division Duplex
TSP	Telematics Service Provider
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access

DCU9628 NAD Module

The DCU9628 NAD is the LTE CAT4 embedded modules designed by Continental Automotive Systems, Inc. The modules will be integrated into Data Connectivity Modules (TCUs) or Head Units (HUs) designed and produced by Continental or by a 3rd party for use by automotive OEMs. DCM-TCUs will be installed into vehicles during the OEM's factory assembly process and will not be accessible without use of special tools. Primary use-cases are data-centric with data and voice connections to Telematics Service Providers (TSP).

1 Key Features

1.1 LTE CAT4 NAD Module

1.1.1 Air Interface Support

- 3GPP Rel-10
- LTE FDD CAT4 (up to 150-Mbps DL/50-Mbps UL)
- LTE TDD CAT4 (up to 90-Mbps DL/27-Mbps UL) for TDD Configuration 1
- UMTS: HSUPA CAT6 (up to 5.76-Mbps), HSPA CAT14 (up to 21-Mbps), HSPA CAT14 (up to 21-Mbps)
- TD-SCDMA: CCSA-rel3, HSDPA CAT15 (up to 2.8-Mbps), HSUPA CAT5/6 (up to 2.2-Mbps)
- GSM: EGPRS Rel-10 236.5kbps (MSC33)
- VoLTE - HD Voice
- Embedded Qualcomm Gen8C GNSS
- GPS/GLONASS/Galileo/BeiDou Receiver
- SBAS supported: EGNOS/MSAS/QZSS/WAAS/GAGAN
- Able to track ~40 channels simultaneously
- 10 Hz update rate (under development)
- Position Accuracy of < 6m @ 95% (open sky)
- Acquisition Sensitivity of -149 dBm
- Tracking Sensitivity of -163 dBm
- TTFF Cold/Warm/Hot (open sky, mean) = 29 sec / 27 sec / 1 sec

1.1.2 Processing and Memory Support

- Embedded Application Processor: Cortex A7 @ 1.3-GHz: 256-kB L2
- RAM: LPDDR2: x32 @ 300-MHz: 256-MB
- NVM: NAND: x8: 512-MB

1.1.3 Electrical Interface Support

- Three antenna ports: Cellular Primary, Cellular MIMO/Diversity and GNSS
- One USB 2.0 HS (configured as peripheral) with built-in USB PHY
- One SPI with dedicated chip select
- Three UARTs
- One dedicated I2C interface
- One 1.8V / 3V SIM interfaces
- One I2S/PCM Audio interface
- Ethernet ready via SGMII
- EMMC via SDIO
- JTAG interface

1.2 Package

- 304-pin LGA module of size 34x40x3.5(H) mm

1.3 Band Configurations Supported

Table 1: DCU9628 Band Configuration Support

Model Name	Region	FDD and TDD LTE Band	UMTS	TD SCDMA	GSM
HM28NA-001	US/Canada/Mexico	2, 4, 5, 7, 12, 13, 17,66,~~71*~~	2, 4 ,5		2, 5
HM28NA-001	EU/RU/Middle East	1, 3, 7, 8, 20, 28, 38, 40,41	1, 8		3, 8
HM28CN-001	CN, India	1, 3, 5, 8, 38, 39, 40, 41	1, 8	34, 39	3, 8
HM28KR-001	Korea	1, 3, 5, 7, 8	1		
HM28SA-001	ROW	1, 3, 5, 7, 8, 28, 38, 40	1, 2, 5, 8		2, 3, 5, 8

1.4 NAD Accessibility Requirement during development and certification

HS-USB: Product teams must make sure to provide access to the NAD communication ports to be used during development and certification testing. Please refer to Section 4.10.40 HSIC for further information. The following functionality must be avaialble after the NAD is integrated:

- Access to the NADs HS-USB interface, including AT command, Diagnostics and NMEA ports.
- Ability to conduct basic call processing and data throughout measurements.
- NAD UART for communication using Linux console.

RF Ports: If on-board antennas are used by the product, provisions must be made to support conducted RF measurements on all antenna interfaces: LTE Primary and MIMO and GNSS.

SIM Interface: Electrical performance of the SIM interface is always evaluated during certification testing of the final product. Product teams must insure that the SIM interface can be accessed for testing without degrading its integrity.

2 Regulatory Compliance Notes

2.1 Regulatory compliance notes

2.1.1 FCC:

This device complies with Part 15, Part 22(H), Part 24(E) and Part 27 of the FCC Rules. The FCC ID for this device is LHJ-HM28NA001. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

2.1.2 Industry of Canada:

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions: (1) This device may not cause interference. (2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) L'appareil ne doit pas produire de brouillage; (2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter, except in accordance with FCC/ISED multi-transmitter product procedures.

Cet appareil et son antenne ne doivent pas être situés ou fonctionner en conjonction avec une autre antenne ou un autre émetteur, sauf conformément aux procédures de produits multi-émetteurs FCC/ISED.

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body. Additional testing and certification for SAR will be required if the distance limitation cannot be met.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps. Des tests et une certification supplémentaires pour le SAR seront requis si la limitation de distance ne peut pas être respectée.

2.2 Device Installation and user manual

The HM28NA-001 module is a proprietary product designed and manufactured by Continental Automotive Systems, Inc. for integration into Telematics control units manufactured by Continental Automotive Systems, Inc. for automotive OEMs.

i. The module is limited to installation ONLY in an integrated device manufactured by Continental Automotive Systems, Inc.
ii. During manufacturing process of the integrated device, the module is soldered onto the PCB of the integrated device.
iii. The integrated device must provide RF connectors to external antennas or RF traces to connect the HM28NA-001 modules to antennas inside the integrated device.
iv. Automotive OEM is responsible for ensuring that the end-user has no manual instructions to remove or install module.
v. The module is limited to installation in mobile applications, according to Part 2.1091(b).
vi. No other operation configurations are allowed.
vii. Changes or modifications to this system by other than a facility authorized by Continental could void authorization to use this equipment.
viii. The module does not have a pre-defined antenna. The module must be installed to provide a separation distance of at least 20 cm from all persons and antenna. Under No conditions may an antenna gain be used that would exceed the ERP and EIRP power limit as specified in Part 22, Part 24, and Part 27.
ix. The module must be installed to provide a separation distance of at least 20 cm from all persons and antenna and must not be co-located or operate in conjunction with any other antenna or transmitter, except in accordance with FCC multi-transmitter evaluation procedures as documented in this filing. Additional testing and certification for SAR will be required if the distance limitation cannot be met.
x. The integrator is responsible for fulfilling FCC and IC requirements for the integrated device. The module must be installed to provide a separation distance of at least 20 cm from all persons and antenna. SAR is related to the final product's implementation and should be assessed based on its proximity to human body.

If Continental chooses to re-use modular approval, then the TCU shall be clearly labeled with an external label containing the integrated modem's FCC ID. For example, the label can include text "Contains device with FCC ID: LHJ-HM28NA001 and IC: 2807E-HM28NA001".

2.3 Instruction of OEMs

Continental must instruct the automotive OEM and provide them to include the following information into the car user's manual (i.e. for the DCM):

1. End-users must be provided with transmitter/antenna installation requirements and operating conditions for satisfying RF exposure compliance:
2. A separate section should clearly state "FCC RF Exposure requirements:"
3. Required operating conditions for end users.
4. The antenna used with this device must be installed to provide a separation distance of at least 20cm from all persons, and must not transmit simultaneously with any other transmitter, except in accordance with FCC/ISED multi-transmitter product procedures. Additional testing and certification for SAR will be required if the distance limitation cannot be met.
5. The Maximum ERP/EIRP and maximum antenna gain required for compliance with Parts 15, 22H, 24E and 27.
6. Clear instructions describing the other party's responsibility to obtain station licensing.

2.4 Antenna requirements for user with HM28NA-001 module

The module must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. Additional testing and certification for SAR will be required if the distance limitation cannot be met.

The HM28NA-001 module does not contain internal antennas and external antenna must be provided by the integrator or OEM. Based on FCC OET Bulletin 65 Supplement C and 47 CRF §2.1091 and on RSS-102 Issue 5, for all LTE/WCDMA/GSM operations the maximum antenna gain including cable loss shall not exceed the following values:

- GSM 850: 6.6 dBi
- GSM 1900: 2 dBi
- WCDMA Band 2: 8.5 dBi
- WCDMA Band 4: 6 dBi
- WCDMA Band 5: 10.4 dBi
- LTE Band 2: 9 dBi
- LTE Band 4: 6 dBi
- LTE Band 5: 10.4 dBi
- LTE Band 7: 9 dBi
- LTE Band 12: 9.6 dBi
- LTE Band 13: 10.1 dBi
- LTE Band 17: 9.7 dBi
- LTE Band 66: 6 dBi

The HM28NA-001 module was tested against general test antenna with below spec and max antenna gain above were calculated according to test results with test antenna:

- GSM 850: 0.82 dBi
- GSM 1900: 1.52 dBi
- WCDMA Band 2: 1.52 dBi
- WCDMA Band 4: 0.68 dBi
- WCDMA Band 5: 0.82 dBi
- LTE Band 2: 1.52 dBi
- LTE Band 4: 0.68 dBi
- LTE Band 5: 0.82 dBi
- LTE Band 7: 3.35 dBi
- LTE Band 12: 0.62 dBi
- LTE Band 13: 0.82 dBi
- LTE Band 17: 0.62 dBi
- LTE Band 66: 0.68 dBi

2.5 Material statement

The End-of-Life Vehicle Directive (EVL) must be applied to the HM28NA-001 module. This means that the component is included into the overall vehicle (since it is permanently installed) and if the explanation of the materials used and, if applicable, disposal descriptions from the vehicle manufacturer.

3 Specifications

3.1 Absolute Maximum Ratings (1)

Table 2: Absolute Maximum Ratings

Parameter		MIN	MAX	UNIT
4V_PMD_V	Power management input supply voltage	-0.5	4.60	V
4V_APT_V	Average power tracking input supply voltage	-0.5	4.60	V
4V_PA_BIAS_V	PA bias input supply voltage	-0.5	4.60	V
3V3_WIFI	WIFI input supply – 3.3V	-0.3	3.96	V
1V8_WIFI	WIFI input supply – 1.8V	-0.3	2.16	V
USB VBUS	USB VBUS input supply	-0.3	5.25	V
V_IN see note (3)	Voltage on any “nonpower supply” pin – see below			
	P3 Pad type signals voltage note (3)	-0.3	Pin F3 + 20% (3)	V
	P5 Pad type signals voltage note (3)	-0.3	Pin B9 + 20% (3)	V
	P6 Pad type signals voltage note (3)	-0.3	Pin M9 + 20% (3)	V
	All other “nonpower supply” pins note (3) (4)	-0.3	Vxx + 20% (3) (4)	V
Analog input voltage to GND		-0.3	2.16	V
Power dissipation see note (2)			10.0	W
Storage temperature, T_{stg}		-65	105	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the module. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Power dissipation assume maximum operating current of 2.5A and nominal operating voltage of 4.0V.
(3) Signal pins shall be referenced to their respective Pad Type Supply. **Warning:No voltage shall be applied to signal pins when NAD is powered off.**
(4) Vxx is the supply voltage associated with the input or output pin to which the voltage is applied.

3.2 Recommended Operating Conditions

Over operating temperature range (unless otherwise stated)

Table 3: Recommended Operating Conditions

Parameter			MIN	TYP	MAX	UNIT
4V_PMD_V	Power management input supply voltage	(1)	3.8	4.0	4.2	V
4V_APT_V	Average power tracking input supply voltage	(1)	3.8	4.0	4.2	V
4V_PA_BIAS_V	PA bias input supply voltage	(1)	3.8	4.0	4.2	V
4V_MODULE_IMAX	Total module maximum peak current, all pins	(4)	-	-	2.5	A
4V_PMD_RMS	Power management input supply RMS current	(5)	-	-	300	mA
4V_APT_RMS	Average power tracking input supply RMS current	(5)	-	-	580	mA
4V_PA_BIAS_RMS	PA bias input supply RMS current	(5)	-	-	20	mA
3V3_WIFI_V	WIFI input supply – 3.3V	(1)	3.0	3.3	3.6	V
1V8_WIFI_V	WIFI input supply – 1.8V	(1)	1.7	1.8	1.95	V
USB VBUS_V	USB VBUS input supply	(1)	3.6	5.0	5.25	V
Operating Temperature:	Fully Compliant Operation	(2)	-30		+75	°C
	Extended Operation	(3)	-40		+85	°C

(1) Voltage range includes both DC and AC components, including ripple, overshoot, undershoot or sag.
(2) Module is functional and meets all required RF performance criteria.
(3) Module is functional and may not meet all required RF performance criteria.
(4) Peak module current drain is dominated by 2A GSM pulse, which is on for 0.57-ms and off for 4.03-ms.
(5) RMS current drain measurement period is 5-ms minimum.

3.3 Output Voltage Supplies

Table 4: Output Voltage Supplies

Parameter		MIN	TYP	MAX	UNIT
VREG_L11_1P8	Digital Reference – 1.8V	1.70	1.80	1.95	V
VREG_L11_1P8	Digital Reference – 1.8V	-	-	100	mA

3.4 ESD Ratings

Table 5: ESD Ratings

Parameter				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002	(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011		±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

3.5 Digital Electrical Characteristics

3.5.1 HSIC Characteristics

At 25°C, VDD_PX = 1.2 V (unless otherwise noted)

Table 6: HSIC Characteristics

Parameter		Comments	MIN	MAX	UNIT
VIH	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	-	V
VIL	Low-level input voltage	CMOS/Schmitt	-	0.35 * V_{DD_PX}	V
IIH	Input high leakage current	No pull-down	-	2	uA

IIL	Input low leakage current	No pull-up	-2	-	uA
VOH	High-level output voltage	CMOS, at rated drive strength	0.75 * V_{DD_PX}	-	V
VOL	Low-level output voltage	CMOS, at rated drive strength	-	0.25 * V_{DD_PX}	V
IZ	Tri-state leakage current	No pull, no keeper	-2	2	uA
RP	Pull resistance	Pull-up and pull-down	17	60	kΩ
RK	Keeper resistance		17	60	kΩ
CIN	Input capacitance		-	5	pF

3.5.2 1.8V Digital I/O Characteristics

At 25°C, VDD_PX = 1.8 V (unless otherwise noted)

Table 7: 1.8V Digital I/O Characteristics

Parameter		Comments	MIN	MAX	UNIT
VIH	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	V_{DD_PX} + 0.3	V
VIL	Low-level input voltage	CMOS/Schmitt	-0.3	0.35 * V_{DD_PX}	V
VSHYS	Schmitt hysteresis voltage		100	-	mV
IIH	Input high leakage current	No pull-down	-	1	uA
IIL	Input low leakage current	No pull-up	-1	-	uA
IIHPD	Input high leakage current	With pull-down	27.5	97.5	uA
IILPU	Input low leakage current	With pull-up	-97.5	-27.5	uA
VOH	High-level output voltage	CMOS, at rated drive strength	V_{DD_PX} -0.45	V_{DD_PX}	V
VOL	Low-level output voltage	CMOS, at rated drive strength	0	0.45	V
IOZH	Tri-state leakage current	Logic high out, no pull-down	-	1	uA
IOZL	Tri-state leakage current	Logic low out, no pull-up	-1	-	uA
IOZHPD	Tri-state leakage current	Logic high out with pull-down	27.5	97.5	uA
IOZLPU	Tri-state leakage current	Logic low out with pull-up	-97.5	-27.5	uA
IOZHKP	Tri-state leakage current	Logic high out with keeper	-22.5	-7.5	uA
IOZLKP	Tri-state leakage current	Logic low out with keeper	7.5	22.5	uA
RP	Pull resistance	Pull-up and pull-down	55	390	kΩ
RK	Keeper resistance		30	250	kΩ
CIO	Input capacitance		-	5	pF

3.5.3 SDC Dual Voltage 1.8V/2.85V Digital I/O Characteristics

At 25°C, VDD_PX = 1.8V (unless otherwise noted)

Table 8: SDC 1.8V Digital I/O Characteristics

Parameter		Comments	MIN	MAX	UNIT
VIH	High-level input voltage	CMOS/Schmitt	1.27	2.0	V
VIL	Low-level input voltage	CMOS/Schmitt	-0.3	0.58	V
VSHYS	Schmitt hysteresis voltage		100	-	mV
IIH	Input high leakage current	No pull-down	-	5	uA
IIL	Input low leakage current	No pull-up	-5	-	uA
VOH	High-level output voltage	CMOS, at rated drive strength	1.4	V_{DD_PX}	V
VOL	Low-level output voltage	CMOS, at rated drive strength	0	0.45	V
IOZH	Tri-state leakage current	Logic high out, no pull-down	-	5	uA
IOZL	Tri-state leakage current	Logic low out, no pull-up	-5	-	uA

At 25°C, VDD_PX = 2.85V (unless otherwise noted)

Table 9: SDC 2.85V Digital I/O Characteristics

Parameter	Comments	MIN	MAX	UNIT

VIH	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_PX}	V_{DD_PX} + 0.3	V
VIL	Low-level input voltage	CMOS/Schmitt	-0.3	0.25 * V_{DD_PX}	V
VSHYS	Schmitt hysteresis voltage		100	-	mV
IIH	Input high leakage current	No pull-down	-	10	uA
IIL	Input low leakage current	No pull-up	-10	-	uA
VOH	High-level output voltage	CMOS, at rated drive strength	0.75 * V_{DD_PX}	V_{DD_PX}	V
VOL	Low-level output voltage	CMOS, at rated drive strength	0	0.125 * V_{DD_PX}	V
RP	Pull resistance	Pull-up and pull-down	55	390	kΩ
RK	Keeper resistance		30	250	kΩ
CIO	Input capacitance		-	5	pF

3.5.4 UIM1 Dual Voltage 1.8V/2.85V Digital I/O Characteristics

At 25°C, VDD_PX = 1.8V (unless otherwise noted)

Table 10: UIM1 1.8V Digital I/O Characteristics

Parameter		Comments	MIN	MAX	UNIT
VIH	High-level input voltage	CMOS/Schmitt	0.70 * V_{DD_PX}	V_{DD_PX} + 0.3	V
VIL	Low-level input voltage	CMOS/Schmitt	-0.3	0.2 * V_{DD_PX}	V
VSHYS	Schmitt hysteresis voltage		100	-	mV
IIH	Input high leakage current	No pull-down	-20	20	uA
IIL	Input low leakage current	No pull-up	-	1000	uA
VOH	High-level output voltage	CMOS, at rated drive strength	0.8 * V_{DD_PX}	V_{DD_PX}	V
VOL	Low-level output voltage	CMOS, at rated drive strength	0	0.4	V
IOZH	Tri-state leakage current	Logic high out, no pull-down	-	5	uA
IOZL	Tri-state leakage current	Logic low out, no pull-up	-5	-	uA

At 25°C, VDD_PX = 2.85V (unless otherwise noted)

Table 11: UIM1 2.85V Digital I/O Characteristics

Parameter		Comments	MIN	MAX	UNIT
VIH	High-level input voltage	CMOS/Schmitt	0.70 * V_{DD_PX}	V_{DD_PX} + 0.3	V
VIL	Low-level input voltage	CMOS/Schmitt	-0.3	0.2 * V_{DD_PX}	V
VSHYS	Schmitt hysteresis voltage		100	-	mV
IIH	Input high leakage current	No pull-down	-20	20	uA
IIL	Input low leakage current	No pull-up	-	1000	uA
VOH	High-level output voltage	CMOS, at rated drive strength	0.8 * V_{DD_PX}	V_{DD_PX}	V
VOL	Low-level output voltage	CMOS, at rated drive strength	0	0.4	V
IOZH	Tri-state leakage current	Logic high out, no pull-down	-	10	uA
IOZL	Tri-state leakage current	Logic low out, no pull-up	-10	-	uA

3.5.5 Digital Output Characteristics

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 1) with respect to the drive current per drive table (Table 12). They can be calculated using these relationships:

$$Vol[max] = \left(\frac{\%drivex\ 450}{100}\right) mV$$

$$Voh[min] = Vdd_{px} - \left(\frac{\%drivex\ 450}{100}\right) mV$$

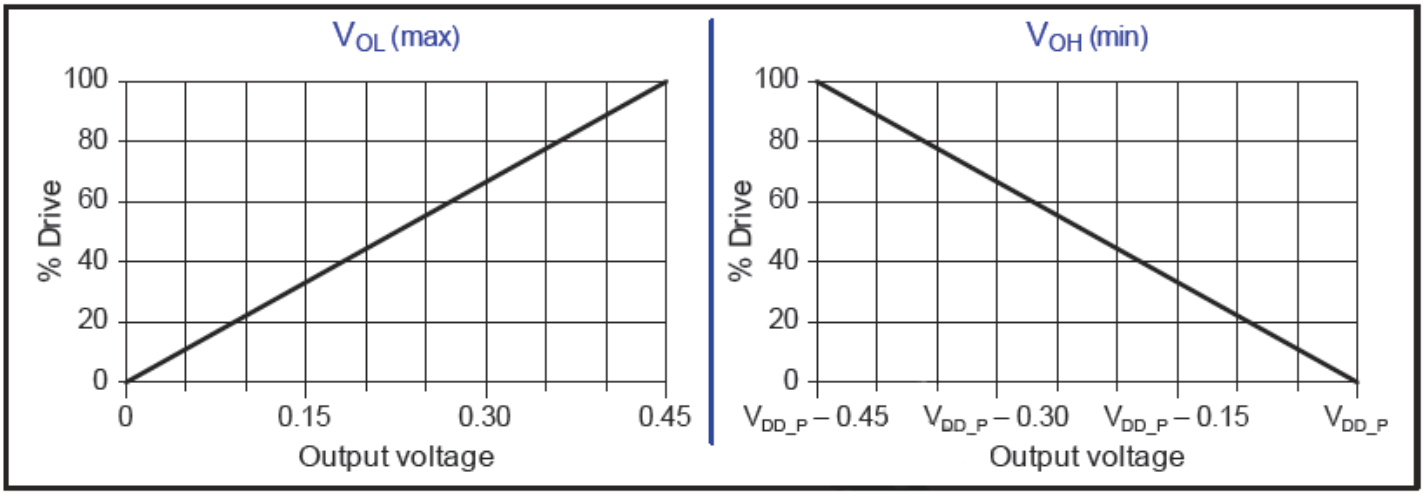

Figure 1: IV curve for VOL and VOH (valid for all VDD_PX)

Table 12: Output Current Drive Strengths

Parameter		Comments	MIN	MAX	UNIT
Iout1	SDC 1.8V	Eight levels, 2-mA steps	2	16	mA
Iout2	SDC 2.85V	Eight levels, 2-mA steps	2	16	mA
Others	All other 1.8V IO	Eight levels, 2-mA steps	2	16	mA

3.6 Timing Characteristics

3.6.1 Secure Digital Interface

Table 13: Supported SD Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
Secure Digital: Physical Layer Specification, version 3.0	None	Timing specifications – see **Table 14**.
SDIO Card Specification, version 3.0	None	

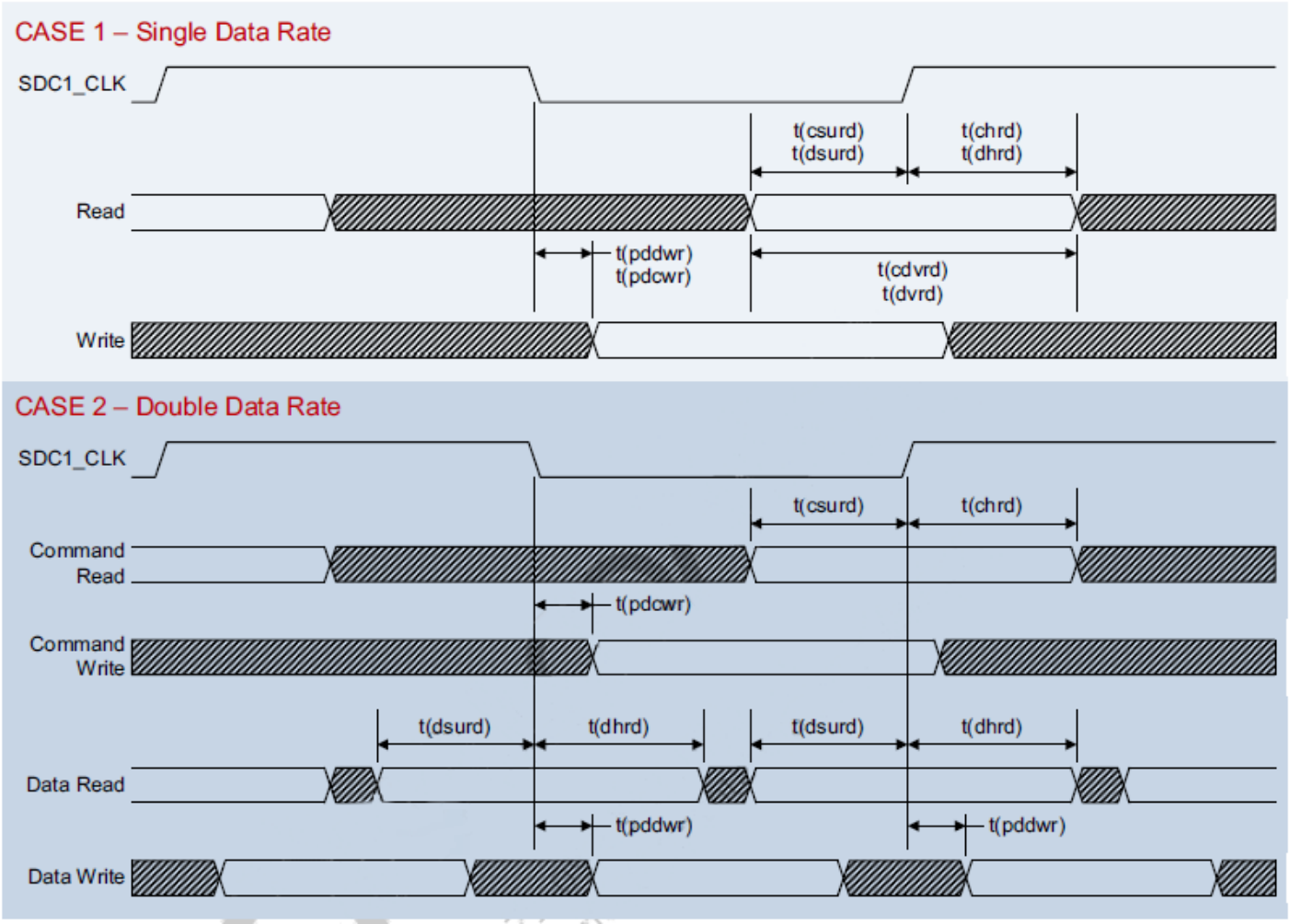

Figure 2: Secure Digital Interface Timing Diagram

Table 14: SDC Interface Timing Characteristics

Parameter		Comments	MIN	MAX	UNIT
Single data rate (SDR) mode – SDC1 up to 200-MHz					
t(cvdrd)	Command valid		2.4	-	ns
t(dvdrd)	Data valid		2.4	-	ns
t(pddwr)	Propagation delay on data write		-1.36	0.76	ns
t(pdcwr)	Propagation delay on command write		-1.36	0.76	ns
Single data rate (SDR) mode – SDC1 up to 100-MHz					
t(chrd)	Command hold		1.5	-	ns
t(csurd)	Command setup		2.5	-	ns
t(dhrd)	Data hold		1.5	-	ns
t(dsurd)	Data setup		2.5	-	ns
t(pddwr)	Propagation delay on data write		-3.7	1.5	ns
t(pdcwr)	Propagation delay on command write		-3.7	1.5	ns
Double data rate (DDR) mode – SDC1 up to 50-MHz					
t(chrd)	Command hold		1.5	-	ns
t(csurd)	Command setup		6.3	-	ns
t(dhrd)	Data hold		1.5	-	ns
t(dsurd)	Data setup		2.0	-	ns
t(pddwr)	Propagation delay on data write		0.8	6.0	ns
t(pdcwr)	Propagation delay on command write		-8.2	3.0	ns

3.6.2 USB 2.0 Interface

Table 15: Supported USB2.0 Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	Low-speed peripheral mode not supported	None
On-The-Go Supplement to USB 2.0 Specification (June 24, 2003, Revision 1.0A or later)	Supports host mode aspect of OTG Only	None

3.6.3 HSIC Interface

Table 16: Supported HSIC Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
High-speed Inter-chip USB Electrical Specification, version 1.0	None	None

3.6.4 I2C Interface

Table 17: Supported I2C Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
I2C Specification, version 5.0, October 2012	None	Multimaster is not supported

3.6.5 UIM Interface

Table 18: Supported UIM Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
ISO/IEC 7816-3	None	None

3.6.6 SPI Interface

The NAD module supports SPI as a master only.

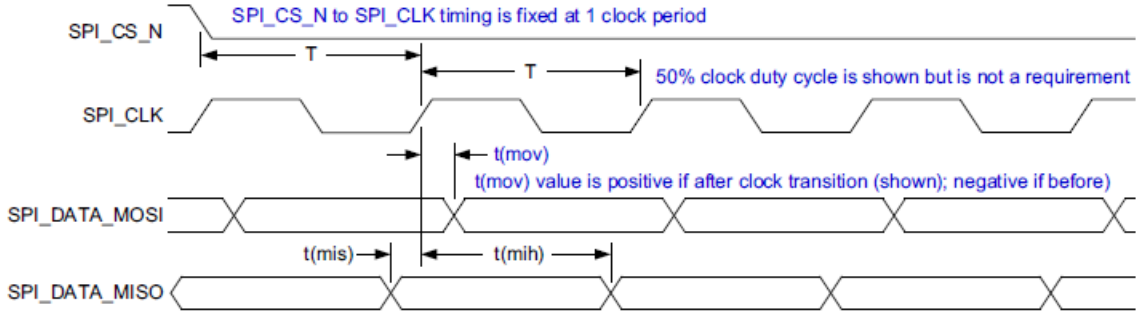

Figure 3: SPI Master Timing Diagram

Table 19: SPI Master Timing Characteristics

Parameter		Comments	MIN	MAX	UNIT
F	SPI Clock Frequency			50	MHz
T	SPI Clock Period		20.0	-	ns
t(ch)	Clock high		9.0	-	ns
t(cl)	Clock low		9.0	-	ns
t(mov)	Master output valid		-5.0	5.0	ns
t(mix)	Master input setup		5.0	-	ns
t(mih)	Master input hold		1.0	-	ns

3.6.7 I2S Interface

Table 20: Supported I2S Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
Phillips I2S Bus Specifications, revised June 5,1996	None	When an external SCK clock is used, a duty cycle of 45% to 55% is required.

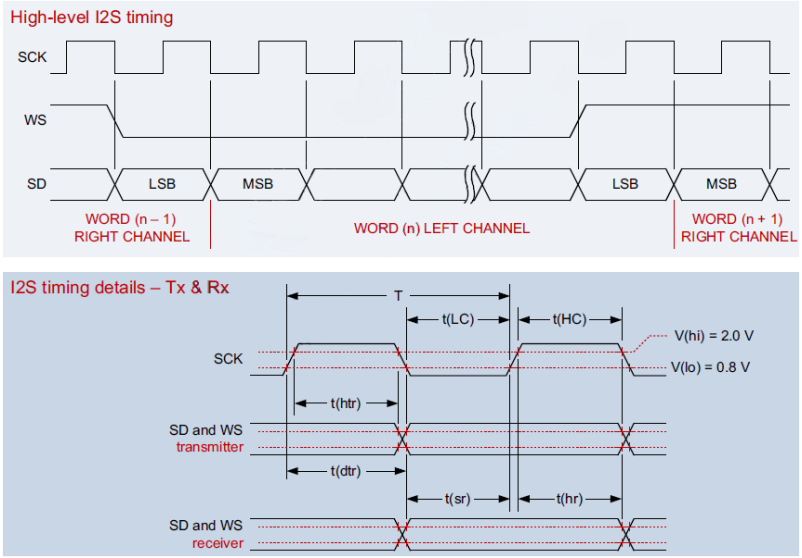

Figure 4: I2S Interface Timing Diagram

3.6.7.1 I2S Interface Timing

Table 21: CAT4 I2S Interface Timing Characteristics

Parameter		Comments (1)	MIN	MAX	UNIT
Using NAD SCK					
F	Frequency		-	12.288	MHz
T	Clock period		81.380	-	ns
t(HC)	Clock high		0.45 x T	0.55 x T	ns
t(LC)	Clock low		0.45 x T	0.55 x T	ns
t(sr)	SD and WS input setup time		16.276	-	ns
t(hr)	SD and WS input hold time		0	-	ns
t(dtr)	SD and WS output delay		-	65.100	ns
t(htr)	SD and WS output hold time		0	-	ns
Using external SCK					
F	Frequency		-	12.288	MHz
T	Clock period		81.380	-	ns
t(HC)	Clock high		0.45 x T	0.55 x T	ns
t(LC)	Clock low		0.45 x T	0.55 x T	ns
t(sr)	SD and WS input setup time		16.276	-	ns
t(hr)	SD and WS input hold time		0	-	ns
t(dtr)	SD and WS output delay		-	65.100	ns
t(htr)	SD and WS output hold time		-1.45	0.85	ns

(1) Load capacitance between 10-pF and 40-pF

3.6.8 External CODEC PCM Interface

3.6.8.1 Short sync (Primary) PCM Interface (2048-kHz clock)

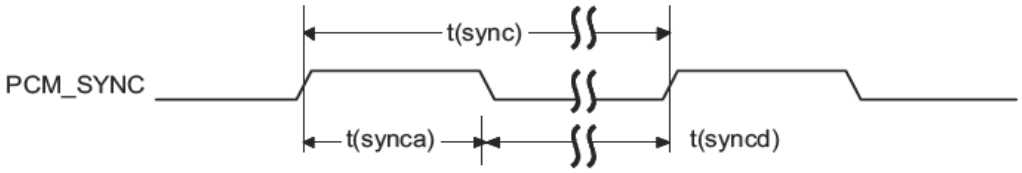

Figure 5: PCM_SYNC Timing Diagram

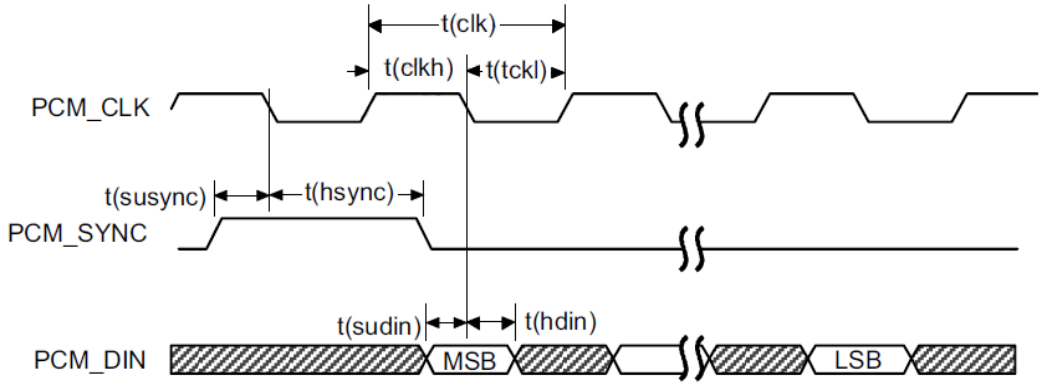

Figure 6: PCM_CODEC to NAD Timing Diagram

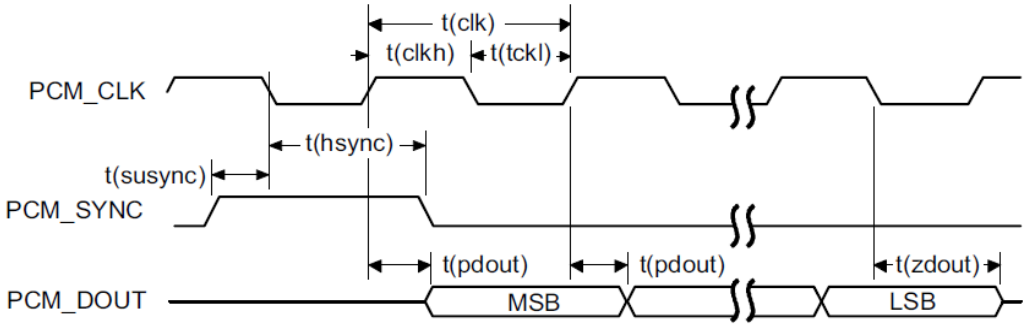

Figure 7: NAD to PCM_CODEC Timing Diagram

3.6.8.2 CAT4 Primary Short Sync PCM Interface Timing

Table 22: Primary Short Sync PCM Interface Timing Characteristics

Parameter		Comments	MIN	TYP	MAX	UNIT
t(sync)	PCM_SYNC cycle time		-	125	-	us
t(synca)	PCM_SYNC asserted time		-	488	-	ns
t(syncd)	PCM_SYNC de-asserted time		-	124.5	-	ns
t(clk)	PCM_CLK cycle time		-	488	-	ns
t(clkh)	PCM_CLK high time		-	244	-	ns
t(clkl)	PCM_CLK low time		-	244	-	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling		-	122	-	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling		60	-	-	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling		10	-	-	Ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid		-	-	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z		-	160	-	ns

3.6.8.3 Long sync (Auxiliary) PCM Interface (128-kHz clock)

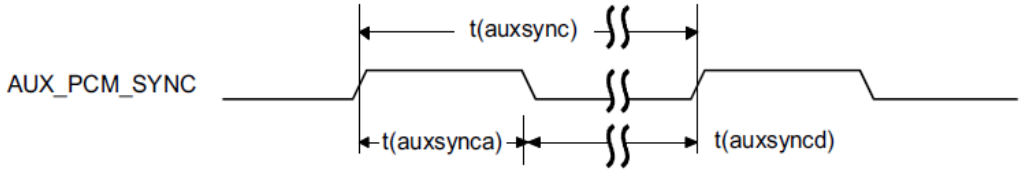

Figure 8: AUX_PCM_SYNC Timing Diagram

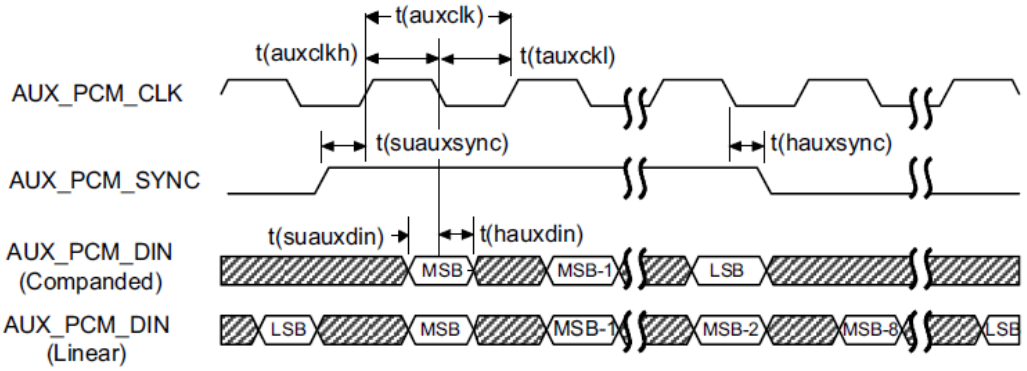

Figure 9: AUX_PCM_CODEC to NAD Timing Diagram

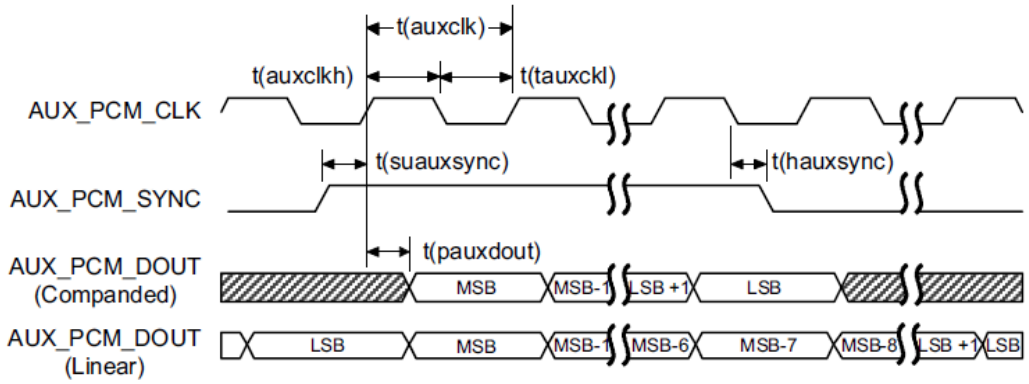

Figure 10: NAD to AUX_PCM_CODEC Timing Diagram

3.6.8.4 CAT4 Auxiliary Long Sync PCM Interface Timing

Table 23: Auxiliary Long Sync PCM Interface Timing Characteristics

Parameter		Comments	MIN	TYP	MAX	UNIT
t(auxsync)	AUX_PCM_SYNC cycle time		-	125	-	us
t(auxsynca)	AUX_PCM_SYNC asserted time		62.4	62.5	-	ns
t(auxsyncd)	AUX_PCM_SYNC de-asserted time		-	124.5	-	ns
t(auxclk)	AUX_PCM_CLK cycle time		-	488	-	ns
t(auxclkh)	AUX_PCM_CLK high time		-	244	-	ns
t(auxclkl)	AUX_PCM_CLK low time		-	244	-	ns
t(suauxsync)	AUX_PCM_SYNC offset time to AUX_PCM_CLK falling		-	122	-	ns
t(huauxsync)	AUX_PCM_SYNC offset time to AUX_PCM_CLK falling		-	122	-	ns
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling		60	-	-	ns
t(hauxdin)	AUX_PCM_DIN hold time after AUX_PCM_CLK falling		10	-	-	Ns
t(pauxdout)	Delay from AUX_PCM_CLK rising to AUX_PCM_DOUT valid		-	-	60	ns
t(zdout)	Delay from AUX_PCM_CLK falling to AUX_PCM_DOUT HIGH-Z		-	160	-	ns

3.6.9 SGMII Interface

Table 24: Supported SGMII Standards and Exceptions

Applicable Standard	Feature Exceptions	Device Variations
Serial-GMII Specification, ENG-46158, Revision 1.8 or later	None	None

3.6.10 MDIO Interface

The MDIO interface is implemented by two signals:

1. MDC clock – driven by the MAC device to the PHY.

2. MDIO data – bidirectional, the PHY drives it to provide register data at the end of a read operation.

The bus only supports a single MAC as the master, and can have up to 32 PHY slaves.

The MDC can be periodic, with a minimum period of 400-ns, which corresponds to a maximum frequency of 2.5-MHz.

The MDIO requires a specific pull-up resistor of 1.5-kOhms, taking into account the total worst-case leakage current of 32 PHYs and one MAC.

Before a register access, PHY devices generally require a preamble of 32 ones to be sent by the MAC on the MDIO line. The access consists of 16 control bits, followed by 16 data bits. The control bits consist of 2 start bits, 2 access type bits (read or write), the PHY address (5 bits), and the register address (5 bits).

During a write command, the MAC provides address and data. For a read command, the PHY takes over the bus at the end of the address bits transmission to supply the MAC with the register data requested.

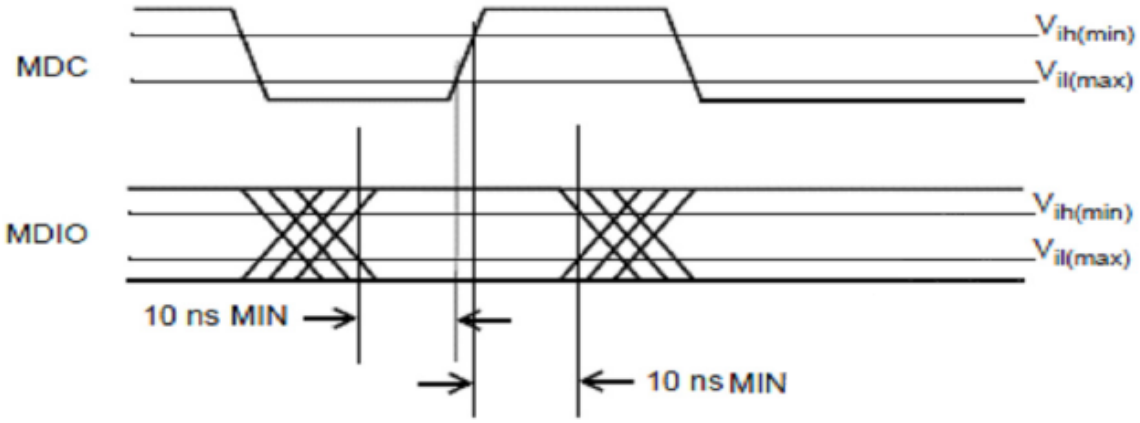

Figure 11: MDIO Input Timing Diagram

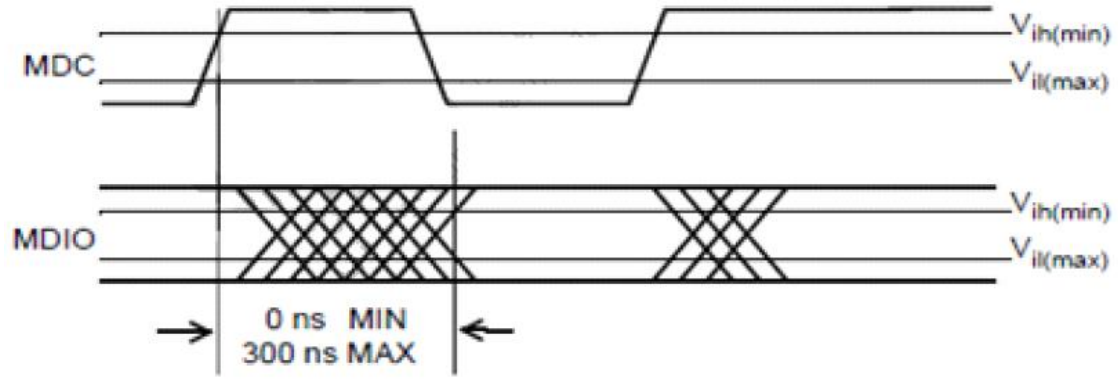

Figure 12: MDIO Output Timing Diagram

3.6.1 Internal Device Frequencies

The table below summarizes the frequencies generated within the NAD for reference only.

Table 25: Internal Device Frequencies

Subsystem/Feature	Frequency	UNIT
PCM Audio Interface	16.0, 512.0	kHz
SPI Interface (Variable, MAX Listed)	50.0	MHz
Fundamental Clock, TCXO_OUT	19.2	MHz
GPLL0	800.0	MHz
GPLL1	614.4	MHz
GPLL2	480.0	MHz
BMIC_PLL	600.6	MHz
MPLL1	576.0	MHz
MPLL2	691.0	MHz
A7SSPLL (Variable, MAX Listed)	1305.6	MHz
NoC Bus (Internal Bus) – Mode Dependent	19.2, 50.0, 100.0, 133.33	MHz
RPM (Cortex-M3) – Depends on Mode	19.2, 100.0, 177.8, 200.0	MHz
APSS (Cortex-A7) – Depends on Mode	400.0, 800.0, 998.4, 1094.4, 1248.0, 1305.6	MHz
LPDDR2 Bus– Depends on Mode	9.6, 48.0, 96.0, 120.0, 150.15, 240.0, 300.3	MHz
Modem Processor – Depends on Mode	115.2, 144.0, 230.4, 288.0, 284.0, 480.0, 576.0, 615.2, 691.2	MHz
USB 2.0 High Speed Mode	240.0	MHz
PMIC Switching Power Supplies	1.60, 1.74, 1.92, 2.13, 2.40, 2.74, 3.20, 3.84, 4.80, 6.40	MHz
Real Time Clock	32.768	kHz

3.7 NAD Module RF Characteristics

3.7.1 NAD Module RF Transmitter Output Power

The Transmitter Power at the NAD antenna terminal at Room Temperature. (not the Fakra of the evaluation board or the Telematics/parent module):

GSM low bands (850/900): +32.5dBm ±1.0 dB (Room Temp.), +1.0/-3.0 (Extreme Temp.)
GSM high bands (1800/1900): +29.5dBm ±1.0 dB (Room Temp.), +1.0/-3.0 (Extreme Temp.)
EDGE low bands (850/900): +26.5dBm ±1.0 dB (Room Temp.), +1.0/-3.0 (Extreme Temp.)
EDGE high bands (1800/1900): +25.5dBm ±1.0 dB (Room Temp.), +1.0/-3.0 (Extreme Temp.)
WCDMA bands: +23.5dBm ±1.0 dB
LTE bands: +23.0dBm ±1.0 dB

Table 26: GSM Multi-slot power reduction

Band	GSM Multi-slot power level according to NV items			GSM Multi-slot maximum output power reduction as declared in certification		
	2 slots	3 slots	4 slots	2 slots	3 slots	4 slots
GSM850	31.0 dBm	29.5 dBm	28.5 dBm	1.5 dB	3.5 dB	4.5 dB
EDGE850	25.5 dBm	24.0 dBm	23.0 dBm	2.0 dB	3.0 dB	4.0 dB
GSM1900	28.0 dBm	26.5 dBm	24.5 dBm	1.5 dB	3.5 dB	4.5 dB
EDGE1900	25.5 dBm	24.0 dBm	23.0 dBm	2.0 dB	3.0 dB	4.0 dB

Note: Tune up tolerance should be considered. These tables reflect the currently certified variants.

3.7.2 NAD Module RF Receiver Sensitivity

The Receiver Sensitivity at the NAD antenna terminal at Room Temperature (not the Fakra of the evaluation board or the Telematics/parent module):

GSM low bands (800/900):	3GPP TS 51.010-1 Section 14.2
WCDMA bands:	3GPP TS 34.121-1 Section 6.2
LTE bands:	3GPP TS GPP 36.521 Section 7
TD-SCDMA bands:	TBD

4 Mechanical Information

4.1 Module Exploded View

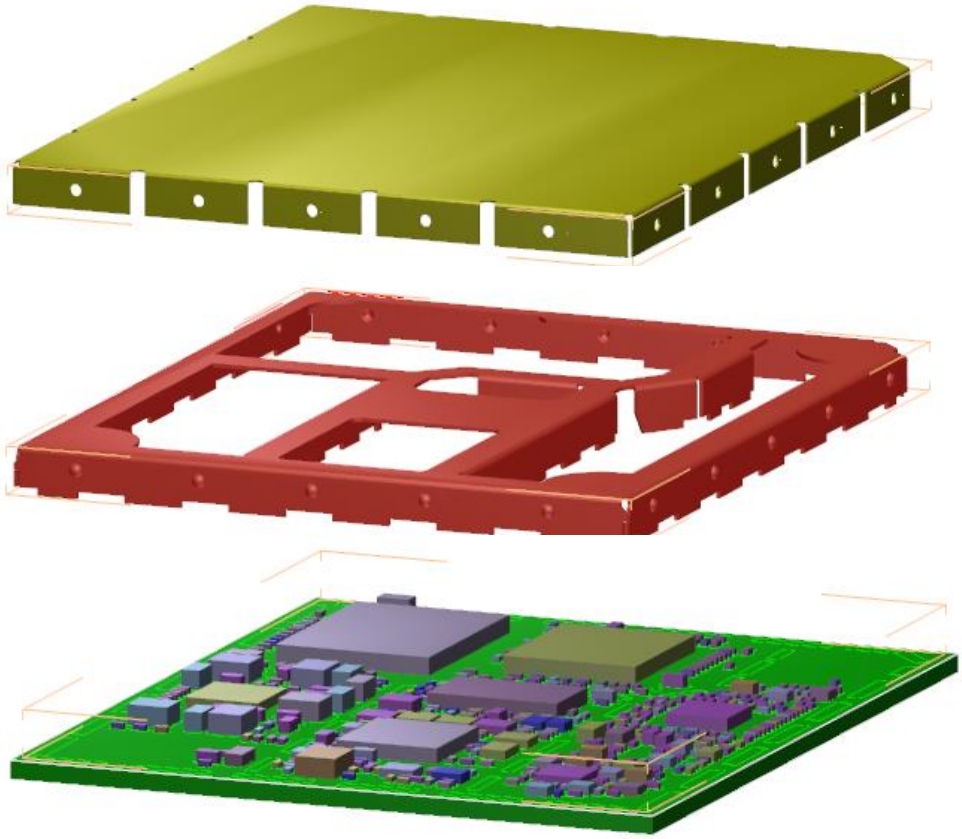

Figure 13: Module Exploded View (an example for illustrative purposes only)

1: Cover
2: Shield
3: PCB Assembly

4.2 Module Top and side Views

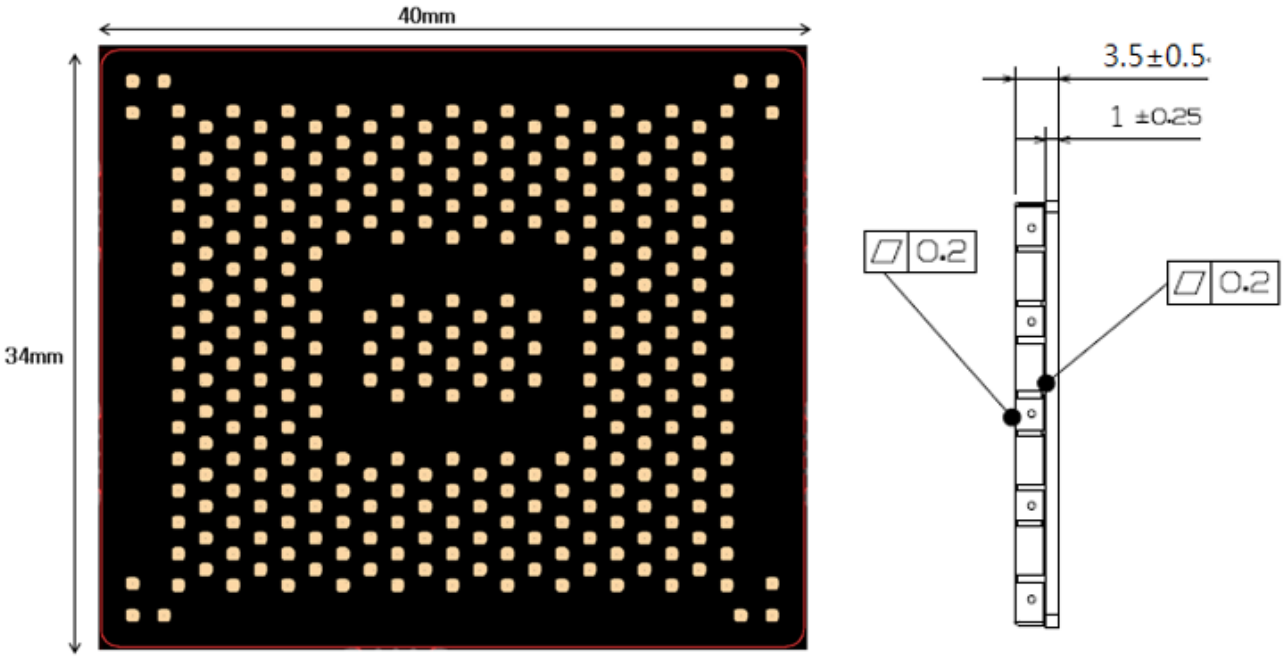

Figure 14: Module Top and Side Views

All dimensions are in mm.

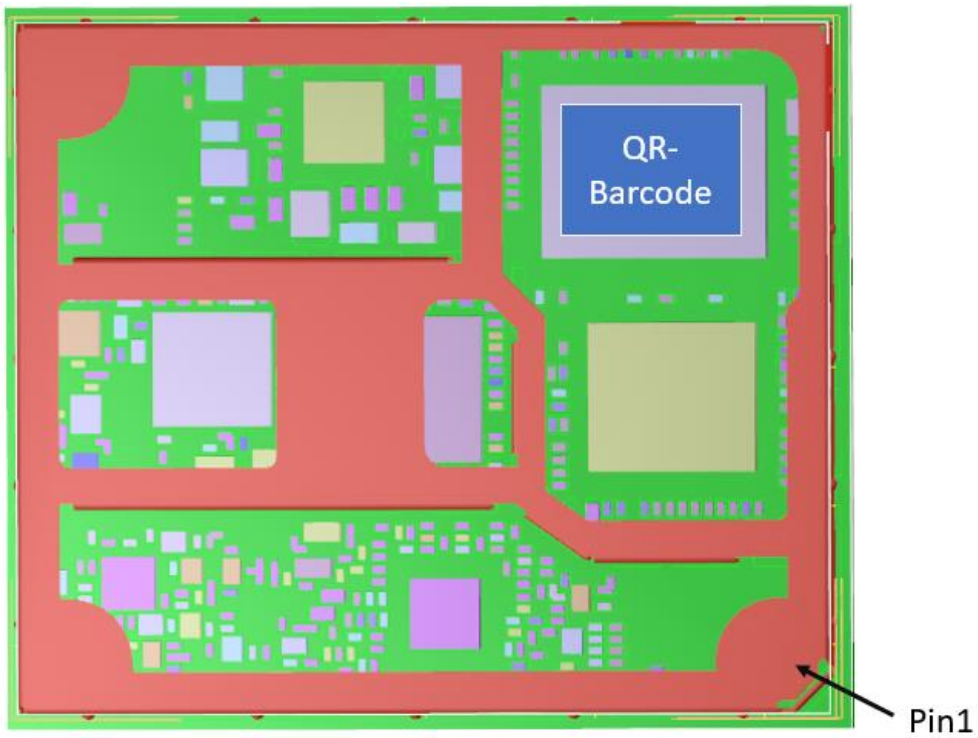

Figure 15: cover placement

Pin 1 is aligned with the corner. Note the label placement.

5 Storage and Handling

5.1 Moisture Sensitivity Level (MSL)

All NAD modules are moisture sensitive and should be kept in their sealed moisture resistant bags until ready for assembly onto the DCM-TCU via the soldering process. Any parts that are not used immediately should be properly resealed in the same moisture resistant bag using appropriate equipment or placed into a dry box until they are needed again. The moisture sensitivity level (MSL) shown below is the amount of time the NAD modules may be exposed before this action must be taken. If the allowed MSL time elapses, the NAD modules must be baked per standard protocol to remove moisture.

Moisture Sensitivity Level: MSL Level 3 (1 Week)

This remainder of this section will be completed in a future release of this document.

6 Part Reliability

This section will be completed in a future release of this document.

7 Certification Information

7.1 NAD—Level Certifications Planned by the TP Certification Team:

Variant	Regulatory	3GPP	MNO	comment
HM28EU-001	CE-RED	GCF	Vodafone	
HM28NA-001	FCC/ISED	PTCRB/GCF	Verizon, Bell, Telcel	
HM28CN-001	NAL (pre-test)	-	China Unicom (pre-test)	
HM28KR-001	KC	GCF	KT, SKT, LG U+	
HM28SA-001	CE(RED)/RCM	GCF	Optus, Singtel, Vivo	