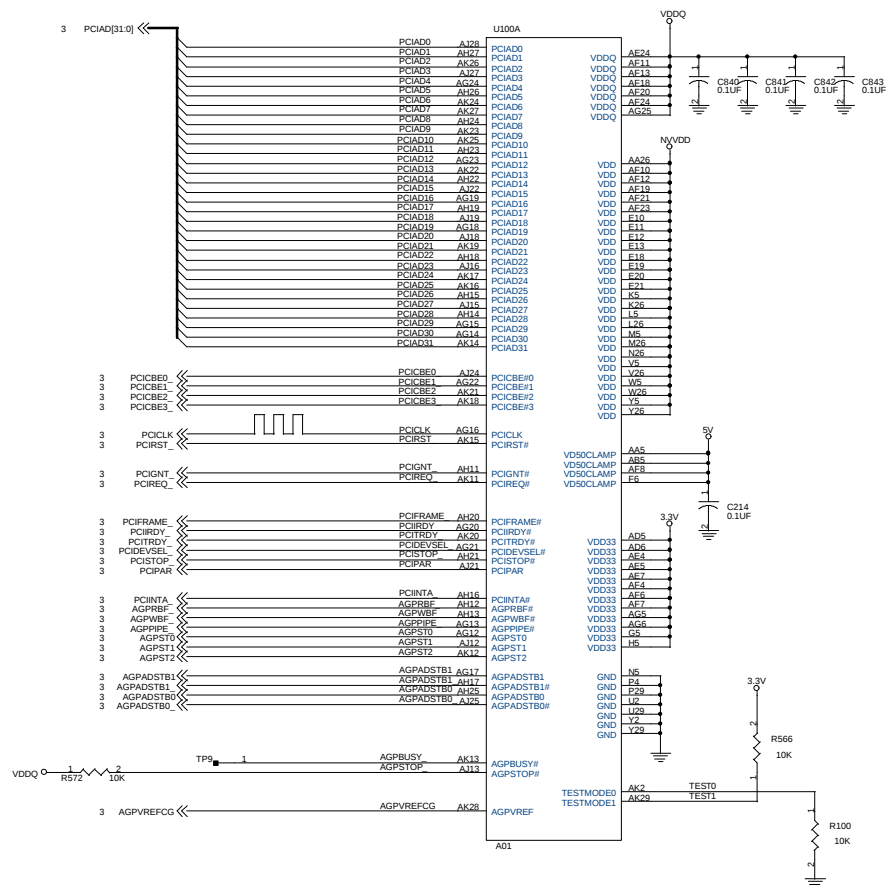
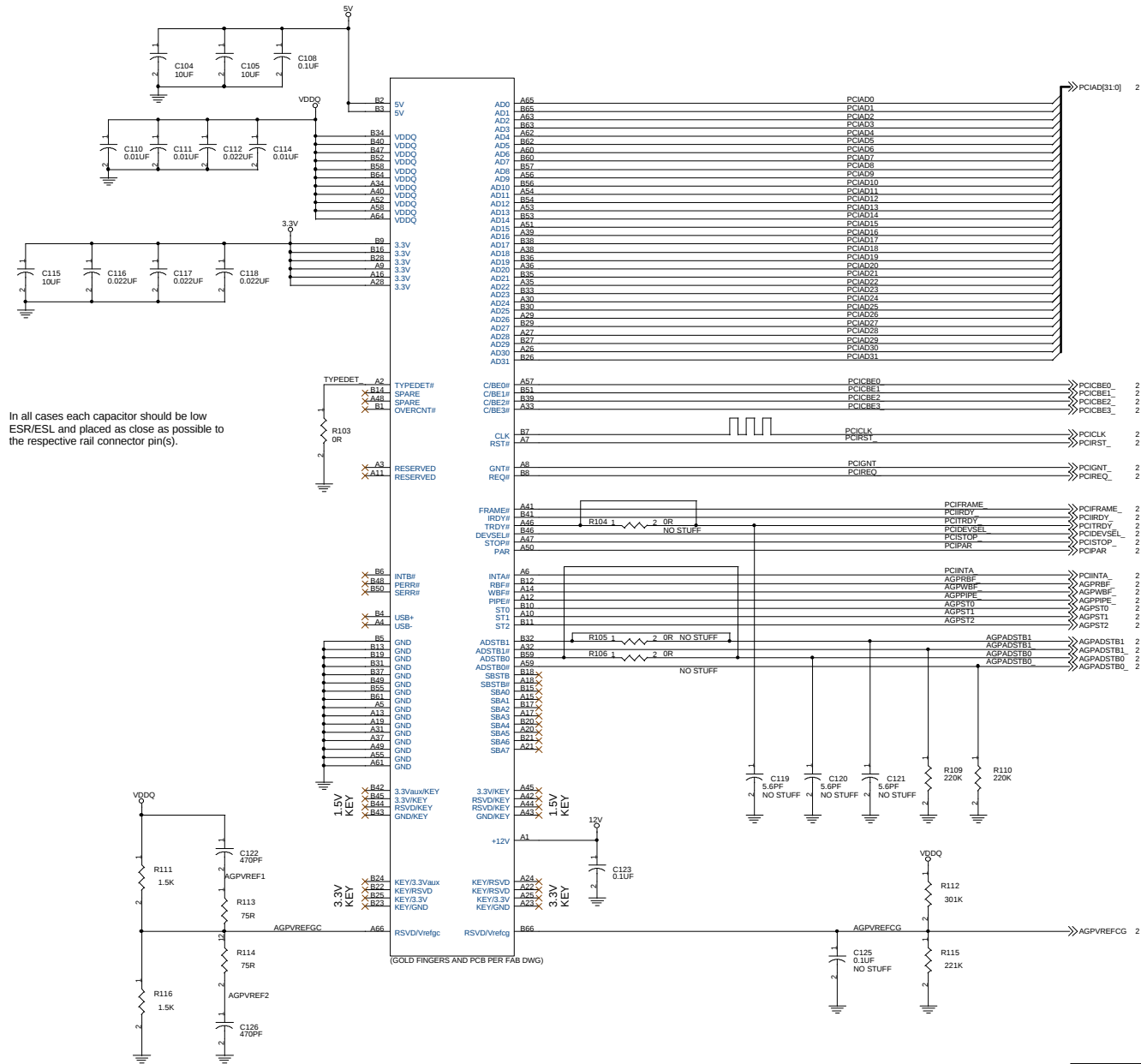


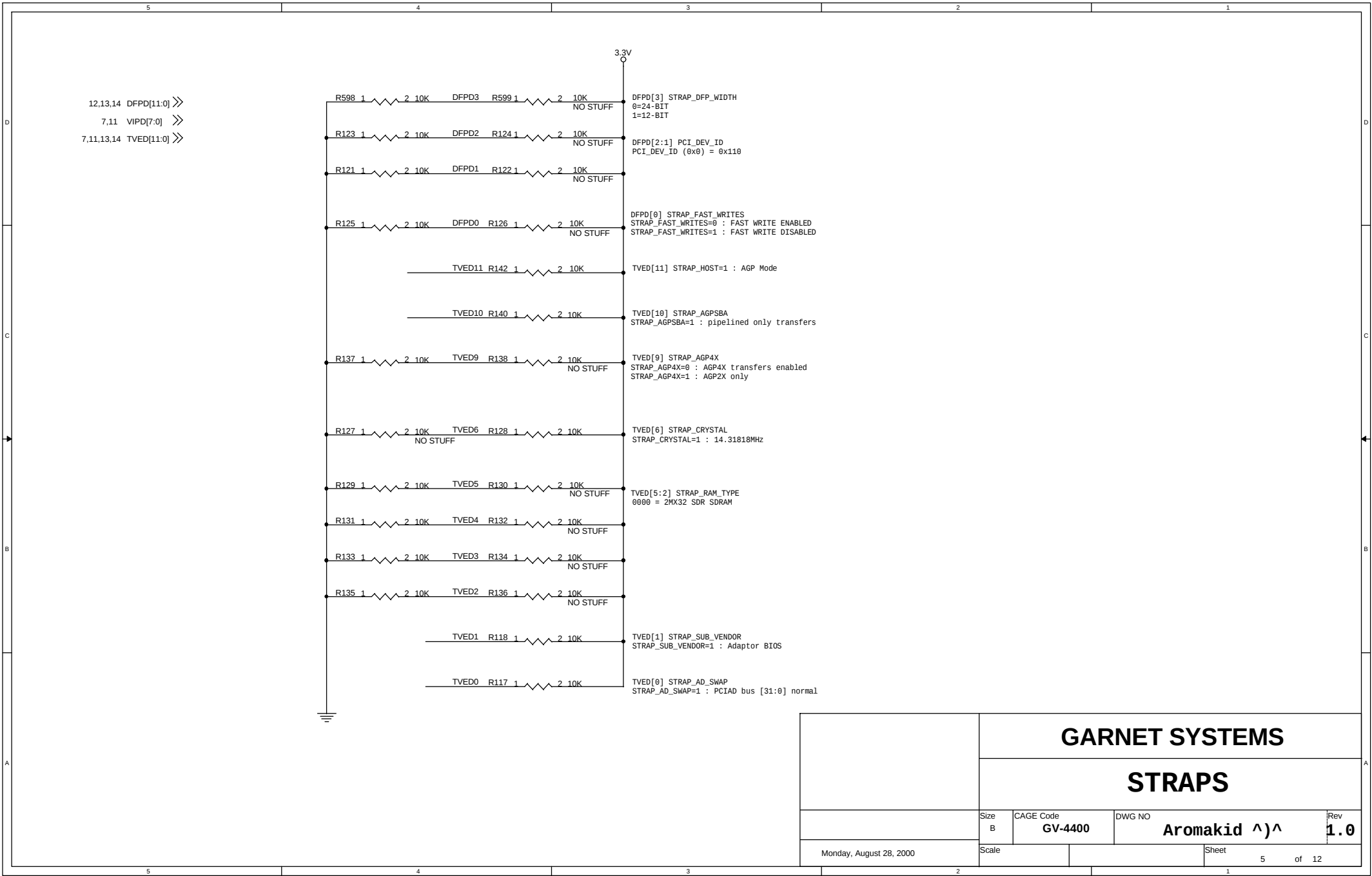
GARNET SYSTEMS				
GeForce2 MX HOST				
Size	C	CAGE Code	DWG NO	Rev
		GV-4400	Aromakid ^)^	1.0
Monday, August 28, 2000	Scale		Sheet	2 of 12

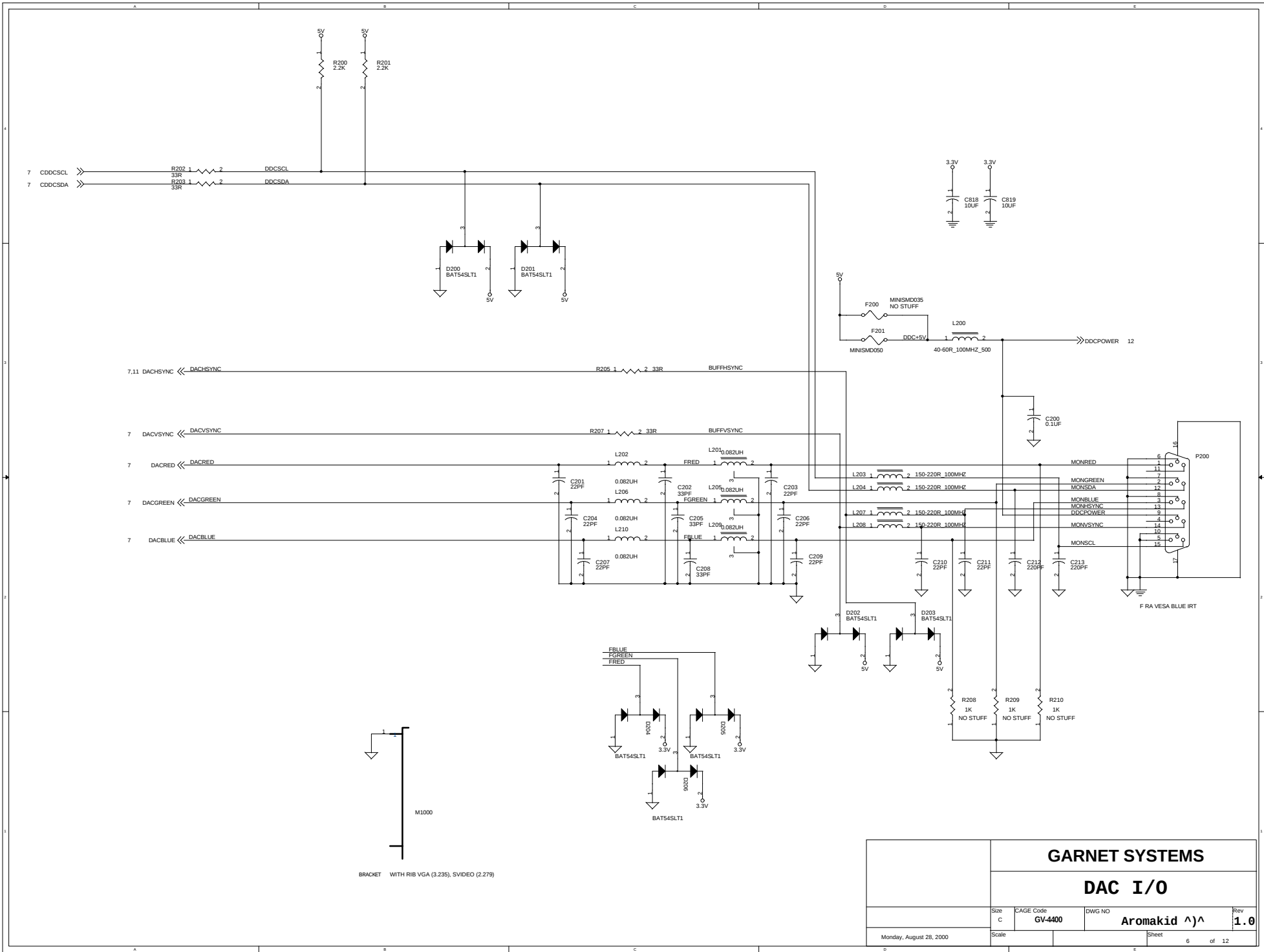
In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).



GARNET SYSTEMS				
AGP I/O				
Size	CAGE Code	DWG NO	Rev	
C	GV-4400	Aromakid ^)^	1.0	
Monday, August 28, 2000	Scale	Sheet	3	of 12

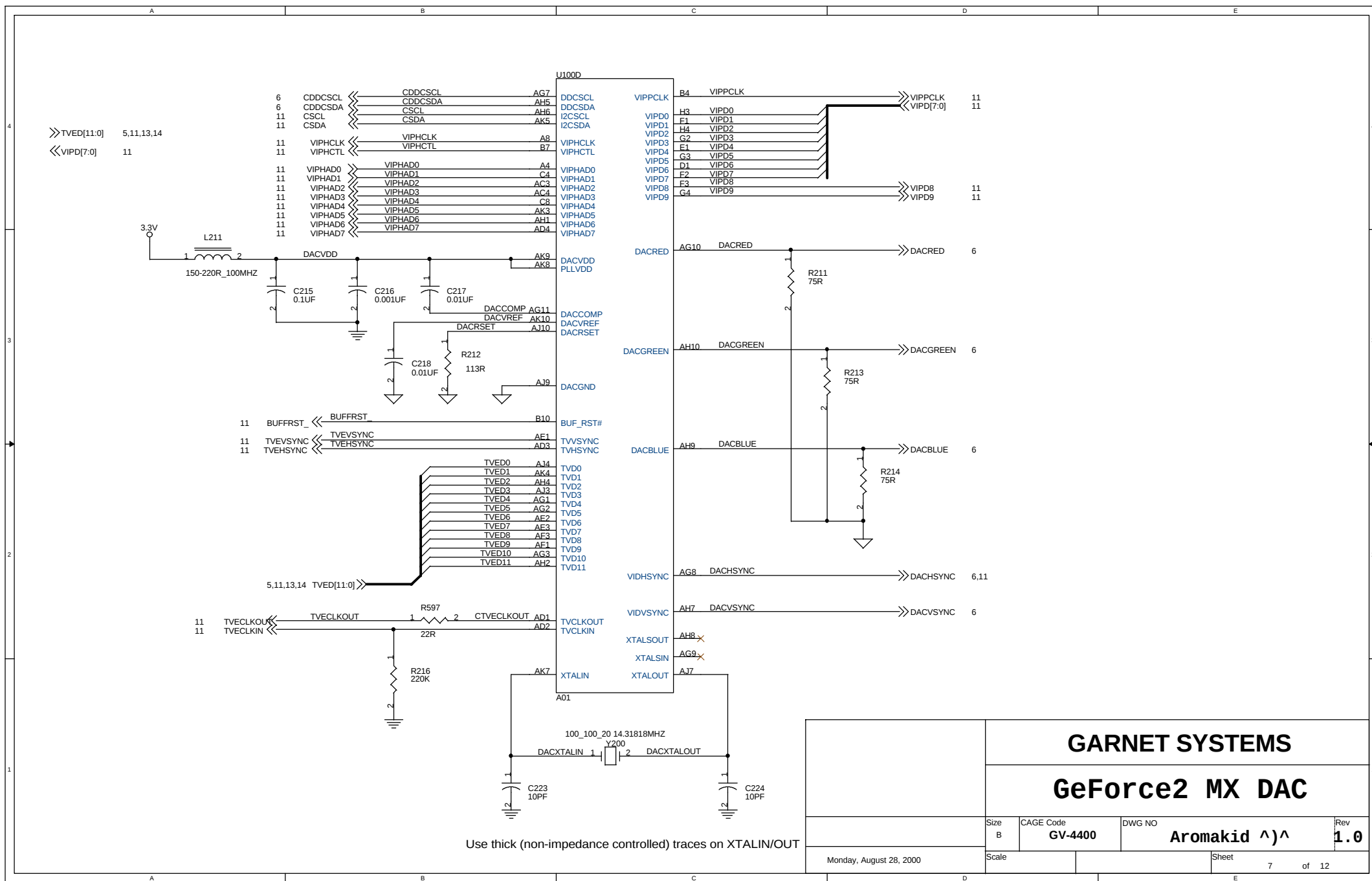
[illegible]

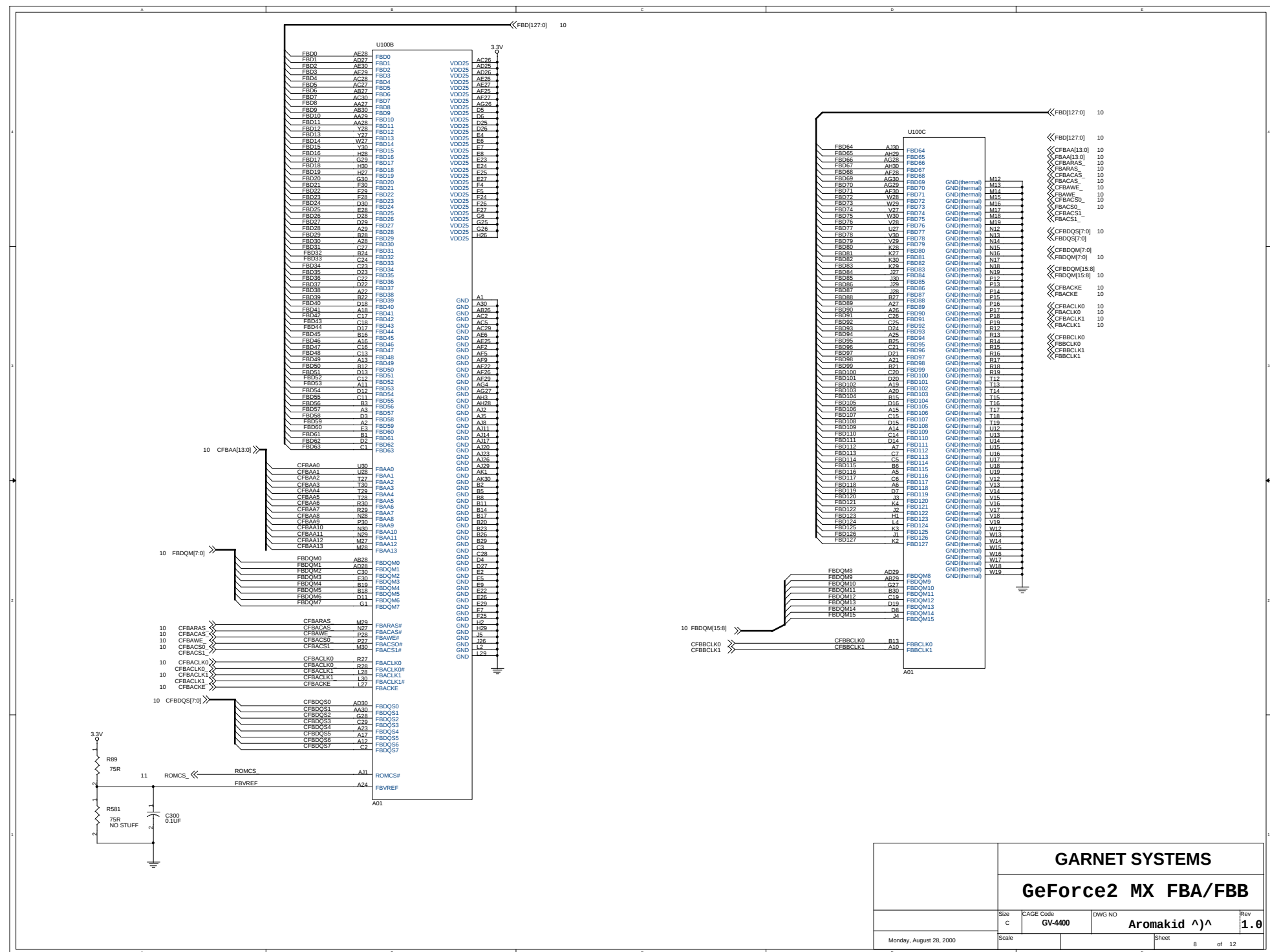


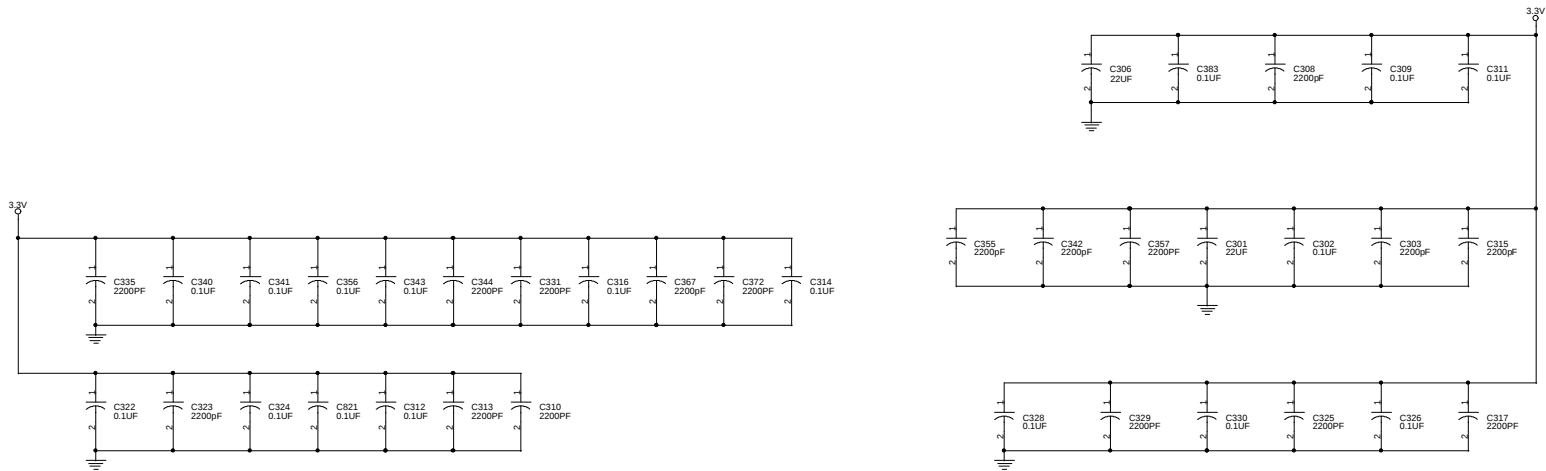


BRACKET WITH RIB VGA (3.235), SVIDEO (2.279)

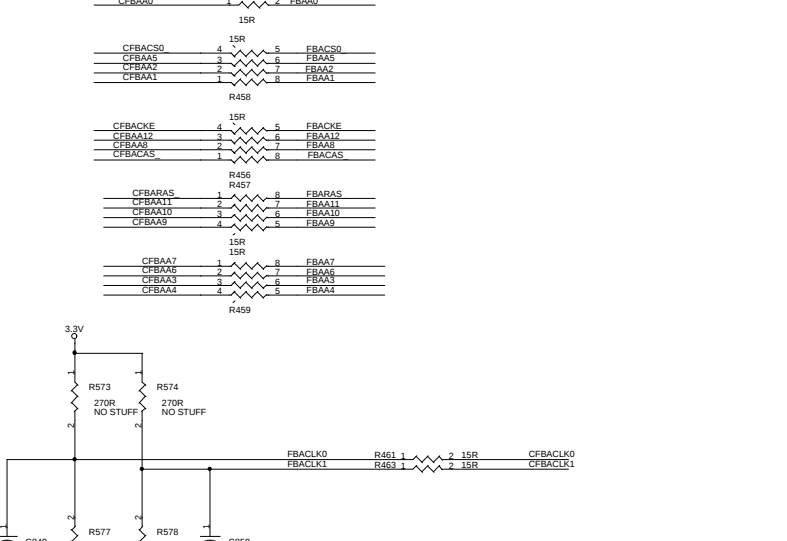
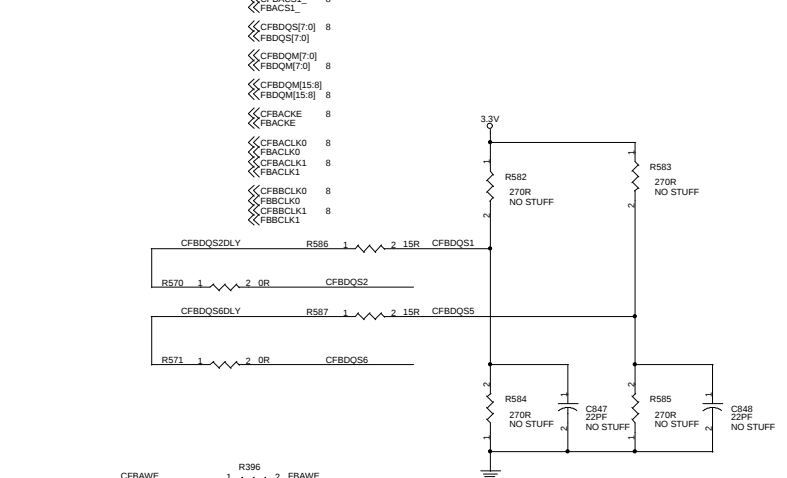
GARNET SYSTEMS			
DAC I/O			
Size C	CAGE Code GV-4400	DWG NO Aromakid ^)^	Rev 1.0
Monday, August 28, 2000	Scale	Sheet 6	of 12



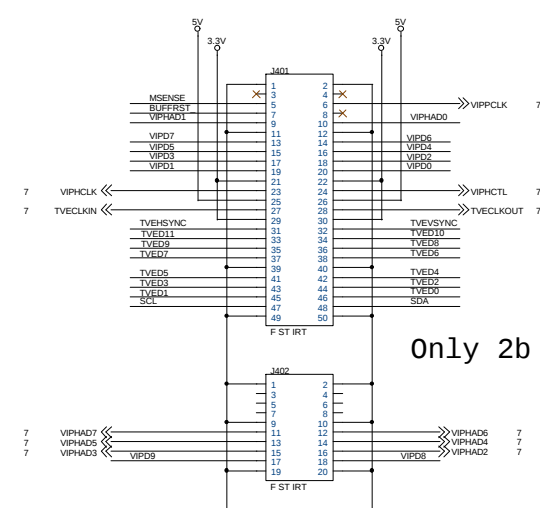
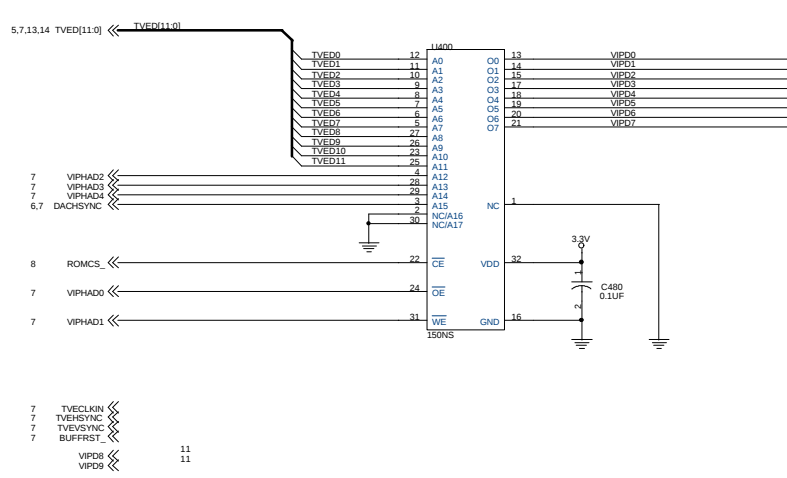
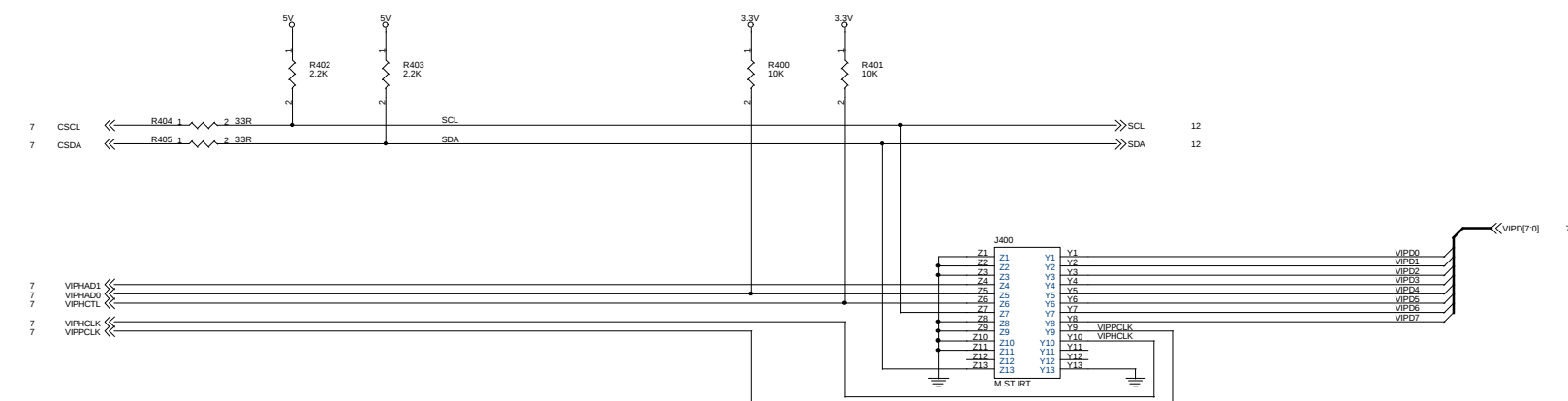




		GARNET SYSTEMS		
		FB DECOUPLING		
	Size C	CAGE Code GV-4400	DWG NO Aromakid ^)^^	Rev 1.0
Monday, August 28, 2000	Scale		Sheet 9	of 12



	GARNET SYSTEMS			
	FBA 2MX32 SDRAM			
	Size C	CAGE Code GV-4400	DWG NO Aromakid ^)^	Rev 1.0
Monday, August 28, 2000	Scale		Sheet	10 of 12



Only 2b host/16b data supported.

VIPHAD[7:2]=VIPD[15:10]
(thru pin muxing)

GARNET SYSTEMS			
ROM VIP & VIDEO IF			
Size	CAGE Code	DWG NO	Rev
C	GV-4400	Aromakid ^)^	1.0
Monday, August 28, 2000	Scale	Sheet	11 of 12

