Circuit Description

1 PRODUCT DESCRIPTION

The GH3052 is a 2.4GHz 40 Channels Analog Modulation Cordless Phone with Digital Answer Machine, Type I, II Caller ID and Full-duplex speakerphone. The unit is capable of either tone or pulse dialing. The internal power supply's isolation is accomplished through a power transformer having an adequate dielectric rating. The circuit wiring is consistent under the requirement of part 68.

The handset unit consists of a keypad with twelve standard keys (0,.. 9, * and #), six function keys (Calls, Del, Memo, Flash, Redial, Volume), and one channel switch key. A Talk key is provided to control pick/release telephone line in a toggle base.

The base unit has a page key, which is used to page the handset unit. It also consists a speaker key for answering incoming calls.

Connection between the device and the telephone network is accomplished through the use of USOC RJ11C in the 2-wire loop calling central office line.

2 BASE UNIT

CPU

The host of base unit is the CPU, DU2. It has two system clocks: 32.768KHz for power down mode and 3.579545MHz for normal mode. It controls the RF combo IC on RF module for wireless communication with handset, DSP chip to provide digital answering machine function, speakerphone and signal path controls. It also handles keyboard and switches scanning, LEDs control, and power managements.

The chip, besides, in charge of Caller ID and Call ID on Call Waiting detection, DTMF generation, ring detection and line states control.

DSP

Another heart of the base unit is digital signal processing IC, DU3. It is a single chip that includes a Digital Signal Processor (DSP), CODECs, Analog Front End, and an interface to external RAM and ROM. It is fully controlled by the system Host, DU2, through a simple interface protocol . The Host provides activation and control of all system functions such as speech recording and playback, memory management, DTMF detection and tone generation, Voice Prompting, True FULL Duplex Speakerphone.

The system clock of the chip is generated from a 4.096MHz crystal and it is multiplied to around 57MHz from internal frequency multiplier to provide 8.0KHz sampling rate of voice recording.

The Analog Front End includes audio signal path switches, mic pre-amplifier and speaker power amplifier to interconnect all signals from/to telephone line and RF module.

RF module

The RF module is mainly formed by Combo IC, U2; low loss amplifier Q26, Q27, FLT2; RX mixer, Q28; IF amplifier Q29, F2, F3; RX VCO, Q30, D2; TX VCO, Q23, D1 and frequency tripler Q24; power amplifier, Q25, FLT1.

The most important part of the module is combo IC that provide TX, RX PLL for VCOs, demodulator, Compandor, battery level detect, mic per-amplifier and receiver power amplifier. It is controlled by CPU via serial linking.

In the receiving path, the RX signal is filtered and amplified on LNA and then converted to IF signal 10.7MHz at the mixer. An 8xxMHz signal is generated on RX VCO, which is controlled

by RX PLL and feed into mixer to mix the IF signal. The signal is demodulate and expanding on combo IC to reproduce audio signal.

In the transmitting path, the audio signal is converted to 8xxMHz signal on TX VCO, which is controlled by TX PLL. The signal is tripled to 2.4GMz RF signal on frequency tripler. Finally, the RF signal is amplified and filter then feed to antenna.

Antenna

Two separated 1/4 wavelength antennas attached on RF module permanently for transmitting and receiving RF signals.

Line Interface Circuit

Line interface circuit, T3, DU6 provides the hybrid 2-to-4 conversion to communicate handset or speakerphone to telephone line. It also included the branch phone reset detection circuit, BQ3, DU6; ringing detection circuit, BC6, BZ2,3, BU2; Line state control circuit, BK1, BQ5, BQ6. The internal telephone line isolation is accomplished through the transformer, T3; Opto-couler IC, BU2; Relay, BK1 and two 10M Ohm resister BR12,16.

3 HANDSET UNIT

CPU

The heart of base unit also is the CPU, HU1. It has two system clocks: 32.768KHz for power down mode and 3.579545MHz for normal mode. It controls the RF combo IC on RF module for wireless communication with base unit. It also handles LCD display, keyboard scanning, LEDs control, buzzer control and power managements.

RF module

The RF module is mainly formed by Combo IC, U2; low loss amplifier Q26, Q27, FLT2; RX mixer, Q28; IF amplifier Q29, F2, F3; RX VCO, Q30, D2; TX VCO, Q23, D1 and frequency tripler Q24; power amplifier, Q25, FLT1.

The most important part of the module is combo IC that provide TX, RX PLL for VCOs, demodulator, Compandor, battery level detect, mic per-amplifier and receiver power amplifier. It is controlled by CPU via serial linking.

In the receiving path, the RX signal is filtered and amplified on LNA and then converted to IF signal 10.7MHz at the mixer. An 8xxMHz signal is generated on RX VCO, which is controlled by RX PLL and feed into mixer to mix the IF signal. The signal is demodulate and expanding on combo IC to reproduce audio signal. Finally, the audio signal is amplified on power amplifier and connects to receiver or headset via headset jack.

In the transmitting path, the audio signal is converted to 8xxMHz signal on TX VCO, which is controlled by TX PLL. The signal is tripled to 2.4GMz RF signal on frequency tripler. Finally, the RF signal is amplified and filter then feed to antenna.

Antenna

Two separated 1/4 wavelength antennas attached on RF module permanently for transmitting and receiving RF signals.

Channel frequencies (MHz)

CH.	BASE TX	H/S TX	CH.	BASE TX	HS/TX
1	2400.75	2472.75	21	2403.75	2475.75
2	2400.9	2472.9	22	2403.9	2475.9
3	2401.05	2473.05	23	2404.05	2476.05
4	2401.2	2473.2	24	2404.2	2476.2
5	2401.35	2473.35	25	2404.35	2476.35
6	2401.5	2473.5	26	2404.5	2476.5
7	2401.65	2473.65	27	2404.65	2476.65
8	2401.8	2473.8	28	2404.8	2476.8
9	2401.95	2473.95	29	2404.95	2476.95
10	2402.1	2474.1	30	2405.1	2477.1
11	2402.25	2474.25	31	2405.25	2477.25
12	2402.4	2474.4	32	2405.4	2477.4
13	2402.55	2474.55	33	2405.55	2477.55
14	2402.7	2474.7	34	2405.7	2477.7
15	2402.85	2474.85	35	2405.85	2477.85
16	2403	2475	36	2406	2478
17	2403.15	2475.15	37	2406.15	2478.15
18	2403.3	2475.3	38	2406.3	2478.3
19	2403.45	2475.45	39	2406.45	2478.45
20	2403.6	2475.6	40	2406.6	2478.6

-END-

Document release information: (ref.: baseTS_2128, 25 Aug. 2001, revision 1.1)

RELEASE NO. :	REVISION NO. :	RELEASE DATE :	SOFTWARE RELEASE NO : T05
R1	0	APR.16,2002	RELEASED TO : KS

1st. release

RELEASE NO. :	REVISION NO. :	RELEASE DATE :	SOFTWARE RELEASE NO : T10
R2	1.0	MAY 6, 2002	RELEASED TO : KS

Change:

- TAD will skip the RAM test, announce 'Unit ready' [page1]
- 7-segment shows the RSSI status. 'In' when RSSI=1, OFF otherwise.[page 1]
- RINGER SWITCH: ON → 7-segment OFF, OFF → 7-segment show '00' [page 1]

end of change