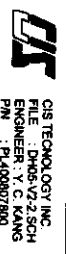
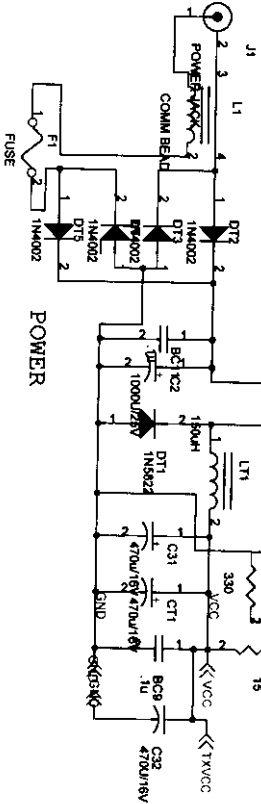
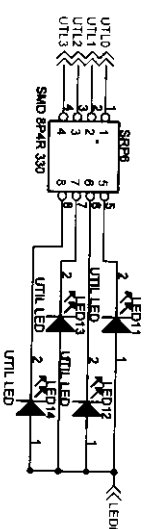
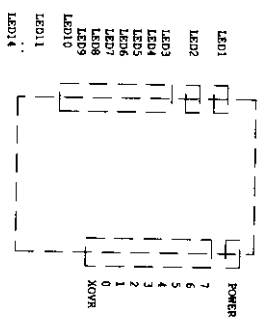
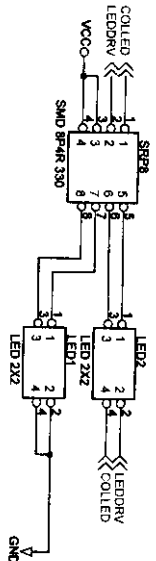
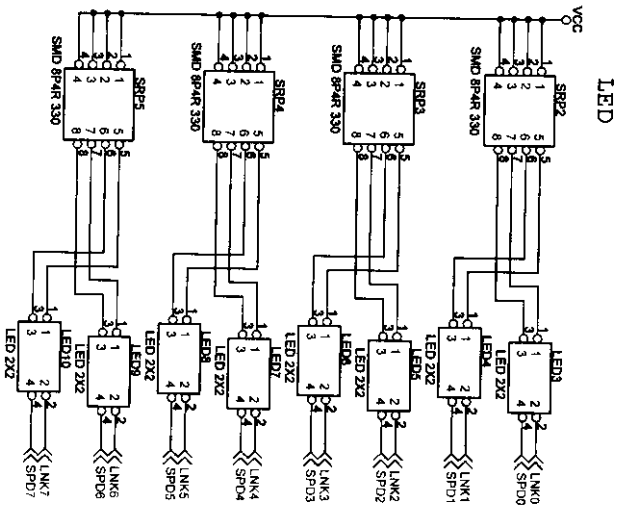
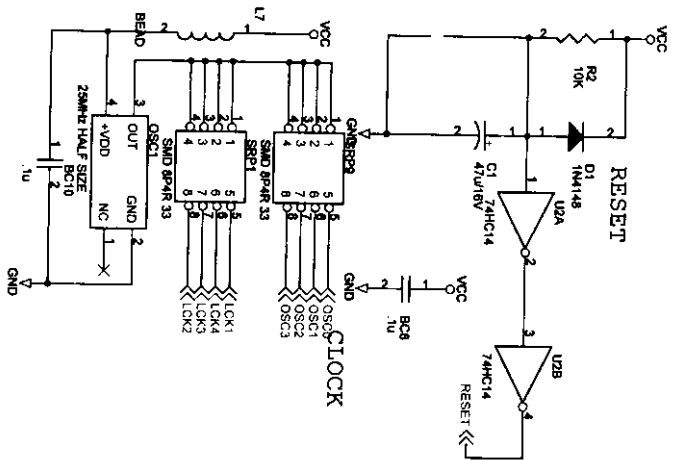


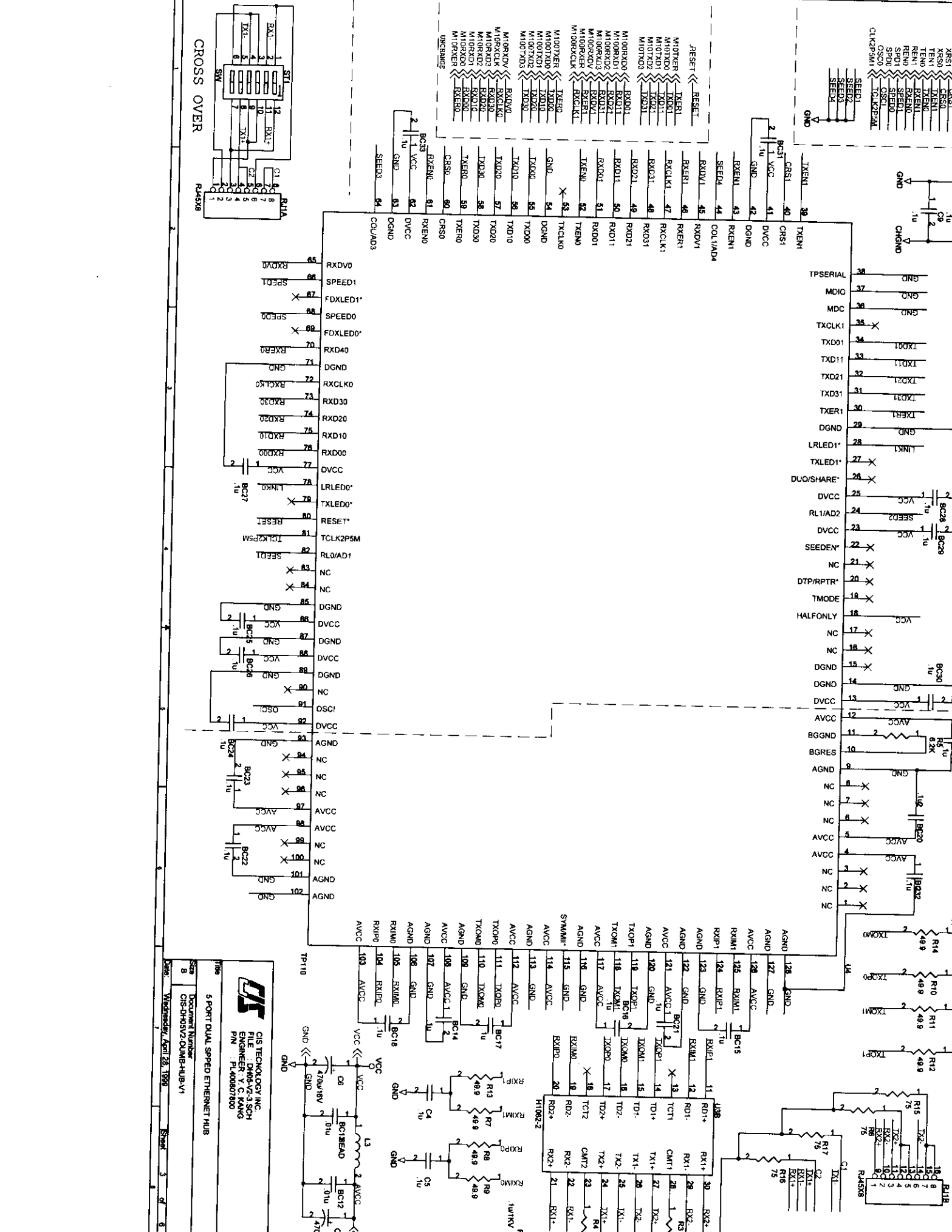
EXHIBIT D

Circuit Diagram

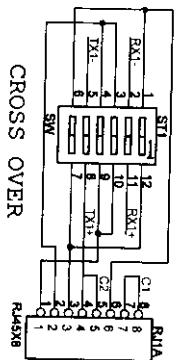


CIS TECHNOLOGY INC.
 5 PORT DUAL SPEED ETHERNET HUB
 ENGINEER: Y. C. KANG
 P/N : PL40007800

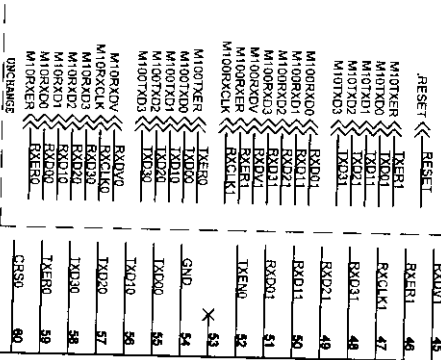
DocuPart Number: CIS-DH002-DUAL-HUB-V1
 Date: Wednesday, April 28, 1999
 Sheet 2 of 8



CROSS OVER



RESET

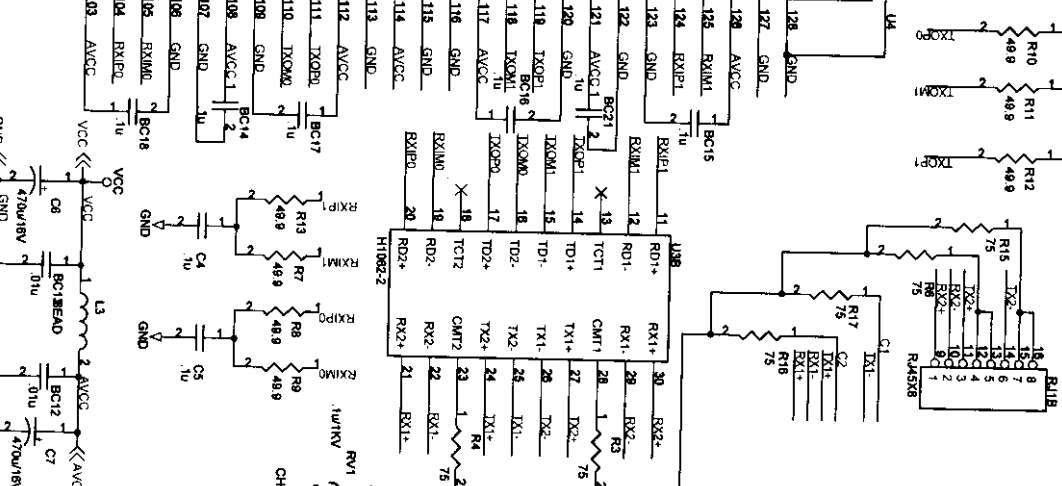


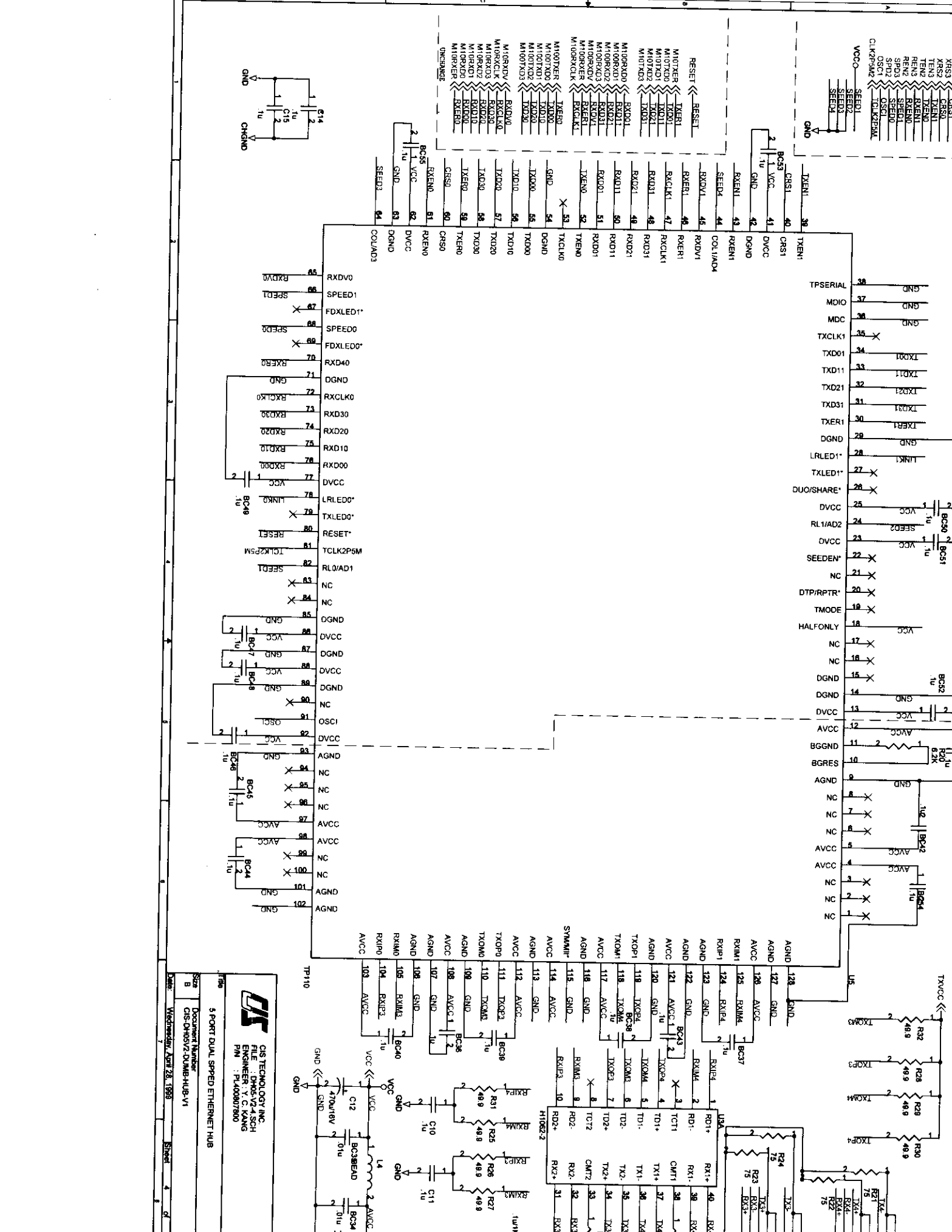
CTS
CTS TECHNOLOGY INC.
 FILE : DM05-V2-3-SCH
 ENGINEER : Y. C. KANG
 P/N : PL400807800

5 PORT DUAL SPEED ETHERNET HUB

Size: B
 Document Number: CTS-DM05V2-3-DUMHUB-V1
 Date: Wednesday, April 23, 1998
 Sheet: 3 of 6
 Rev: 1

TP-110





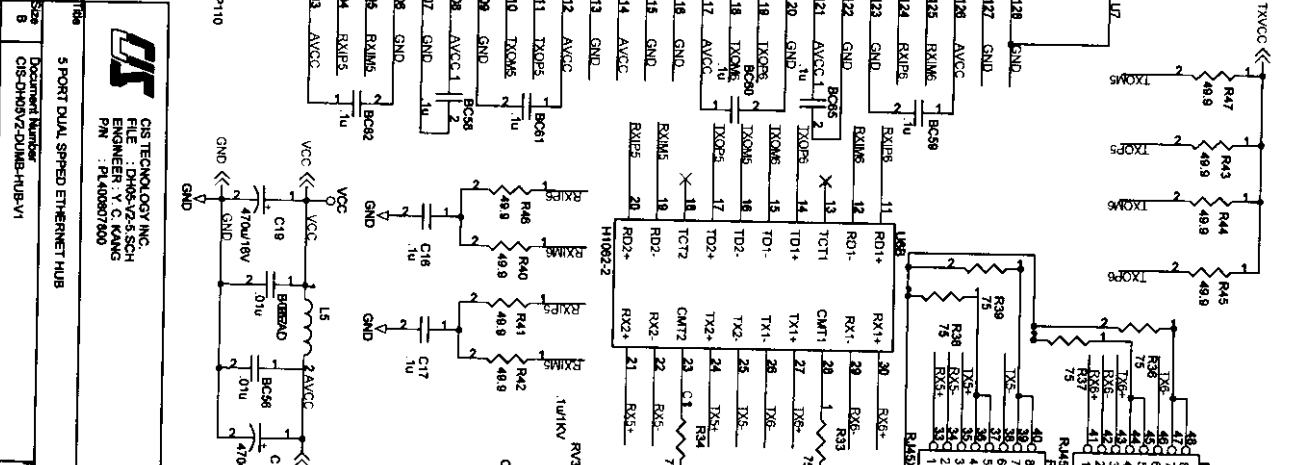
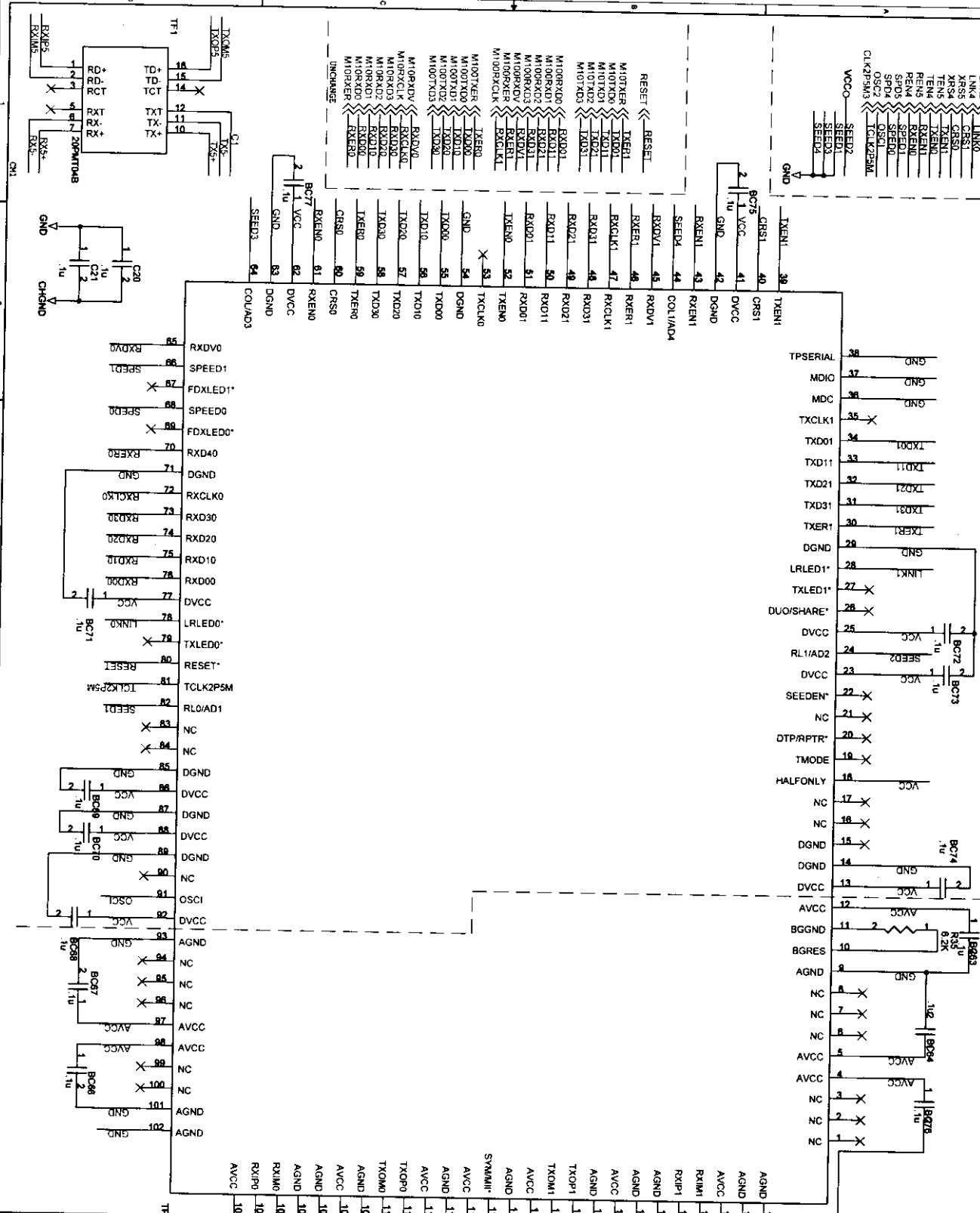
| Pin | Signal | Component |
|-----|------------|-----------|
| 38 | TPSERIAL | GND |
| 37 | MDIO | GND |
| 36 | MDC | GND |
| 35 | TXCLK1 | X |
| 34 | TXD01 | TXD01 |
| 33 | TXD11 | TXD11 |
| 32 | TXD21 | TXD21 |
| 31 | TXD31 | TXD31 |
| 30 | TXER1 | TXER1 |
| 29 | DGND | DGND |
| 28 | LRLED1* | LINK1 |
| 27 | TXLED1* | X |
| 26 | DUO/SHARE* | X |
| 25 | DVCC | VCC |
| 24 | RL1/AD2 | SEED2 |
| 23 | DVCC | VCC |
| 22 | SEEDEN* | X |
| 21 | NC | X |
| 20 | DTP/RPTR* | X |
| 19 | TMODE | X |
| 18 | HALFONLY | VCC |
| 17 | NC | X |
| 16 | NC | X |
| 15 | DGND | DGND |
| 14 | DGND | DGND |
| 13 | DVCC | VCC |
| 12 | AVCC | VCC |
| 11 | BGGND | BGGND |
| 10 | BGRES | BGGND |
| 9 | AGND | AGND |
| 8 | NC | X |
| 7 | NC | X |
| 6 | NC | X |
| 5 | AVCC | VCC |
| 4 | AVCC | VCC |
| 3 | NC | X |
| 2 | NC | X |
| 1 | NC | X |
| 128 | AGND | AGND |
| 127 | AGND | AGND |
| 126 | AGND | AGND |
| 125 | AVCC | VCC |
| 124 | RXP1* | RXP1 |
| 123 | AGND | AGND |
| 122 | AGND | AGND |
| 121 | AVCC | VCC |
| 120 | AGND | AGND |
| 119 | TXOP1 | TXOP1 |
| 118 | TXOM1 | TXOM1 |
| 117 | TXOM1 | TXOM1 |
| 116 | TXOM1 | TXOM1 |
| 115 | AGND | AGND |
| 114 | AVCC | VCC |
| 113 | AGND | AGND |
| 112 | AVCC | VCC |
| 111 | TXOP2 | TXOP2 |
| 110 | TXOM2 | TXOM2 |
| 109 | AGND | AGND |
| 108 | AVCC | VCC |
| 107 | AGND | AGND |
| 106 | AGND | AGND |
| 105 | EXIM2 | EXIM2 |
| 104 | RXP2* | RXP2 |
| 103 | AVCC | VCC |
| 102 | AGND | AGND |
| 101 | AGND | AGND |
| 100 | AGND | AGND |
| 99 | AVCC | VCC |
| 98 | AVCC | VCC |
| 97 | AVCC | VCC |
| 96 | NC | X |
| 95 | NC | X |
| 94 | NC | X |
| 93 | AGND | AGND |
| 92 | DVCC | VCC |
| 91 | OSCI | OSCI |
| 90 | NC | X |
| 89 | DGND | DGND |
| 88 | DVCC | VCC |
| 87 | DGND | DGND |
| 86 | DVCC | VCC |
| 85 | DGND | DGND |
| 84 | NC | X |
| 83 | NC | X |
| 82 | RL0/AD1 | SEED1 |
| 81 | TCLK2P5M | TCLK2P5M |
| 80 | RESET* | RESET |
| 79 | TXLED0* | LINK2 |
| 78 | LRLED0* | VCC |
| 77 | DVCC | VCC |
| 76 | RXD00 | RXD00 |
| 75 | RXD10 | RXD10 |
| 74 | RXD20 | RXD20 |
| 73 | RXD30 | RXD30 |
| 72 | RXCLK0 | RXCLK0 |
| 71 | DGND | DGND |
| 70 | RXD40 | RXD40 |
| 69 | FDXLED0* | X |
| 68 | SPEED0 | SPEED0 |
| 67 | FDXLED1* | X |
| 66 | SPEED1 | SPEED1 |
| 65 | RXDV0 | RXDV0 |
| 64 | COLLAD3 | DGND |
| 63 | DVCC | VCC |
| 62 | DVCC | VCC |
| 61 | RXEN0 | RXEN0 |
| 60 | CRS0 | CRS0 |
| 59 | TXEN0 | TXEN0 |
| 58 | TXD00 | TXD00 |
| 57 | TXD10 | TXD10 |
| 56 | TXD20 | TXD20 |
| 55 | TXD30 | TXD30 |
| 54 | TXD40 | TXD40 |
| 53 | TXCLK0 | TXCLK0 |
| 52 | TXEN0 | TXEN0 |
| 51 | RXD01 | RXD01 |
| 50 | RXD11 | RXD11 |
| 49 | RXD21 | RXD21 |
| 48 | RXD31 | RXD31 |
| 47 | RXD41 | RXD41 |
| 46 | RXCLK1 | RXCLK1 |
| 45 | RXER1 | RXER1 |
| 44 | COLLAD4 | DGND |
| 43 | RXEN1 | RXEN1 |
| 42 | DGND | DGND |
| 41 | DVCC | VCC |
| 40 | CRS1 | CRS1 |
| 39 | TXEN1 | TXEN1 |
| 38 | BCS3 | BCS3 |
| 37 | VCC | VCC |
| 36 | GND | GND |
| 35 | SEED1 | SEED1 |
| 34 | SEED2 | SEED2 |
| 33 | SEED3 | SEED3 |
| 32 | SEED4 | SEED4 |
| 31 | LINK1 | LINK1 |
| 30 | LINK2 | LINK2 |
| 29 | LINK3 | LINK3 |
| 28 | LINK4 | LINK4 |
| 27 | LINK5 | LINK5 |
| 26 | LINK6 | LINK6 |
| 25 | LINK7 | LINK7 |
| 24 | LINK8 | LINK8 |
| 23 | LINK9 | LINK9 |
| 22 | LINK10 | LINK10 |
| 21 | LINK11 | LINK11 |
| 20 | LINK12 | LINK12 |
| 19 | LINK13 | LINK13 |
| 18 | LINK14 | LINK14 |
| 17 | LINK15 | LINK15 |
| 16 | LINK16 | LINK16 |
| 15 | LINK17 | LINK17 |
| 14 | LINK18 | LINK18 |
| 13 | LINK19 | LINK19 |
| 12 | LINK20 | LINK20 |
| 11 | LINK21 | LINK21 |
| 10 | LINK22 | LINK22 |
| 9 | LINK23 | LINK23 |
| 8 | LINK24 | LINK24 |
| 7 | LINK25 | LINK25 |
| 6 | LINK26 | LINK26 |
| 5 | LINK27 | LINK27 |
| 4 | LINK28 | LINK28 |
| 3 | LINK29 | LINK29 |
| 2 | LINK30 | LINK30 |
| 1 | LINK31 | LINK31 |

CIS TECHNOLOGY INC.
 FILE: D:\HW\21\1064\HUB-V1
 ENGINEER: Y. C. KANG
 P/N : PL400807800

3-PORT DUAL SPEED ETHERNET HUB

Document Number: CIS-DH05V2-DUMH-HUB-V1
 Size: B
 Date: Wednesday, April 23, 1998

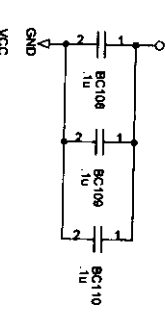
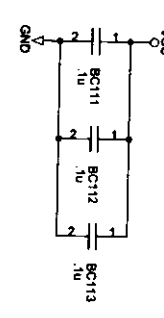
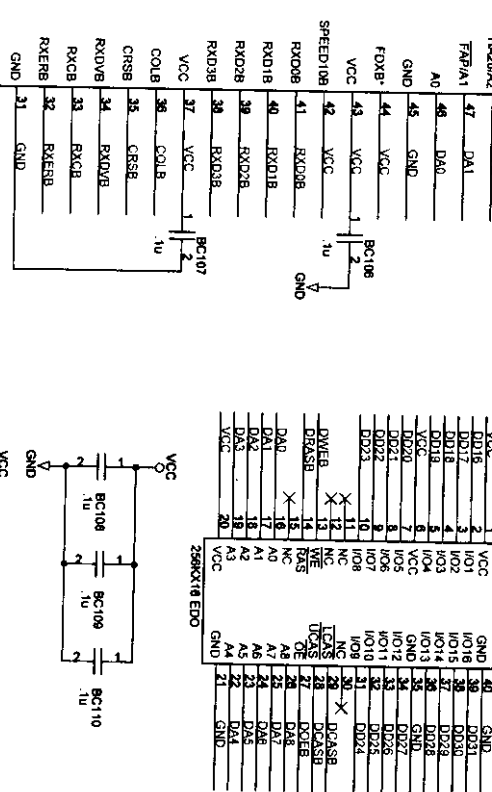
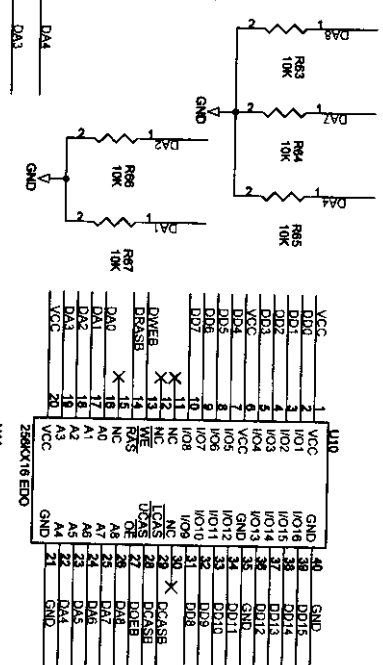
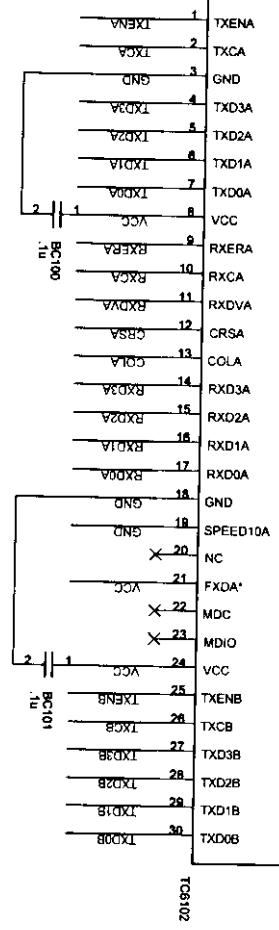
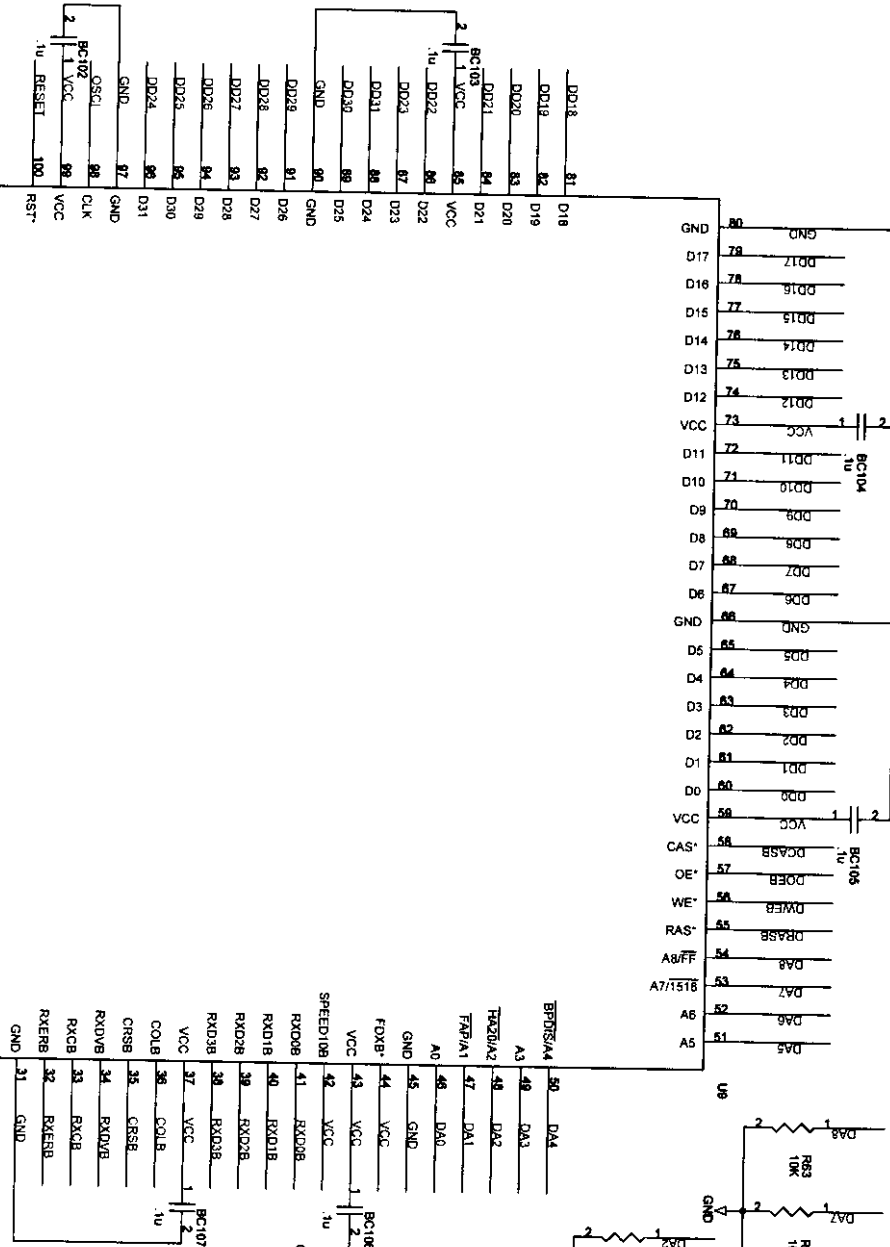
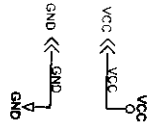
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5 PORT DUAL SPEED ETHERNET HUB
Document Number: CIS-DH05VZ-DLUMB-HUB-V1
Date: Wednesday, April 28, 1999
Sheet: 5 of 8

CIS TECHNOLOGY INC.
FILE: DH05VZ-S-SCH
ENGINEER: V. C. KANG
P/N: P1400007000

LCK3 <<< DSQ1
 RESET
 S100TXEN TXENA
 S100TXD3 TXCA
 S100TXD2 TXGA
 S100TXD1 TXD3A
 S100TXD0 TXD2A
 M100LCA TXD1A
 M100LCA TXD0A
 S100CRS CRSA
 S100COL COLA
 M100TXD3 RXD3A
 M100TXD2 RXD2A
 M100TXD1 RXD1A
 M100TXD0 RXD0A



CTS
 CIS TECHNOLOGY INC.
 FILE : DMS-VZ-6-SCH
 ENGINEER : V. C. KANG
 P/N : P400807800
 Wednesday, April 28, 1999
 5 PORT DUAL SPEED ETHERNET HUB
 Document Number
 CIS-DH0VZ-DUM6-HUB-V1
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