Technical Description

DE900

Version 1.2

5th September, 2002/BJ

Technical Function Description DE900

The most important functions of the main subassemblies of the DE 900 are described in the following. A functional unit consists of the mainboard and the LCD module with a keypad board.

The DE 900 is characterised by a POCSAG protocol receiver which is based on the double superheterodyne principle. This means that the high frequency input signal is converted to the wanted signal via two intermediate frequencies.

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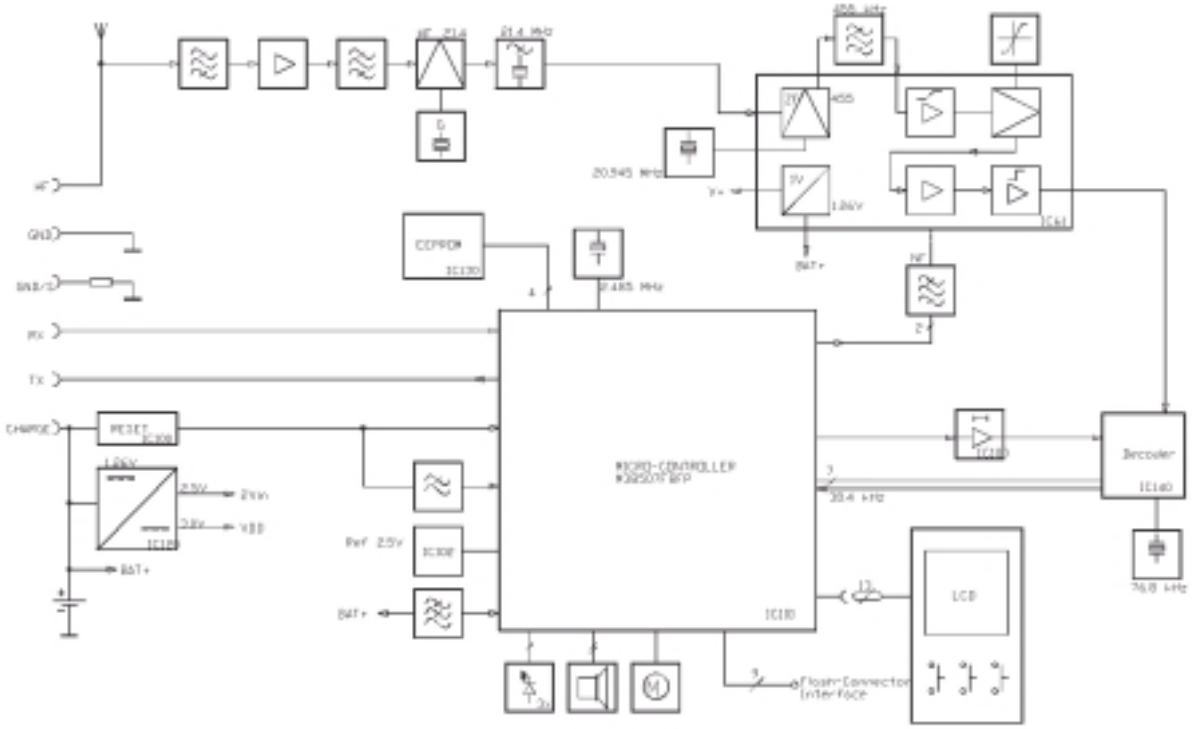
1. Block Diagram

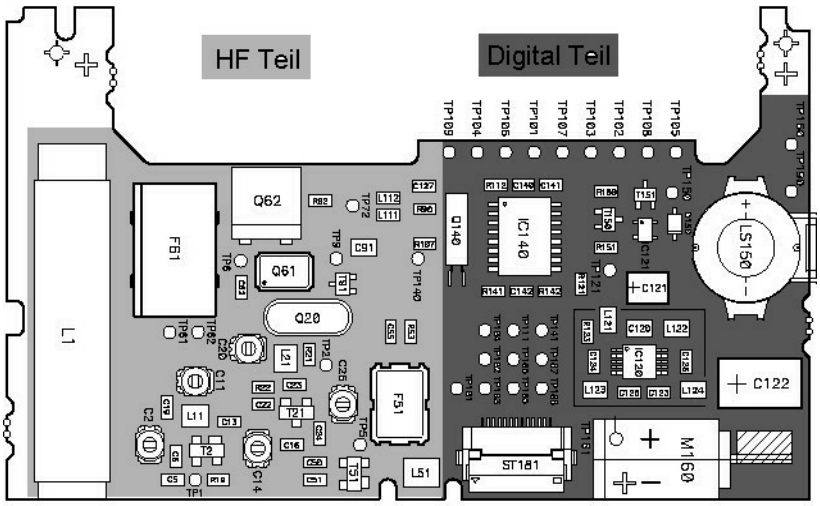


1.1. Message Signal Reception

- The received message signal is transmitted via the antenna to the high-frequency (HF) section
- The LNA (low-noise amplifier) both filters and amplifies the signal there
- The 1st mixer converts the filtered high frequency signal to a 21.4 MHz IF signal
- The 21.4 MHz filter separates the wanted IF from the other combination frequencies
- The 2nd mixer converts the filtered high frequency signal to a 2 MHz IF
- Re-filtering
- The threshold amplifier prepares the IF signal for demodulation
- The demodulator processes the signal using an external resonator
- The now-activated LF filter (Sallen & Key) is baud rate dependent and is switched by the microprocessor
- The comparator generates a clean 0V / 3V signal formatted in the POCSAG protocol
- This signal is then deciphered by the decoder and forwarded to the microprocessor via a serial interface
- In the case of message signal comparison (e.g. the RIC had already received a recently sent message) → communication with EEPROM
- In normal operation, however, an instantaneous alarm is triggered
- → Beep
  → Vibrator
  → Display illumination
  → Message display
- In the terminal step, the message is saved in the EEPROM

2. MAINBOARD

The mainboard is constructed of a 4-layer multilayer circuit board and is fitted with SMD components. To optimise reception, the circuit board is divided in two subsections: the HF section and the digital section.



2.1. Power Supply

The power supply is provided by means of the rechargeable battery (1.26 V nominal) or a conventional battery.

The following power supply voltage range is required by the mainboard.

BAT+	=	1.26 V/DC	for IF section, DC/DC converter, vibrator, beeper, voltage monitoring and regulation
V_{DD}	=	3 V DC	for microprocessor, decoder, EEPROM and LCD module
2Vin	=	2.5 V/DC	for LCD illumination
V+	=	1 V/stab.	for HF transistors

V_{DD} voltages = 3 V, 2Vin and V+ = 1 V are generated by the receiver itself via the DC/DC converter and the IF-IC.
If the rechargeable battery voltage drops below 1.18 V, the battery alarm is triggered via the microprocessor (rhythmic clicking). Counting from this moment on, the device is still operational for approx. 24 hours more. If the voltage drops below 1 V/DC, the microprocessor resets and the device is switched off.

NiMH, NiCad rechargeable batteries or dry cell batteries can be used as power supply sources. Please note that when non-rechargeable batteries are used, the receiver recognises these as such and no recharging can take place.

2.2. Antenna / Amplifier / Filter

The signal is coupled via ferrite antenna L1. C1, C2, C3 and C4 tune the antenna to the proper resonance. The signal is subsequently amplified by transistor level T1/T2, which functions as a cascode switch. The desired frequency band is selected by means of a coupled filter consisting of both parallel resonant circuits L11/C11/C12 and L14/C14/C15.

2.3. Quartz Crystal Oscillator

The major component here is a Colpitts oscillator. The output circuit with components C20/C30/L22 is needed for selection of the oscillator signal. The collector circuit filters out the doubled quartz crystal frequency (second harmonic) for the 2m band. The oscillator signal is transferred to the mixer via coupling capacitor C24.

The oscillator frequency lies in the 4m band. The frequency during 2m UB and 2m MB operation is 21.4 MHz higher than the receiving signal. In the 2m upper band, the oscillator frequency is 21.4 MHz lower than the receiving signal.

2.4. First Mixer Level / Filter

Transistor T51 mixes the amplified antenna signal with the local oscillator signal and sends it to the first IF 21.4 MHz. Oscillator circuit L51/C52 represents the load resistance at this stage.

The IF signal is filtered through the next quartz crystal filter F51. This filter selection serves the purpose of suppressing adjacent channel interference and image frequency interference. R51, L51 and C52 as well as R53, L52, C55 and the input capacitance of IC 61 form the necessary matching impedance for the quartz crystal filter.

The IF signal is then transferred to IC61 via coupling capacitor C56.

2.5. IF-IC

In the second mixer level, the wanted signal 21.4 MHz is converted to 455 kHz. Quartz crystal Q61 delivers the oscillator frequency 20.945 MHz. The conversion to 455 kHz is implemented in the IF module TA31145 (IC 61) integrated mixer.

The signal is subsequently filtered and amplified. The amplifiers are integrated in the IF-IC, the external ceramic filter F61 filters and also determines the channel separation (25 kHz / 12.5 kHz) for the receiver.

In the last step, quadrature demodulation converts the signal to base band (LF). The external ceramic discriminator is responsible for the necessary phase shifting of the 455 kHz signal. The active section of the quadrature demodulator is integrated in the IF-IC.

The signal mixed in the base band is sent through a third order low-pass filter circuit composed of R71, R72, R73, C71, C72, C73 and the amplifier integrated in IF-IC. Capacitors C74 and C75 further reduce the cut-off frequency for both baud rates 1200 and 512 bits/second. BAUD_512 and BAUD_1200 conductors are high resistance for the 2400 baud rate. The corresponding 512 or 1200 conductor is connected to GND.
The band-limited LF signal is then passed to the integrated FSK comparator. In order to optimise comparator functionality, the Quick-Charge input at the DC level sets symmetrical input signals (preamble and synch) to a mean signal value.

At the open collector output FSKOUT uses resistor R91 to adjust the signal to the 3 volt level, after which the signal is forwarded to the decoder for further processing (RDI_NPC).

To reduce power consumption, the IF module is switched off by the BATT SAVE input. If the IC61 is switched off with a 0-signal, the 1 volt power supply for the HF level, which is regulated by T91, is also switched off.

2.6. Decoder

The decoder SM8212B works with baud rates 512, 1200 and 2400. It can decode 8 RICs in as many frames as desired. The RICs to be decoded are loaded in the decoder RAM at start-up.
The microprocessor communicates with the decoder via signal conductors /INT_PCD, DOUT_NPC, DIN_NPC and CLK_NPC_INV. This circuitry also permits decoded messages to be relayed to the microprocessor. To optimise communication, the conductor CLK_NPC has a built-in time delay formed by R106 and C105. Moreover, the clock must also be inverted (IC100).
The quartz crystal Q141 is additionally used for the clock because the requirements for accuracy placed on it are very high. C143 can correct frequency to some degree.
Output CLK0 controls the 38.400 kHz signal which is used as a secondary time basis by the microprocessor.
As soon as the decoder detects a synchword, OUR_NPC is set "high" for 1 second.
The decoder uses the BS1 conductor (RXE_NPC) to switch the IF-IC and thereby turn the HF on and off.
The BS2 signal is utilised as a control signal for the comparator of the IF-IC, which makes dynamic adjustment of the comparator level possible. If the case of a symmetrical input signal (preamble or synch signal), the level is set to the mean value of the comparator.
A FFSK version of the DE900 is planned for the future. This additional level would switch on via the BS3 conductor.

2.7. µC Microprocessor / µC Clock / Reference Voltage

The microprocessor (IC 101) controls the illumination, vibrator and display as well as message processing and communication. The M38507F8FP version is equipped with a flash-programmable software, whereas the M385078FP version is mask programmed.

Besides the supply voltage, the microprocessor requires two additional tact frequencies. Q101 delivers 2.4576 MHz as the actual frequency, and input XCin receives the 38.400 kHz signal generated by the decoder. During low activity periods, the microprocessor works with the 38.400 kHz clock speed (low speed) and briefly switches every 0.5 seconds to the faster clock speed (high speed) for interrupt processing.

The reference voltage diode (IC 102) delivers a 2.5 V power supply, which is used by the microprocessor to monitor the operating voltage. This occurs independently of the Ah counter. To reduce power consumption, reference voltage is clocked via VREF_ON pin 41 of the microprocessor and therefore is only available for limited times.

For the LCD display, the microprocessor uses a serial interface (RS_LCD, CSB_LCD, SI_LCD, CLK_LCD, RSTN_LCD) to communicate with the display driver located on the glass. However, the microprocessor cannot display individual pixels.

All other signals are described in the sections dealing with the corresponding subassemblies.

2.8. Keypad Board / LCD

The keypad board is connected via plug ST181. In addition to the communication conductors (see chapter P Microprocessor), there are three key conductors (BUT_1, BUT_2, BUT_3), the key interrupt conductor (BUT_INT) and the power supply.
Expansion possibilities for future EX devices (explosion protected) are provided via the coils L180 to L183 and R180 to R184. At present however, these are not used and are bridged on the circuit board with a wire jumper.

2.9. EEPROM

The device uses the 64KBit EEPROM (IC 130) as a storage unit for the programmable options, calling addresses, as well as for the storage of received calls. As the DE900 is not equipped with RAM, even the message comparison proceeds via the EEPROM.
The EEPROM is configured such that the programmable options and the calling addresses are saved in a protected area.

2.10. Beeper

The beeper LS150 can be controlled with conductor CLK_LS and various frequencies. With the conductor AMPL_LS, loudspeaker volume can be controlled via T150 in 2 steps. A 0-signal sent to AMPL_LS means higher volume.
The beeper itself is optimised for a frequency of 2.7 kHz.

2.11. Optical Signalling

Optical Signalling takes place in two ways: via the 3 LEDs which are responsible for the background illumination of the LCD, and via the direct display of the message on

the LCD. The 3 LEDs are operated with power supply 2xVIN. The transistor T190 is utilised to switch the supply voltage on and off.

2.12. Vibrator

Besides the optical and acoustic signalling methods, the vibrator M160 can also announce an incoming call. The microprocessor generates the vibration pattern and dispatches it through the conductor /VIBRATOR, with which transistor T160 switches the motor on/off.

2.13. DC/DC Converter, Reset

DC/DC converter TPS60301 (IC 120) is employed to generate voltage V_{DD} = 3 V and voltage 2X_VIN from the operating voltage BAT+. To accomplish this, a new IC that functions purely capacitively was set in place. The coils serve the sole purpose of interference reduction. In addition to the IC, the external components C123, C124, C125 and C126 are required. The IC functions with a 2-step loading pump. The first step involves doubling the input voltage. Power supply 2X_VIN at Out1 is available for this purpose. The second loading pump, which already possesses the doubled input voltage, functions in two modes, x1.5 or x2, depending on the voltage output. Directly attached to the second loading pump is a serial regulator that delivers the stabilised 3 volt supply to Out2.

L121, L122, L123 and L124 serve to reduce interference from the DC converter.

If the voltage BAT+ sinks below 1 V, the detector (IC121) triggers a signal causing the microprocessor to reset. The level at /LOWBAT is now 0.

2.14. ESD Protection

The device has an array of various features built in to protect against electrostatic discharge. The first ESD measure only functions when connected to the battery recharging unit. One contact pin of the recharging unit is longer than the others, which results in the ESD conductor of connection plug ST111 making electrical contact before the remaining conductors. In this way, static electricity is discharged through resistor R111.

ESD protection measures have also been taken at the communication conductors. FS2 and FS3 are voltage distributing PADs and D111 is a Schottky diode (twin diodes) affording protection against excessive voltages.

2.15. Switching-On / Off Sequence

Starting sequence of the DE900:

- Insertion of the battery → voltage BAT+ OK
- 3V and doubled battery voltage is generated by the DC converter

- The reset release from IC121 is time-delayed (by R102 and C103) and sent to the microprocessor
- The microprocessor starts up
- Battery measurement - no-load (>1.16V) → battery symbol
- EEPROM is tested (checksum) and read out
- Battery measurement - with load (>1.25V) → beeper/vibrator as load, batt.- / rechargeable battery recognition
- Programming of decoder → decoder test
- Switch-on beep
- Low-speed mode

Switching OFF Sequence:
- Battery is removed
- IC121 delivers the reset impulse without time delay to PIN7 of the microprocessor
- The microprocessor writes important data in the EEPROM, the supply voltage is maintained by C122

Battery Depletion:
- Battery voltage sinks gradually. The battery alarm is triggered at 1.18V.
- Battery voltage < 1V → IC121 delivers reset impulse to PIN 7 of the microprocessor
- The microprocessor writes important data in the EEPROM
- Battery voltage < approx. 0.6V → DC converter switches off

3. LCD, KEYPAD MODULE:

The keypad module consists of 3 components:

- Optical fibre which also acts simultaneously as a holder for the LCD and the keypad board
- The keypad board is equipped with a connector that is plugged into connection plug ST181 at the mainboard.
- LCD with chip mounted on the glass

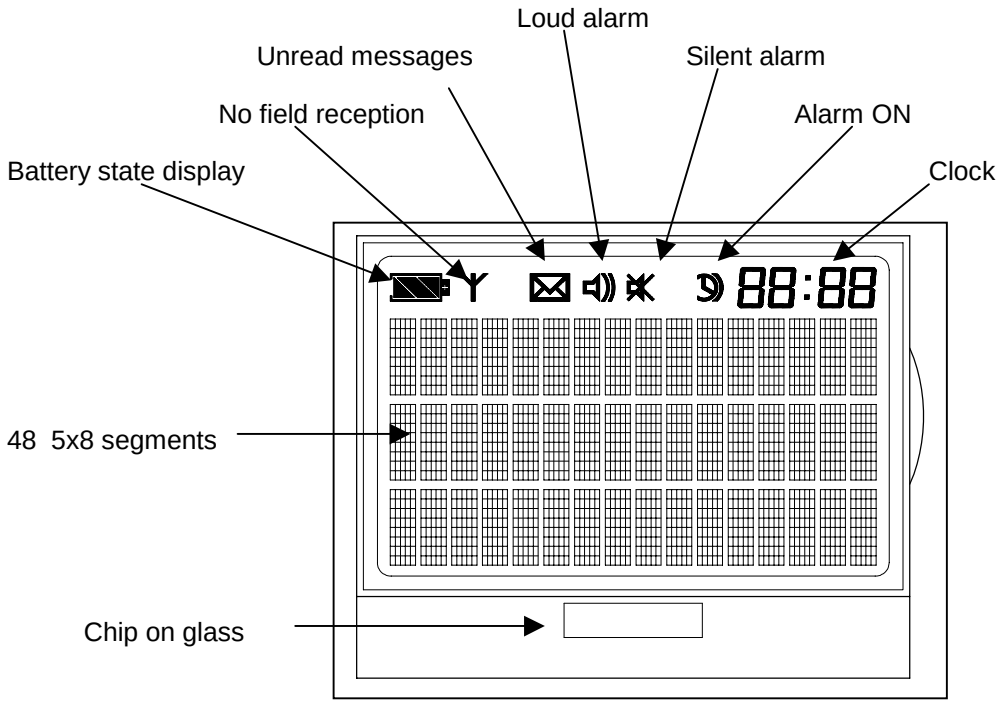
3.1. Keypad Board

The gold pads for buttons S1, S2 and S3/S4/S5 are arranged on the keypad board. If the 3 buttons are pressed, an interrupt will be triggered via conductor BUT_INT. The resistor diode network composed of R303...R306 and D300,D301 and D302 is responsible for generating this interrupt.

3.2. LCD Liquid Crystal Display

The LCD display with the ST7093A driver chip is mounted directly on the glass and is controlled by the microprocessor via 5 control wires. The 7.2 volt power supply necessary for the high-contrast display is generated by the chip itself using capacitors C300, C301 and C302. This voltage is present at Vout. Contrast is roughly adjusted by voltage dividers R320 and R301 and can be fine-adjusted with the software.

Explanation of the LCD sections:



3. CONNECTING THE RECEIVER WITH PERIPHERAL DEVICES

Peripheral devices such as **battery rechargers LGxx 300/429** and **(A)LG500** and the **programming attachment PGM 300/429** are connected to the receiver via the 6-pole contact in the housing. The signals are transmitted by means of the double spring contacts mounted on the 6 gold pads of the circuit board.

The contact strips contain the following signals:

Identification	**Function**
HF	HF signal input
GND	Common earth/ground
ESD	Static electricity earth/ground (pre-contact)
RX	RX signal for programming attachment, charging control for battery recharger
TX	TX signal for programming attachment, call control for battery recharger
BAT+	Charging of rechargeable battery, external operating voltage

A positive interrupt at the RX signals the pager that the recharger is connected

The following conditions are valid for a battery recharger:

RX = low => No charging current
RX = high => Charging current ON
TX = low => No unread call
TX = high => Unread call present

A codeword at the RX signals the pager that the programming attachment is connected

RX/TX => RS 232 communication at the 0/3V level