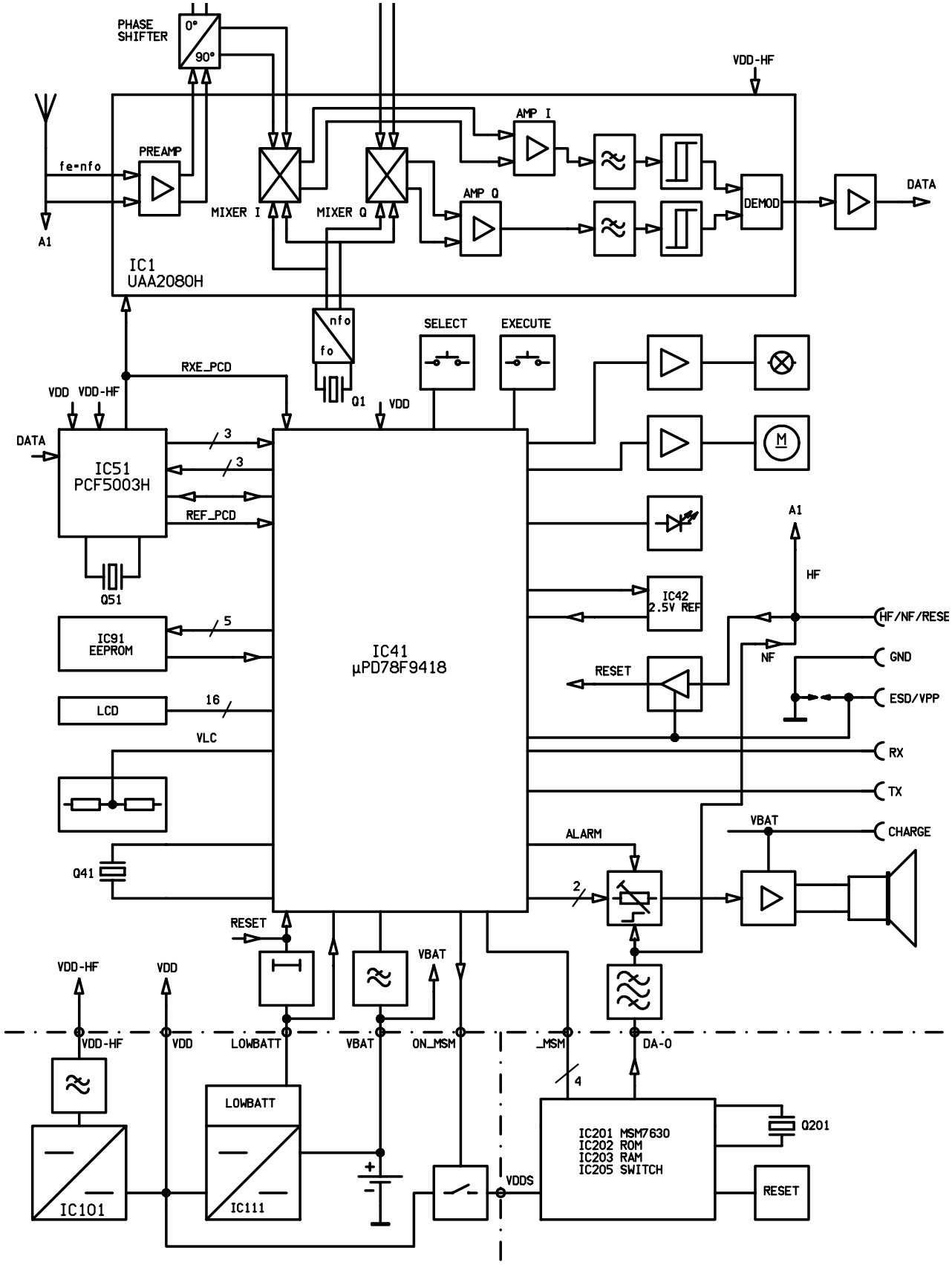
Technical Functional Description DV500

1. Schematic Block Diagram



2. HF - Part

2.1. General
The HF – receiver stage is constructed with the direct conversion chip UAA2080 (IC1). This chip supplies the demodulated DFSK-POCSAG - signal at the output.

2.2. Input Circuits
The aerial is tuned with C3. The aerial signal reaches the RF pre-amplifier through the symmetrical inputs VI1RF und VI2RF. The output circuit of this amplifier is equalised to the receiver frequency with L2, L3 and C6. The amplified input signal reaches the two mixer inputs through the quadrature network C10, C11, L4 and L5.

2.3. Oscillator
The oscillator frequency is defined by the quartz Q1 and C16. The output circuit of the oscillator with C15 and L8 is dimensioned to the 2- or 3-times quartz frequency (multiplier 1) in broad-band. This oscillator signal internally reaches a multiplier stage, which is tuned to the 1- or 3-times of its frequency (multiplier 2) with C12, L6 and L7. Therefore the following broad-band multiplications of the quartz frequency result:

Band	Multiplier 1 Factor m_1	Multiplier 2 Factor m_2	Multiplication Factor $n = m_1 * m_2$
VHF - 4mXX	2	1	2
VHF - 2mXX	3	1	3
UHF - G/H	2	3	6

The symmetrical oscillator signal also reaches the mixers.

2.4. Mixers
Present on the chip are two identical mixers, which are supplied with the two signals (I- and Q-Signal) and the oscillator signal. The IF – signal obtained after the mixing is still symmetrical and the middle of the spectrum is situated at 0 Hertz.

2.5. IF, Demodulation
The IF – signal reaches the limiter amplifiers through the internal IF – amplifiers and -filters. At the output of the quadrature demodulator, the DFSK-POCSAG - signal is available for the decoding.

3. Digital Part

3.1. Decoder

The serial data stream (RDI_PCD) reaches the decoder (IC51) through the uncoupling resistors R31and R33. The HF – amplifier is switched on and off with the line RXE_PCD.
The decoder is controlled from the µC, wherein the RIC to be decoded are stored in the EEPROM of the decoder. Also defined at 512, 1200 or 2400 Baud by the programming of the decoder is the transmission rate.
The decoder continually analyses the data stream received and in the case of a coinciding RIC wakes-up the µC by means of an interrupt on the line INT_PCD.

3.2. µC and Peripherals

The two clock frequencies are fed-in to the µC (IC41) by Q41 (2.458 MHz) and, derived from Q51, from the decoder through REF_PCD (32.768 kHz).
The decoded data through SDA_PCD and SCL_PCD reaches the µC. On the basis of the programmed functions, in the case of a correctly identified RIC the corresponding output ports are actuated with the data belonging to it for the alarm notification.
Serving as user interface are the keys SELECT and EXECUTE (S1 and S2), the LCD - display (LCD1), the red signalling - LED (D71), the vibrator switched through T72 (M71) and the LF- stage with loudspeaker controlled by the µC (also refer to chapter 4).
The programmable options of the receiver are stored in the EEPROM (IC91). Foreseen as the interface to the charging – and programming device are the two lines RX and TX. Except with respect to the voltage level, the protocol conforms to RS232.
Through the lines TXD_MSM and RXD_MSM, the µC controls the voice print, for more details, please refer to chapter 5 (Voice Part).
With the programming voltage applied, the buffer (IC43) makes possible the controlling of the RESET – line through the interface and through RX/TX enables the programming of the flash – memory of the µC.
The voltage divider (R41, R42 und R43) together with the capacitors (C41 und C42) serves to generate the LCD - voltages.
The retarding (delay) network (R78, R48, C48 and D42) out of the LOWBATT signal from the IC111 generates the RESET Signal for the µC.

4. LF - Part

4.1. Beep

The alarm signal generated by the µC is conducted to the final amplifier through R61,T61,R82, R83 and C82.

4.2. LF - Amplifier

The LF - amplifier NJM2076M (IC81) is operated with VBAT and for the purpose of saving electric power can be switched in through transistor T81. The loudspeaker is

located in a full bridge circuit, formed by 2 NPN – transistors in the IC81 itself and the two external PNP - transistors T82 und T83.

4.3. LF - Filter
The LF – signal from the voice print through DA-0 reaches the LF - filter formed with the transistors T62 and T63. The limit frequency of this filter is defined at 6.4 kHz.

4.4. Volume
The volume of the LF – signal can be adjusted in 4 levels with the lines VOL1 and VOL2. The resistors R81, R82, R83 and R84 form a switched voltage divider.

5. Voice Part

5.1. General
Located on the voice print is the 3-fold chip-set, which is responsible for the generation of the voice.

5.2 MSM7630
This is the actual voice processor with a computing performance capacity of 20 VAX-IPS (33 MHz 486 computer). The MSM7630 is clocked at 33 MHz with the resonator Q201. IC204 together with C209 and R206 forms the reset circuit for the IC 201.

5.3 ROM MR27V3202E
Required for the storing of all phonemes for the German language and for the storing of the program for the voice synthesizing is a ROM with 4Mbyte. IC205, R208, D201 and R209 serve for the reduction of the standby - current.

5.4 RAM MSM51V18165D
The 1 MByte RAM serves as operating memory for the voice processor.

5.5 Interface to the Voice Print
The voice processor is controlled through the lines RXD_MSM and TXD_MSM. The Baud rate is adjusted to 19’200 bps with the resistors R202...R205.
With the line STBY_MSM, the 3 chips can be set to the standby - mode.
UPORT_MSM logically is „0“, as long as an LF – signal is output at DA01.

6. Power Supply

6.1. General
The power supply to the device is effected either with a rechargeable battery or with a normal battery. The device is fully operative within a voltage range of VBAT = 1.10...1.55 Volt.
The battery voltage is measured by the µC through the filtering R44 and C44. Serving as basis for this measurement is the 2.5 Volt reference IC42.

6.2. DC/DC - Converter

The DC/DC – converter generates a controlled voltage of VDD = 3 Volt (IC 111) from the battery voltage. The MAX1676 is a step-up converter with an integrated switching transistor and also integrated active rectification. The Schottky diode D111 is there for optimal stimulation of oscillations in the case of low battery voltages.
The DC/DC – converter charges the energy stored in the coil L111 to the smoothing capacitance C112. This process is repeated until the internal comparator detects the output voltage as being sufficiently high and switches off the charging process. The output voltage is adjusted through the voltage divider R105, R116 and R118.
If the input voltage drops below a value of – typically - 1 Volt, or if VDD collapses, the converter sets the LOWBATT – signal, which controls the RESET – line of the μC. The reset – threshold is set by the voltage divider R103, R114 and R117.

6.3. HF – Power Supply

The power supply VDD-HF for the direct conversion chip is controlled at 2.3 Volt by means of IC101 and additionally filtered by the low-pass R109, C101 and C102.

6.4. Power Supply Voice Print

With the switching transistor T120, the power supply VDDS (VDDSwitch), on which the voice processor, RAM and ROM are operated, can be switched. VDDS is applied when the receiver is switched on; Thereafter follows a booting of the voice processor, which lasts for approximately 10 seconds; during operation, VDDS is always on.