SWISSPHONE

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Technical Description

DE516C

Version 1.1

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List of Contents

1 Function Description

1.1 General

The data for the pager are transferred in POCSAG code format. These are then frequency modulated transmitted (DFSK). The direct conversion receiver of the DE516C mixes the received signal in only one step from the receiving frequency to the LF range. The data are then directly given out as a bitstream by means of the integral digital demodulator.
This decoder developed by Swissphone analyses this data stream and activates the microcontroller as soon as a message arrives.
The microcontroller operates the display and responds to signals from button presses. It runs a clock and manages the RAM.
The basic functions of the operating system are stored in the internal ROM of the controller; the main part is, however, stored in battery backed up RAM. The device-specific settings are stored in EEPROM and are copied into the battery backed up RAM after the device has been switched on.

The device has a socket strip with connections for external aerial, a charger and a serial interface. (see charge and programming adapter for the DE516)

The battery compartment takes one AA battery (LR6, AM3). The pager accepts alkaline, nickel-metal hydride and nickel-cadmium cells.

2 Digitalprint

2.1 Digital Section

2.1.1 Block Diagram

The design of the DE 516C is explained with the help of two block diagrams. One diagram for the digital section and one for the receiver section.

The digital section consists of the following blocks:

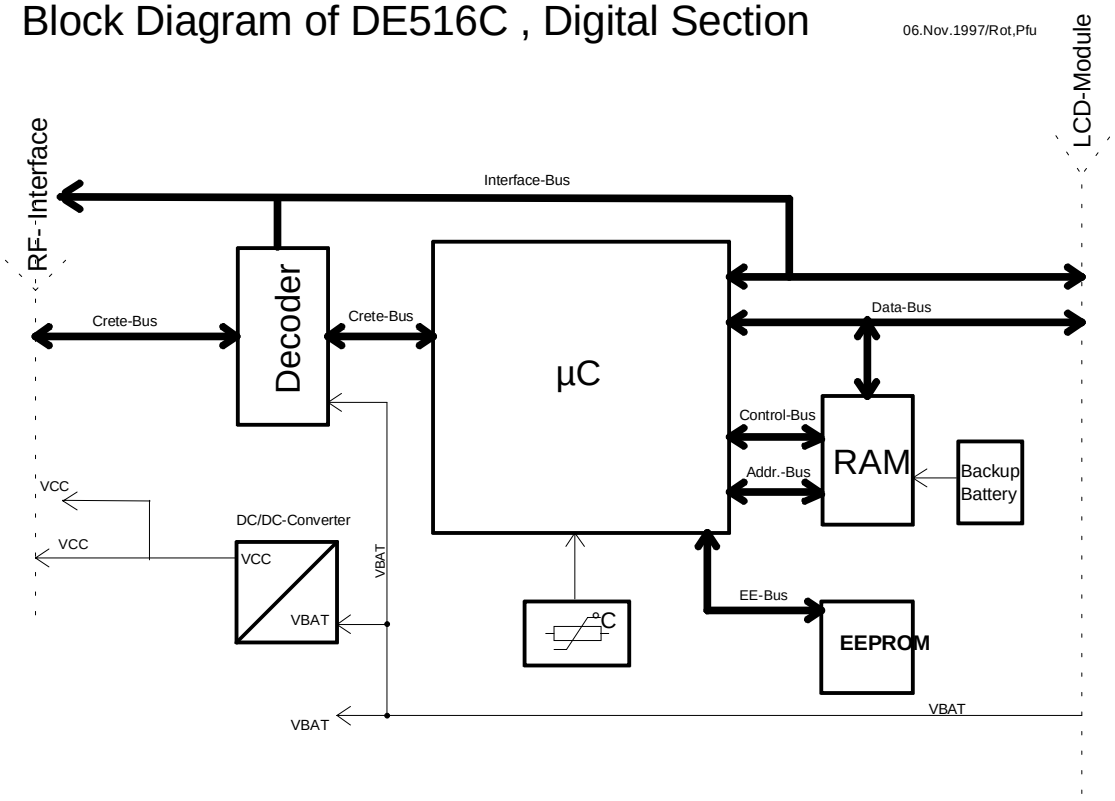
a) POCSAG decoder
b) Microcontroller (µC)
c) Static RAM
d) EEPROM
e) Real time clock
f) DC/DC converter (power management)
g) Battery backup

The following buses connect these blocks:

Analogue - digital: a) Crete (decoder) bus

Digital - digital:
c) Crete (decoder) bus
d) I^2C bus
e) Control bus
f) Address bus
g) Data bus

Digital - display:
h) Interface bus
i) Data bus



2.1.2 Miscellaneous buses

The connections between the individual blocks are described in this section.

1. Crete (decoder) bus
2. I^2C bus
3. Interface bus
4. Control bus
5. Address bus
6. Data bus

2.1.2.1 Crete (decoder) bus

The Crete(decoder) bus connects the digital section (decoder) with the receiver section via the plug connector V240. The Crete(decoder) bus also connects the decoder with the µC and contains the following connections:

a)	EC		Analogue section - decoder interface
b)	RFDIN		Analogue section - decoder interface
c)	\CSCRETE		µC - decoder interface
d)	SIN_UP	(DIN)	µC - decoder interface
e)	SCLK		µC - decoder interface
f)	SOUT_UP	(DOUT)	µC - decoder interface
g)	INT_CRETE	(UPIR)	µC - decoder interface
h)	RST_CRETE	(EXTC)	µC - decoder interface
i)	TX	(INT3)	µC - decoder interface – analogue section

k)	VREG1	(D/A1OUT)	Analogue section - decoder interface
l)	AIFIN		Analogue section - decoder interface
m)	SCL		µC – EEPROM, real time clock (I2C clock)
n)	SDA		µC – EEPROM, real time clock (I2C data)
o)	PLLEN		µC - analogue section
p)	CSIRDA		µC - analogue section
q)	RX		µC - analogue section
r)	Int_PCD		µC - analogue section

a) EC
The economiser is an open drain output. The signal must be inverted by T240 before it can be received by the HF digital section interface V240 pin 5.
For an HF section with a 'single super', the signal is not inverted, i.e. R248 is fitted instead of the transistor circuit.

b) RFDIN
The data signal of the receiver part V240 pin 3 is connected to the comparator input CMP2IN. The comparator output DCDCCLK is directly connected to the input DIFIN, i.e. the comparator is a level shifter.

c) \CSCRETE
ChipSelect of the serial interface (SIN_UP, SOUT_UP; SCLK), active low.

d) SIN_UP
Data input, data direction: µController ⇒ decoder

e) SCLK
Bi-directional clock. The µC is normally the master except when the decoder has stored 500 characters. The decoder then becomes the master and controls the SCLK.

f) SOUT_UP
Data output, data direction: Decoder ⇒ µController

g) INT_CRETE
The decoder informs the µC that an event has occurred. After that, the µC starts to read out the status register of the decoder (e.g. when more than 400 characters are stored in the decoder RAM).

h) RST_CRETE
The µC is capable of triggering a reset in the decoder. High level is Vbat. For this, the line to the µC is connected to port 7.3 of the IC100 (open drain). The pull-up resistor R127 is connected to EXTC (Vbat).
Resistor R127 and capacitor C123 together with the internal capacitor generate the necessary delay.

i) TX
The resistor R232 keeps the TX line at logical zero. A logical high at TX triggers an interrupt in the decoder, should the pager be in the programmer. The decoder feeds the new information via INT_CRETE to the µC. Capacitor C232 prevents ESD problems (see also Section: 3.2.1 ESD Protection

k),l),o),p),q) Not used in the DE516 C.

m)n) see I2C bus

2.1.2.2 I2C bus

The serial standard I2C bus from Philips connects the µC to the EEPROM and to the real time clock.

a) SCL µC – EEPROM, real time clock (I2C clock)
b) SDA µC – EEPROM, real time clock (I2C data)

a) SCL
I2C bus clock - line
R143 serves as pull-up as all outputs are open drain.

c) SDA
Serial data line
R144 serves as pull-up as all outputs are open drain.

2.1.2.3 Interface bus

The interface bus is the connection between the µC and the display module (driver and display). It also includes the control line for the buzzer and the backlighting. It contains the following lines:

a) COM
b) SEG0
c) \WRLCD
d) \RDLCD
e) RSLCD
f) LIGHT_LCD
g) LSCLK
h) LSAMPL
i) SDA
j) SCL

a,b) COM, SEG0
Circuit description, see also Section 2.2.4 Static Symbol.
f_{SS} = 50kHz/512 = 97.7Hz
Amplitude = 0...3V
Sampling ratio = 1 : 1

c,d) \WRLCD, \RDLCD
Read and write lines for the LCD driver

e) RSLCD
Read selector for the LCD driver

f) LIGHT_LCD
Line for control of the backlighting

g,h) LSAMPL, LSCLK
Lines for control of the buzzer. The volume of the alarm is set using the analogue output LSAMPL and the frequency by means of LSCLK.

i),j) see I2C bus

2.1.2.4 Control bus

a) \WR
b) \RD
c) \RST_UP
d) \RAMCS
e) \CSROM
f) V_RAM

a) \WR
Writing for the SRAM
Resistor R150 prevents writing to RAM during the start up and switches off the stage.

b) \RD
Reading for the SRAM

c) \RST_UP
The reset IC 170 monitors the supply voltage V_{dd}. The entire system is reset if the voltage drops. When this happens, the write access to the RAM is blocked and the µC reset.

d) \RAMCS
The read and write access to RAM are formed by the two NAND gates IC152 and IC153. The control line \RST_UP assumes an additional protection function so that no access can be made during the reset mode.

e) \CSROM
The \CSROM line controls the access to the data ROM – which may or may not be fitted.

f) VRAM
see Section 2.1.8.2 Backup battery.

2.1.2.5 Address bus

a) A0-A15
b) A16
c) A17

a) A0-A15
Address line to SRAM and ROM

b) A16
Additional address line for the 1Mbit SRAM

c) A17
Additional address line for a possible 2Mbit data ROM

2.1.2.6 Data bus

a) D0-D7

a) D0-D7
Data lines between µController, RAM, ROM and LCD driver.

2.1.3 Decoder

Connections that are not used are not mentioned here. This section describes the signals that have not already been described in one of the above buses.

They are the following:

a)	VBAT	i)	CMP1IN	r)	TEST0
b)	VCC	k)	CMP2IN	s)	DCDCCLK
c)	DGND	l)	EXTC		
d)	AGND	m)	AIFIN		
e)	SUBGND	n)	INT0		
f)	VREF	o)	INT1		
g)	XTALIN	p)	INT2		
h)	XTALOUT	q)	INT4		

2.1.3.1 Description of the ports of the decoder SW95 (Crete)

a) VBAT
Battery supply voltage: $1V \leq VBAT2 \leq 5.5V$, $VBAT2 \leq VCC$
The output EXTC is connected internally with Vbat2.

b) VCC
Supply voltage: $2.7V \leq VDD \leq 5.5V$
Capacitor C120 is the block capacitor of VDD.

c-e) DGND, AGND, SUBGND
Digital, analogue and substrate GND's.
In the layout, the analogue GND should be connected to the reset circuit. The substrate GND should also be connected to the analogue GND.

f) VREF
The reference voltage of the decoder is no longer used. (Resistor R128, however, enables a connection between decoder and µC.)

g-h) XTALIN, XTALOUT
Connections for the decoder quartz Q120 (1.2001 MHz)

i) CMP1IN
CMP1IN is set to V_{dd} by a pull-up resistor R125

k) CMP2IN
Comparator input, generates a clock at DCDCCLK.

l) EXTC
The decoder can switch its internal voltage supply from Vbat (battery voltage) to Vcc (DC-DC converter 3V). This happens when Vbat drops below 1.05 volts; the critical path bit is then set. For this, the capacitor C123 must be connected to this pin so that switchover can take place without a voltage dip. EXTC delivers the signal for \RESET at the decoder.
At the critical voltage, OUT0 goes for a moment to logic low. Together with the critical path bit, the decoder switches from Vbat to Vcc.

m) AIFIN
Data input for 455 kHz IF signal
The DIFIN is normally used in the DE516C. This is why the AIFIN pin is connected to GND.

n-q) INT0...INT2, INT4
These inputs are also not used and are therefore connected to GND.

r) TEST0
This pin is only used in a special test mode (decoder). For this reason, it is also connected to GND.

s) DCDCCLK
Generates a clock so long as CMP2IN is at logical low. This signal is connected to the digital input DIFIN. At this output the clock frequency is switched on and off in step with the incoming data at CMP2IN.

The following lines are described in Section 2.1.2.3 Interface bus :

a) COMMON
b) SEG0

The following lines are described in Section 2.1.4 µController :

a) \CS
b) DIN
c) SCLK
d) DOUT
e) UPIR
f) INT3 TX
g) CRFLAG (\RESET)

2.1.4 µController

2.1.4.1 General

The µController (µC) is an 8-bit processor from the 38-family from Mitsubishi.

The clock frequency of the µC is produced by the crystal Q100 and die capacitors C101 and C101. The resistor R100 is fitted to give a better build-up. The quartz circuit is formed by the following components. The clock frequency of the µC is 2.457 MHz.

Capacitor C100 is the back-up capacitor of the µC.

2.1.4.2 Miscellaneous lines

Reset	Reset is triggered by the reset component IC170
Vcc, GND	Voltage supply 3V
Xout, Xin	Clock frequency 2.457MHz
Vref	Reference voltage for switching in V_{dd} via T100.

2.1.4.3 Port 0

CMOS Port. address lines to SRAM

0-7 A0-A7 Address port for the lower range.

2.1.4.4 Port 1

CMOS Port. address lines to SRAM

0-7	A8-A15	Address port for the upper range.

2.1.4.5 Port 2

CMOS Port. Data lines to SRAM, data ROM and LCD driver.

0-7	D0-D7	Data port

2.1.4.6 Port 3

CMOS port. Control lines to SRAM

0	A17	Additional address line for the data ROM
1	A16	used as extra address line for the 1Mbit SRAM.
2	\ONW	Pull-up resistor R101
3		Reserve
4		Reserve
5		Reserve
6	\WR	Write
7	\RD	Read

2.1.4.7 Port 4

CMOS port. Connection to LCD driver, decoder, external interface

0	VRef_Switch	Switches V_{ref} over to V_{dd}
1		Reserve
2	INT_Crete	Interrupt input, connected to the decoder
3	INT_PCD	Interrupt input for additional decoder.
4	RX	RX line to read data from the external interface.
5	TX	TX line to write data to the external interface. Normally logical low. A change (pager in programmer) is detected by IC120 when the TX level is set to logical high.
6	SCL	Clock line I2C BUS
7	SDA	Data line I2C BUS

2.1.4.8 Port 5

CMOS Port, (motor, buzzer, background lighting and buttons).

0	MOTOR	Control line for the motor (vibrator)
1-3	KEY0-2	Button interrupts
4	/INT	Input for 12 second interrupt of the real time clock
5	LSCLK	Frequency for the buzzer
6	LSAMPL	D/A converter, determines the amplitude of the beeper
7		Reserve

2.1.4.9 Port 6

CMOS Port, control lines for LCD driver and measuring of Vbat.

0	VBAT	A/D converter to measure the two battery states: low and discharged. Low battery state is displayed in the LCD. Discharged battery is used to switch off the pager. The digital part remains in operation, even when the HF stage no longer receives. The pager is therefore switched off at a minimum battery state.
1	NTC2	Temperature measurement
2	\WRLCD	Write for the LCD driver
3		Reserve
4	\RDLCD	Read for the LCD driver
5	Light_LCD	Switches on backlighting
6		Reserve
7	RSLCD	LCD address bit switching control/display data

2.1.4.10 Port 7

Open drain port, temperature measurement, connection to decoder

0	SIN_UP	Serial interface to decoder (write)
1	SOUT_UP	Serial interface to decoder (read)
2	SCLK	Clock for the interface
3	RST_CRETE	The decoder can be reset with this line from the µController. A time delay can be set by capacitor C117 together with the internal resistance in the decoder.
4	NTC	used to measure temperature, normally open
5	\CSROM	
6		Reserve
7	SW_RST	Possibility to trigger a hardware reset via the µController. Connected to the port IC170 voltage detector.

2.1.4.11 Port 8

CMOS Port, connections to decoder and PLL

0	\CSCRETE	Chip-Select Crete (decoder)
1	PLLEN	Reserve (DE800: enable for the PLL)
2	Batt_Mes	artificial load for measuring the battery
3		Reserve
4		Reserve
5		Reserve
6	EECLK	Connected to EEDAT for recognising the I2C EEPROM
7	EEDAT	

2.1.5 Static RAM (SRAM)

Size: 128k∗8 bit
Package: 32-TSOP

Operating voltage: 3V ±10%
Data retention voltage: Min. 2V

All messages and system data (program, typeface, menu, icons, RIC etc.) are stored in SRAM. A special backup battery allows the storage of these data in SRAM over a period of years (see also Section 2.1.8.2 Backup battery).
Capacitor C150 is the back-up capacitor for the RAM.

2.1.6 EEPROM

Size: 1024 bit (128 bytes)
Package: 8-TSOP

The following data are stored in EEPROM:
- Pager definitions
- Production data
- Serial number

The data are copied into and stored in SRAM during normal use.

2.1.7 Real Time Clock

Package: 8-TSOP

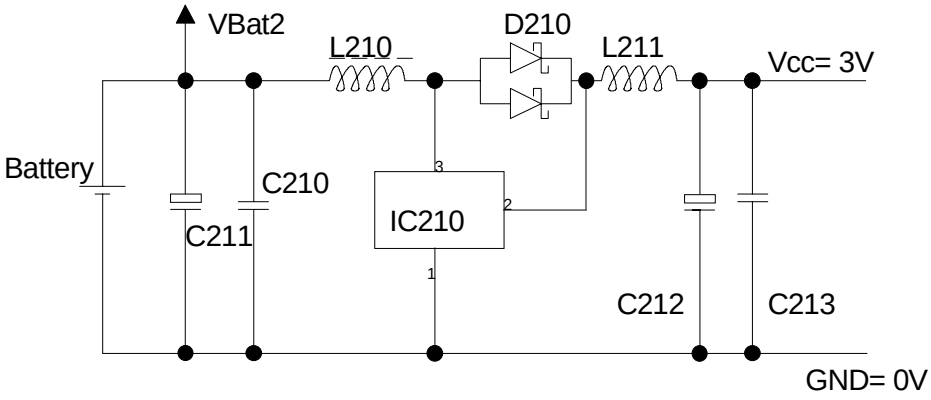
Operating voltage: 1.8 to 5.5 V
Data retention voltage: Min. 1V

In the real time clock IC 141, a clock runs on the basis of the 32.768 kHz quartz. Seconds, minutes, hours and years are counted. The programmable interrupt is set to 12 sec. A special backup battery allows the clock time to run on for a period of years (see also Section 2.1.8.2 Backup battery).
Capacitor C140 is the back-up capacitor for the real time clock.

2.1.8 Power-Management

2.1.8.1 DC/DC converter

The following diagram shows the basic circuit of the step-up converter which consists of IC210 (RH5RC301A from RICOH), the coil L210, the Schottky diode D210 and the charging capacitor C212 . The primary energy source is a battery supplying 0.9 to 1.5 volts. The choke L211 should suppress high frequency interference in the converter.
The variable Vbat voltage 1.0V ... 1.5V is set to a constant supply voltage of Vcc = 3.0V.



In an initial phase, the coil of IC210 is switched in for a defined period of time. The current in the coil rises. The maximum current produces the magnetic energy $W_M = i^2 L/2$ in the coil.
In the second phase, the coil is switched off. The stored magnetic energy passes to the storage capacitor. The Schottky diode prevents discharging of the charging capacitor during the first phase.
The converter has a slight voltage ripple because of the on-off control.

2.1.8.2 Backup battery

The lithium battery BAT160 supplies the SRAM and the real time clock if the normal battery is discharged or is not being used.
To prevent discharge during normal pager operation, the lithium battery is disconnected from the supply voltage via T160. If V_{dd} drops out, the supply voltage is switched over from V_{dd} to V_{Lith} by means of IC170 (voltage detector). At the same time, the RAM is brought into a special low power mode.

Transistor T160 prevents discharge of the back-up battery should no battery be in use (data retention). \RAMCS must be set to logical high during the data retention period. CE2 of the RAM must be at logical 0.

2.1.9 Temperature Measurement

Is not used in the DE516 at the moment.
The temperature can be measured using the resistance network made from R107 and NTC R105. For this, Vref is switched in via P4.0 to supply the A/D converter.

2.1.10 Backlighting

The backlighting consists of an optical fibre and two double-LEDs. The supply voltage level is Vbat. The voltage for the LEDs is raised by means of a switched inductance. This is produced with the clocking of an astable time-base circuit consisting of T200 and T202.
R204 und R205, together with C202, form a low-pass filter to reduce HF interference.

Voltage: V_{bat} = min. 1V
Frequency: approx. 35kHz
Sampling ratio = 1 : 1:1

2.1.11 Buzzer

The buzzer circuit is so designed that the frequency and amplitude can be changed. It is driven by the µController.

Voltage:	V_{bat} = min. 1V
L_{sample}:	Amplitude = max. 3V
L_{sclk}:	Frequency = approx. 2800Hz

2.1.12 Vibrator

The vibrator motor is driven by the µController. The supply voltage is V_{bat}.

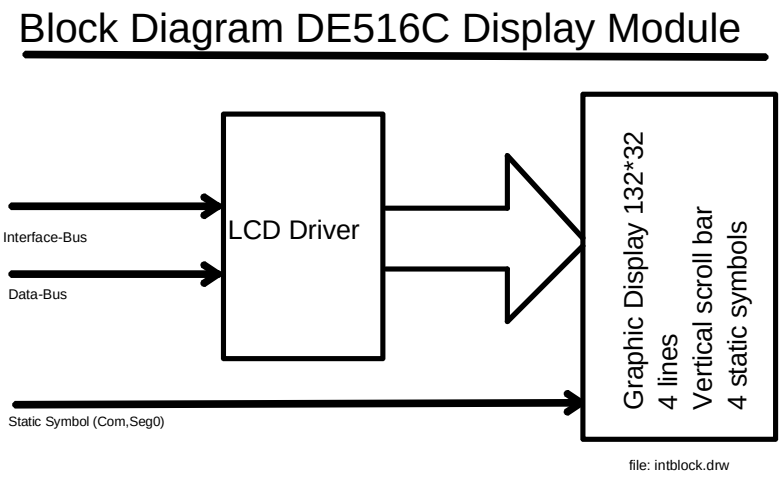
2.1.13 Peripheral Interface

The peripheral interface contains the following contacts:

V_{bat}:	Input from battery / external aerial connector
RX:	Communication with PC, receiver, adapter recognition
TX:	Communication with PC or printer, transmitter, adapter recognition
GND:	GND
GND/s:	Static GND, protection against electrostatic charges

2.2 Display Module

2.2.1 Block Diagram



2.2.2 Interface between Digitalprint and Display Module

The interface between the two modules is a 51-pin soldered strip. The display driver is connected to the µC by this strip. In addition, there is a heatseal connection between the glass and the Digitalprint. The static On Symbol is driven by this connection.

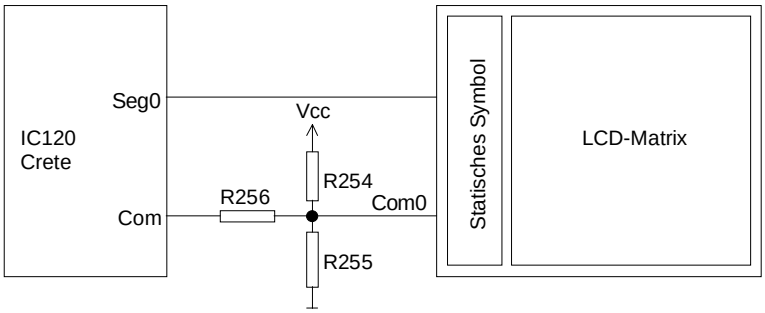
2.2.3 Technical Data

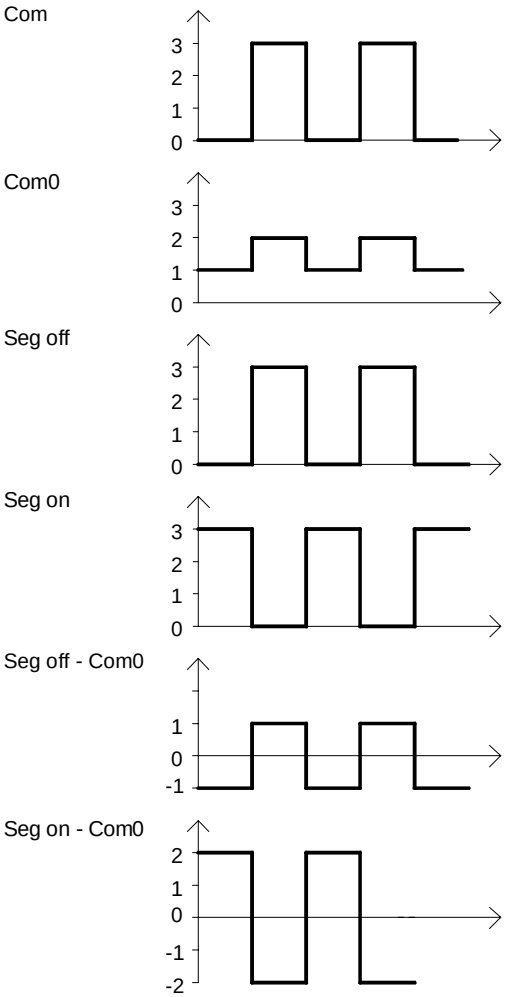
Visible area:	Min. 22.35mm ∗ 60.40mm	
Lines:	4	
Characters:	Min. 80	
Colour:	Yellow-green, supertwist	
Display:	Full graphic (32 ∗ 132 pixels)	
	for text:	32 ∗ 120 pixels
	for icons:	32 ∗12 pixels
Static symbols:	One	
Symbols:	No reception New message Battery low	
Special:	Vertical scroll bar:	shows the length of the message
	3 icon fields:	optical indication of the buttons
LCD voltage:	Graphic field:	6.34V at 25°C Bias: 1/7
	Static symbols:	min. 1.4V
LCD frequency:	Graphic field:	62.5Hz (frame frequency)
	Static symbol: 97.7Hz	

2.2.4 Static Symbol

The static symbol is controlled by the decoder. The CMOS output of the decoder has a value of 3V. This voltage must be reduced to obtain a good contrast. This reduction is carried out by the resistors R254 and R255.

Manufacturer's specifications:	Optimum	1.45 V
	90%	1.4V ... 2.2V
	80% and less	2.5V

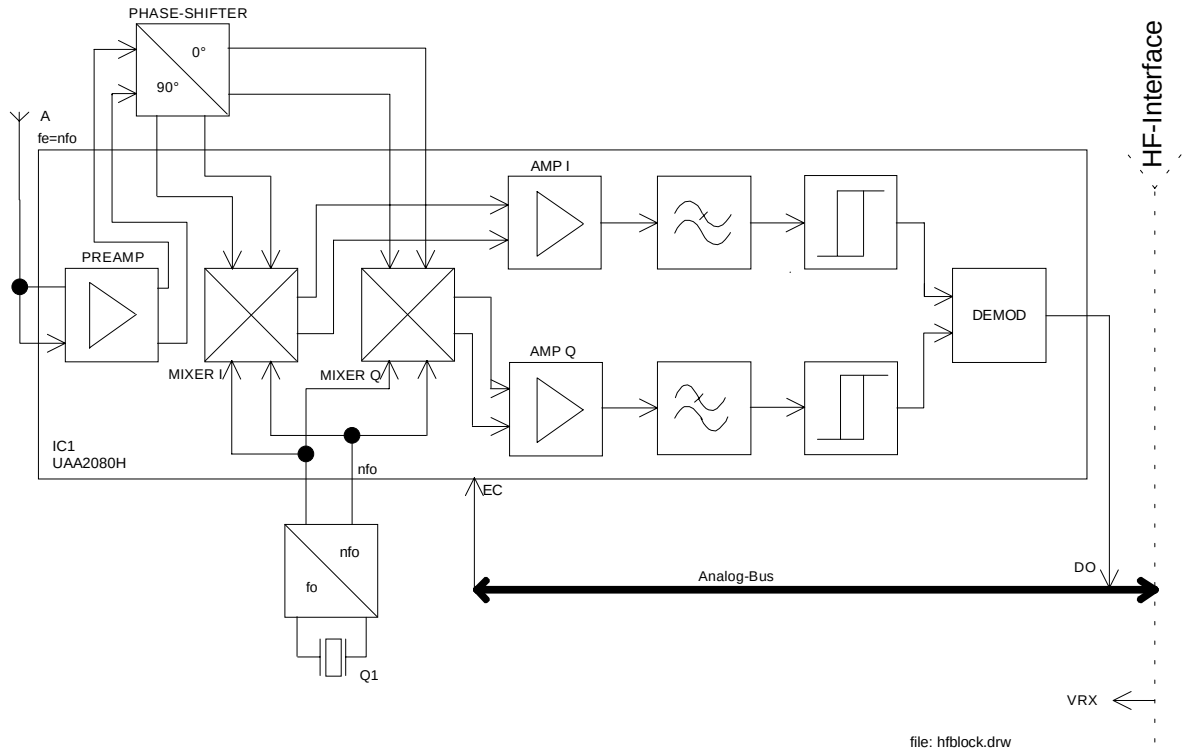




3 HF Stage

3.1 Block Diagram

Blockdiagramm DE 516 Ex, Mainmodul Analogteil



3.1.1 Summary

The HF stage is implemented by a direct conversion chip from Philips. This chip converts the HF signal directly into a digital stream of data.

3.1.2 Aerial / Preamplifier (LNA)

Two alternative aerial types can be fitted, depending on the pager. The ferrite aerial can receive frequencies up to 200 MHz. A frame aerial is necessary for higher frequencies.
The components C4, C5 and C6 are used to adapt the aerial properties to the IC UAA2080H. A coupling using C1, L1 and C3 has been provided to enable the attachment of an external aerial to the pager.
L2, L3 and C22 form the output tuned circuit of the LNA. The necessary supply voltage for the LNA is fed via L2 and L3.
The gain of the LNA is adjusted with R1.

3.1.3 Phase Shifter with Adaptation

The output signal of the LNA is picked symmetrically off the C22 and decoupled via C23, C24 and C27. C27 assists in the impedance transformation. The signal is then split into two paths that are shifted by +45° and -45° respectively to the signal received. Because of the balancing, these splits are present in duplicate (C26 / L4 and C25 / L5).

3.1.4 Quartz Oscillator Circuit

The harmonic mode crystal Q1 is actively driven by UAA2080H. The impedance compensation (L9, C12 and R2) ensure a fast build-up time. Trimming the oscillator frequency is possible by changing the ratio of C10 to C11.

3.1.5 Harmonic Generator

Depending on the pager, the quartz frequencies are increased by a factor. The factor is divided into two stages:
A) harmonic generator: a bandpass filter lets through only a certain harmonic of the oscillator.
B) mixer: the mixer amplifies the signal coming from the harmonic generator and adds new harmonics. The mixer's filter finally filters out the necessary frequencies.
The bandpass filter consists of C14 and L8, C13 and R3. R3 is for damping.

3.1.6 Mixer / Demodulator

The signal from the phase shifter is mixed with the processed signal from the oscillator. The working impedance from C15 and L6/L7 forms the oscillator circuit. The gain is adjusted with R4.
As the oscillator signal has the carrier frequency, the mixed product reaches also into the baseband where the digital quadrature demodulator that follows it can directly process the signal.

3.1.7 Digital – HF Interface

The interface between the digital and HF stages consists of a 6-pin plug-in connector strip. These pins are for the battery supply V-Bat , GND, data line (Do) reserve pin, economiser line (EC) and V_{dd}. The receiver is switched on and off by the economiser signal. When the receiver is switched on (EC=high), the result is a stream of data at pin 3. It is possible to measure the baseband signals at the test points TP1 and TP2.

3.2 General

3.2.1 ESD Protection

The capacitors C231 and C232 protect the RX and TX lines that connect the interface with the µController.
The diode D1 protects the HF stage against ESD.

3.2.2 External Aerial

The external aerial is supplied from Vbat (plug V230.1). L230 decouples the signal to the digital stage.
The signal is fed into the HF-Print via the socket BU1 and coupled into the aerial circuit via C1/R8 and C3.