Technical Description
DE 506

Contents

4. Technical Description

4.1. Introduction

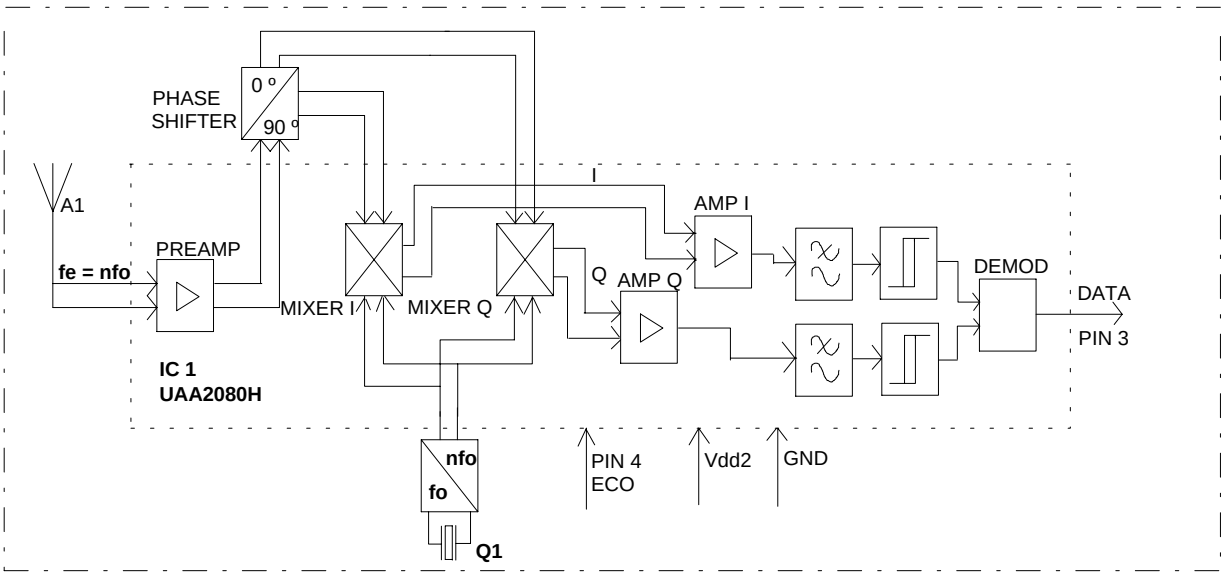
4.1.1. General

The Swissphone Information Pager DE 506 combines the most advanced technology with its compact form.
The "Direct Conversion" DFSK POCSAG Paging Receiver is controlled by a CMOS - microprocessor and is fed either by 1.2V accumulator or by 1,5V dry battery.

The receiver contents two functional parts sandwiched and connected over 6-pin plug-socket connection.

The Liquid Crystal Display (LCD) is fixed to the digital module with the help of a metal frame.

4.1.2. RF-Block Diagram



The radio signal received over antenna (A1) is amplified internally in IC1 (differential input) and is split thereafter in a phase shifter into two signals 90° apart from each other.

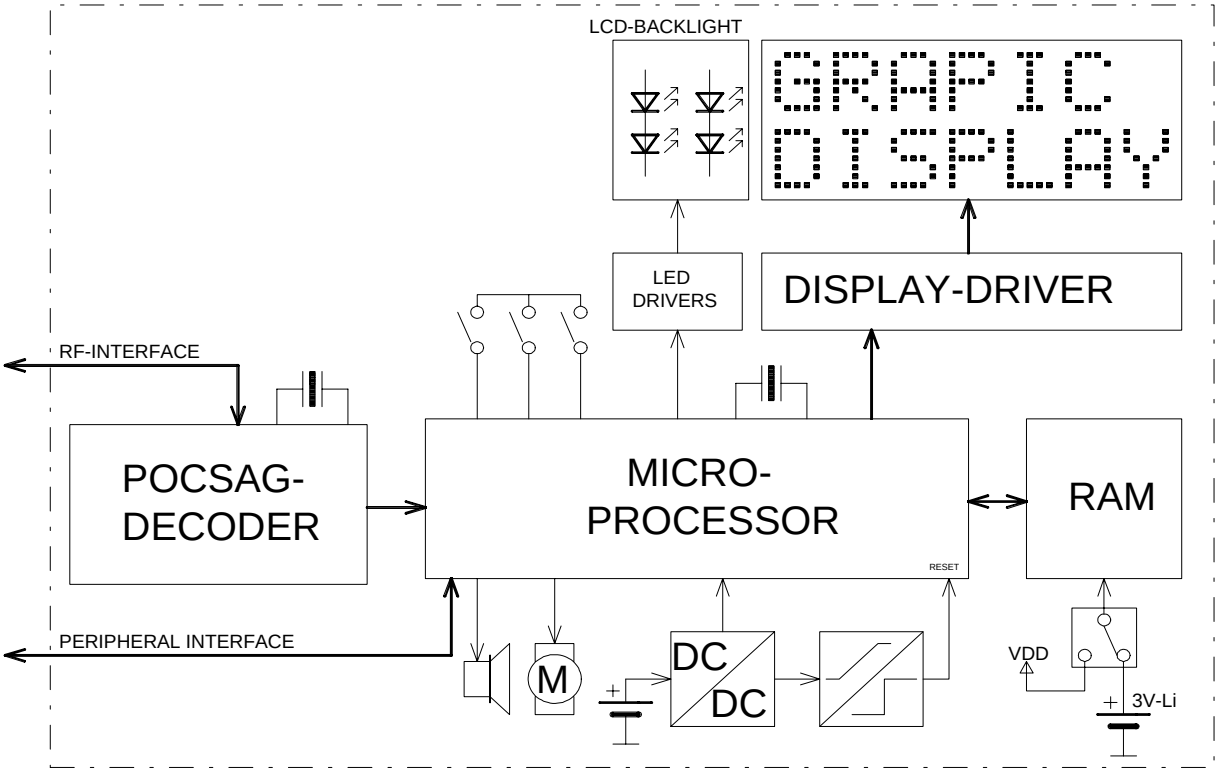
Both the signals are mixed in two identical mixers in IC1 with a local oscillator, which lies with Direct Conversion principle directly on the reception frequency (n*fo = fe).

The quartz Q1 oscillates at a lower frequency. The output signal of the quartz is multiplied by n in relation to the Reception Frequency (see chapter 4.2.2 Oscillator).

Both the signals (I and Q) gained after the mixing, are in AF range and are still phase shifted by 90°. They are filtered within IC1 (necessary gap from neighbouring channels), amplified further, limited and lead to a quadrature demodulator. The output signal at pin3 corresponds to the digital DFSK-POCSAG signal which is lead to the Digital Part for further processing.

The DC-IC is switched off through the Economizer Signal (ECO) in certain time intervals in order to save battery power.

4.1.3. Digital part-Block Diagram



The serial data stream (POCSAG-Coding) with its corresponding transmission speed of 512, 1200 or 2400 Bits/s is evaluated by the decoder. The POCSAG decoder "PCF 5001T" also includes the EEPROM for RIC addresses and the pager configuration.

The decoded signal is now passed over to the microprocessor (U1) in the blocks of four bits. The data are then structured and stored in 32kx8 full S-RAM (U2). In addition to that, in case of an incoming call or corresponding operation of the pager, the text data are sent to both LCD drivers situated on the Digital Module. The data are then displayed on the LCD.

The operating voltage V_{DD} of 3V is produced by a DC/DC converter. All the components are defined for this voltage, the only exception being the programming of EEPROMs (see chapter EEPROM).

The RS-232 interface and the acknowledgement of the adaptation related to it, is supervised by the microprocessor (see the description of periphery interface). The battery voltage V_{batt} as well as the operational voltage V_{DD} is constantly monitored by a voltage detector and the information is passed on to microprocessor for further processing and the corresponding signals are displayed whenever necessary (Low Battery alarm). The user can change the battery or recharge the accu, as the case may be.

4.2. Functional Description RF- Part

4.2.1. RF-Chip

The whole processing on the RF-Stage is carried out by the RF-chip UAA2080H (IC1). The chip works on the principle of Direct Conversion. This means that the mix frequency of the local oscillator is identical to the reception frequency.
The processing is carried out basically over symmetrical signals and not over ones referenced to Ground. Due to this, some steps have two inputs for one signal (differential input).

The antenna A1 is adapted to the Input-Stage (in IC1) by the capacitors C4, C5, C7, C8 and the trimmer C6. After the pre-amplification (also within IC1), the signal is split into two signals 90° phase shifted. This is achieved by turning the phases of L4 and L5 in one direction and the phase of C25 and C26 in the other direction. The elements L2, L3, C23, C24, C27 and the trimmer C6 form the adaptation from the output of pre-amplifier to the phase shifter.

The mixing of the both signals with the local oscillators (see chapter Oscillator 4.22), as well as the filtering, amplification with limitation and modulation following thereafter, are carried out in the RF-chip internally. The RF-chip provides the demodulated digital DFSK-POCSAG signal on pin 3 for further processing.

4.2.2. Oscillator

The oscillator is built on the principle of "Colpitts" and consists of basic elements Q1, R2, L9, C10, C12 and the trimmer C11 (fine adjustment of oscillation frequency). The active part of the oscillator is built in the Receiver-chip.

The Quartz (3rd harmonic wave) oscillates on an integral part of the reception frequency and must be multiplied by the corresponding factor n. The factor n depends upon the reception frequency range.

UHF (430 - 470 MHz)	n = 6
VHF (138 - 174 MHz)	n = 3

The required multiplication is achieved through two stages. The active parts thereof are within the chip. Outside the chip, two corresponding tuned circuits can be recognised, which are formed on one side by L8, C14 and C13, and on the other side by L6, L7 and C15.

4.2.4. Economizer

The control of the RF-chip (over pin 4) is taken over by the Digital part (Decoder). If the EC input of the receiver lies on the "Low" (or GND), it is in the "Stand By" mode. In case of "High", the receiver is in the "Normal Operation" mode.

4.3. Functional Description of Digital-Module

4.3.1. POCSAG Decoder

The PCF 5001T is a decoder capable of decoding CCIR Radio paging Code 1 autonomously. In other words, it can carry out functions like address comparing, synchronisation, economising the RF-part, error correction etc. without help of the microprocessor.

4.3.1.1. Addresses

The PCF 5001T allows four RIC-addresses in two different frames.

Frame 1: RIC A & B (1. and 2. main addresses)
Frame 2: RIC C & D (3. and 4. main addresses)

The RICs (excl. last three LSB`s) are stored in the internal EEPROM-Arrays #1 and #2 (See chapter EEPROM)

4.3.1.2. Economizing of RF-Receiver part

The economising is done to save battery power and thus increase its life. It is supported by the basic structure of POCSAG-Code. It is achieved by switching off the receiver part during pre-defined intervals depending upon the RIC code. The receiver is switched on only during the time slot corresponding to the RIC code of the pager (total 8 time slots) and is switched off for the rest of the time. Switched-on period is increased by response time of the oscillator (receiver establishment time). Four values of this time can be set in PCF 5001T via EEPROM (These values are dependent on the transmission speed).

4.3.1.3. EEPROM

The internal EEPROM of the decoder (in addition to RAM) is used for storing address and options. The 5V voltage required for programming EEPROM cells is supplied by the programming unit over the VBATT interface line. The pager DE506 itself can produce 3V voltage only.
The EEPROM is programmed over an external interface via microprocessor.

4.3.2. Microprocessor

The microprocessor carries out the data handling e.g. data comparing, word processing, alarming, LCD-driving and outputs via RS-232 interface. It activates the clock (Time Stamping) and carries out commands of push buttons. The symbols are driven by the internal LCD-driver.

4.3.3. DC/DC Converter

The RH5RC301 (U9) is a step-up converter which converts the battery voltage of 1 - 1.5V into 3V (VDD) required for the digital logic. The internal FET switch of the converter is switched with the frequency of 60 kHz. It charges a smoothing capacitor with stored energy through a coil. This process is continued till the internal comparator finds the output voltage, fed back over an internal voltage divider, as sufficient and then switches off the RC-oscillator.

4.3.4. CMOS-RAM (Battery-supported)

The RAM (IC8) is a fully static RAM with a capacity of 32 kbytes. Various data stored therein are e.g.:

- messages
- battery threshold value
- serial number of the pager
- RIC's (Radio Identification Codes)
- company logo
- fonts (scripts)
- user guide (languages)
- various user parameters

These data are written on the RAM during the programming process. As this RAM has to be supplied with operating voltage constantly, it is supported by a 3 Volt lithium battery BT2. The above mentioned data are thus secured. When the pager is in operating mode, the RAM receives V_{DD} 3V power internally from the pager. During the time when the battery is being changed or when it is completely discharged, the lithium battery automatically comes into action to supply the required power for RAM.

4.3.5. Display-Driver

A LCD-driver which is mounted, with "Tape Automated Bonding (TAB)" technology, on the rear side of the Digital board, is controlled by the microprocessor via eight data lines D0..D7 and various control lines of the microprocessor.
In this driver, there is voltage tripler which, with the help of an external capacitor, produces the 6.5V required for the LCD glass.

4.3.5.1. Liquid Crystal Display (LCD)

The display contents 5 symbols and a "Dot-matrix-Array", which is arranged fully graphically. The LCD is driven at the multiplex rate of 1:32. The menu symbols are illustrated through the dot matrix on the full graphic display. In this way all the symbols and the corresponding functions can be switched on and off. The pager displays date and time in standby mode (programmable option: display switched off with the exception of "ON" symbol).

4.4. Periphery-Interface

4.4.1. General

The pager DE 505 recognises through this interface, which periphery unit it has been adapted to. Depending upon the type of periphery unit, the messages can be read out individually. There is also the possibility of connecting an external antenna over the periphery unit.
Accumulator battery can be charged over this interface. Therefore no Pager with dry cell (alkaline battery) should be inserted.

Following peripheral units can be used for DE506 pager:

LG 505/510	simple charging device
LGA 505/510	charging device with antenna connection
SG 505	interface unit, allows communication with a PC or a serial printer.

4.4.2. Pin connections

PIN 1 "V batt."
This pin is directly connected to the Plus contact of the accumulator battery. It is meant for charging the battery and feeding a radio signal (external antenna connection).

Attention! Do not insert a pager with dry cell in the charging device.

PIN 2 "RX" / PIN 3 "TX"
The connections RX and TX (TTL signal 0/5V) enable the communication with a PC.
Rx enables reading and TX enables writing data.

PIN 4 "GND"
Connection to Ground.

PIN 5 "GND/s"
This pin is used for draining away statical charges of the pager, over a resistor (EMC).