Attachment AE
Post Crash Immersion Capacitor Failure Analysis

KEMET

Final Corrective Action Report
(Business Confidential)
Date: January 9, 2003

Reference Information

Customer CA#: N/A	**KEMET CA#**: P253H
Customer P/N: C0603C102J3GAC	**KEMET P/N**: C0603C102J3GAC
Date Reported: December 18, 2002	
Area: Electrical	

Description:

DME Corporation returned one demounted capacitor of P/N C0603C102J3GAC for failure analysis due to low insulation resistance. The customer reports that the capacitor failed as a short during functional testing. No lot number information was provided for the capacitor in question.

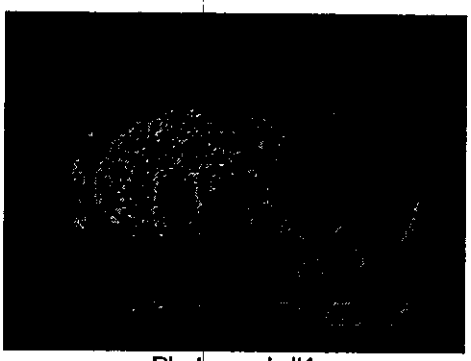
Corrective Action Team:

Gabriela Macias, Quality Manager
Abel Rodriguez, Process Engineer
Matt McNeary, Ceramic CQE Manager
Miguel Sanchez, Failure Analysis Technician
Alicia Cruz, Customer Quality Engineer

Problem Analysis:

Step 1. Physical Analysis

Physical analysis was performed on the returned capacitor as received using a light stereoscope at various magnifications. Excessive solder and flux residues were observed on this part (see Photograph #1).



Photograph #1

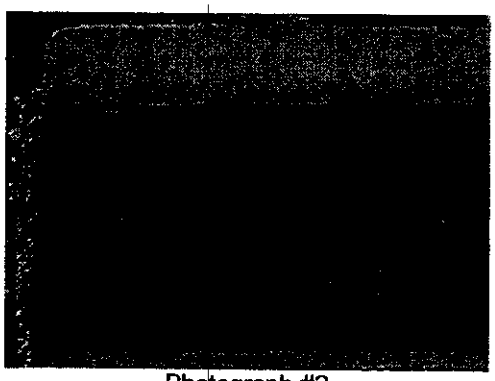
Step 2. Electrical Measurements

Electrical measurements on the demounted capacitor were taken. Results revealed that the capacitor exhibited insulation resistance of <100 K-Ohms; therefore, the capacitor was considered to be electrically short.

Step 3. Cross-sectional Analysis

The demounted capacitor was mounted in clear acrylic resin for cross-sectional analysis. Layers of the capacitor were carefully removed using very fine grit grinding disks, and the exposed areas were microscopically examined for a failure site. A metallograph utilizing polarized light was used throughout the analysis.

A parallel plate crack of thermal stress nature was noted on the capacitor (see Photograph #2). No KEMET manufacturing anomalies were noted on the returned part.



Photograph #2

Containment Action:

Unfortunately, no date code information was provided for the returned capacitor making it difficult to examine historical batch records.

KEMET provides ongoing containment through sample testing at our Destructive Physical Analysis (DPA) process monitoring station, as well as 100% electrical testing.

Root Cause:

The thermal shock crack formed after the capacitor was soldered onto the PCB at DME Corporation. With time and humidity, the insulation resistance degraded along the crack site until the capacitor failed during use. KEMET could not have detected this capacitor as a failure prior to shipment.

Corrective Action (Selected, Verified, Implemented):

KEMET continually strives for increased robustness of ceramic chip capacitors. Some of our projects have focused on improvements in customer handling and soldering, while other projects have focused on improvements in the capacitor itself. Cracks can occur when chips are thermally shocked by improper use of a manual iron while performing touch-up or rework operations. Thermal shock cracks can also occur if severe temperature profiles are used during the soldering process. KEMET suggests that DME Corporation review the manufacturing process for areas that may introduce thermal stress on the capacitors during board assembly or rework.

KEMET Process Enhancements

With the use of designed experiments, the KEMET team verified that optimizing the dip cycle in the termination application process to produce a denser termination results in improved chip robustness. This has been confirmed by a reduction in mechanical/thermal stress cracks as evaluated by KEMET's accelerated Board Mount Test (BMT) and Destructive Physical Analysis (DPA).

KEMET's Board Mount Test (BMT) assesses the product's ability to withstand customers' assembly operations without developing a mechanical/thermal stress crack. It is meant to stress the chips much harder than would be expected during a customer's soldering process. BMT consists of mounting chips on an FR4 substrate using a solder wave with a thermal shock of 180°C. The mounted chips are placed in an environmental chamber at 85°C and 85% RH with rated voltage applied for 20 hours. Afterwards, insulation resistance is measured. BMT is intended to accelerate the creation of a mechanical/thermal stress crack by exposing chips to an elevated thermal shock (180°C compared to 90°C - 120°C for typical customer solder waves) followed by exposing chips to the environmental conditions of temperature, humidity, and voltage. Failures are analyzed to determine root cause and estimate failure rate. The optimized termination application process was implemented on July 1998.

KEMET continued the effort to drive the accelerated test PPM further down. Experimentation next focused on the end termination firing process. The KEMET processing variable observed is heat work, the product of kiln temperature and soak time. As heat work is increased, the glass frit in the silver end termination diffuses further into the capacitor body. In addition, silver from the end termination diffuses into the silver-palladium electrodes as heat work is increased. These two effects can result in a stress riser which reduces thermal and mechanical robustness when heat work is on the upper side of the allowable operating range. By narrowing the process window for heat work to the lower end of the operating range, KEMET confirmed adequate sintering of the end metallization while eliminating the potential for stress riser creation. This optimization was implemented in March 2000.

Based on the internal design of the capacitors, KEMET is confident that these parts were manufactured prior to the implementation of this corrective action.

Preventive Action:

KEMET will continue to monitor the performance of this part type through the use of KEMET's management review system.

KEMET is committed to working with DME Corporation to resolve this concern to your satisfaction. If we can be of any further assistance or if you have any questions concerning the content of this report, please contact us via phone, fax, or e-mail (listed below).

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