THEORY OF OPERATION

TM-882A

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This PLL - controlled VHF marine transceiver provides an accurate and stable multi-channel operation.
The transceiver consists of 6 main sections:

- **Transmitter**
- **Receiver**
- **Low Voltage Detection**
- **Weather Alert**
- **Local Oscillator PLL (Phase Lock Loop) Circuit**
- **Memory Backup**

- **Transmitter**

  The audio is picked up either from the internal or external MIC, the audio signal is then amplified by Audio Amplifier, IC205 NJM3403 (4/4), IC205 NJM3403 (3/4) and filtered by a low pass filter IC205 (2/4), IC205 (1/4). The audio is adjusted with VR2 to obtain a suitable Audio frequency response, and then modulated with the carrier by VCO, through Varicap diode D7.

  The modulated signal output from the VCO is amplified by Q14, Q2, Q3 and Q4. When the supply voltage is 7.2 V, this signal will be amplified up to 2W and 5W when supply voltage is 13.8 V. The amplified signal then passes through a low -pass filter network which consists of L6, C18, C70 filters out spurious emission, and the antenna switching circuit, D1, D10. The signal is filtered by another low-pass filter circuit which consists of L1, L2, C1, C8, C9, C15 and C16. These low pass filters are necessary to suppress the second and third harmonics. The signal is then fed into the antenna input terminal and radiated out. The signal is also fed into another path consisting of C55, R77, D3 for sampling, and is converted into a direct current voltage for the Automatic Power Control (APC) circuit Q9, IC2, Q7. Q7's collector current is used to maintain the output power stability.

  When the unit is transmitting, the audio signal is added to the TX VCO Varicap diode D7. The capacitance of D7 is varied following the audio signal and when mixed with the carrier to form the modulated signal.

- **Receiver**

  The receiver uses a double frequency super-heterodyne circuit. The first Immediate Frequency (IF) is 21.6 MHz and the second is 455 kHz.

  The RF signal is received by the antenna, and passes through a low-pass filter network L1, L2,C8, C9, C15, C16, to filter out the unwanted signals, the antenna switching circuit D1, D10 switching circuit to receive. The received RF signal then passes through a RF transformer T5. And is amplified by RF amplifier Q18. T2, T3, T4, C60, C61, C10, C62

form the band pass filter. The RF signal then is mixed with the local oscillation frequency by the mixer Q19. A first IF (Immediate Frequency) 21.6 MHz is produced. The IF is passed through a coil L11 and a pair of crystal filter F1 and F2 to further filter other unwanted signals. The first IF then is amplified by Q1 and the FM IF demodulation IC1 (DBL5018V) which consists of a local oscillator, a demodulator, a second mixer, squelch control circuit, and RF amplifier. The 21.6 MHz IF then is mixed here with second mixer and converted into 2nd Immediate Frequency (IF) 455 kHz. The 2nd IF passes through a ceramic filter F3 to filter out the residue unwanted signal at pin 5 of IC1 output this final IF signal and the Audio signal is output at pin 9 of IC1 (DBL5018V).

The audio signal is fed through demodulator circuit R35, C80, R10, C116 and amplified by Q6, Q206. The amplified audio then passes through a volume control VR203 and finally amplified by Audio amplifier IC206 (NJM386) and heard in the speaker.

The squelch control is also controlled by IC1 (DBL5018V). The second IF passes through low pass filter R6 and C30. IC1 (DBL5018V) internal squelch control R48, R49, C113, C112 and R50 form as a squelch amplifier. The ceramic filter produces a squelch signal (RF noise). This signal is amplified by Q5 and regulated by D4 to produce a direct current voltage as a control voltage. The control voltage then is input to pin 12 of IC1 (DBL5018V); pin 13 of IC4 sends the digital squelch control signal to the MCU mute the audio speaker path. The 8 level squelch control is performed by IC208. IC208 (NJM4051) is an integrated 1 out of 8 squelch level controlled by SQD1, SQD2, SQD3 from the MCU. The ladder network R257 – R265 and IC208 form a variable resistor network which corresponds to the squelch level.

- **Low Voltage Detection**

  The battery voltage; divided by R215, R214 is input to IC204 for voltage level comparison. If the battery voltage drops below 6.2V, IC204 (XC61CN4302PR) outputs a low level to MCU to indicate the battery is in low state.

- **Weather Alert:**

  The second IF demodulated signal is output from IC1 (DBL5018V) pin 9 and amplified by Q12. When the Audio signal consists of a weather alert signal (1050 Hz) the audio signal also will be amplified by Q207 and reshaped to form an about 600 mV signal. The signal is input to an audio frequency phase lock loop filter IC207 (LMC567) pin 3. When the input frequency is equal to the IC207 internal oscillating frequency (1050 Hz), pin 8 of IC207 (LMC567) will output a low level to the MCU.

- **PLL (Phase Lock Loop) Circuit:**

  Both the receiver and transmitter share the same PLL (Phase Lock Loop) Circuit to produce the receive carrier or the transmit frequency. A phase Lock Loop (PLL) IC3 (M56760), TX VCO Q16 and RX VCO Q15. The fundamental frequency is determined by X2 (12.8 MHz) and as the PLL reference oscillator. This signal is frequency divided by IC3 and a 6.25 kHz signal is produced. When the VCO frequency applied to and frequency divided by IC3 produces a frequency comparable to 6.25 kHz, PLL will control the VCO. When these two frequencies are matched, a constant control voltage is output from PLL to lock VCO in desired frequency. The PLL also will output a lock indication to MCU to indicate the PLL is

in frequency lock status.

- **Memory Backup**

  IC202 is an EEPROM AT93C46 that acts as a memory backup for the working channel code and the system parameters. Every time when the unit is switched on, the MCU will reset the system, clear the RAM, and recall in the memory from the EEPROM to refresh the RAM in MCU IC201.