Memo

Date: March 14, 2002

To: CKC

CC:

From: P-Com

Subject: Processing Gain

1. Scope

This Memo presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain on the AirPro Gold 20F. Family Products.

2. Applicable Reference Documents

1. "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" Title 47 Part 15 section 247 (e) Code of Federal Regulations. (47 CFR 15.247).
2. "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.
3. "HFA3861B Direct Sequence Spread Spectrum Baseband Processor" Harris Corporation Semiconductor Sector Preliminary Data Sheet, Melbourne FL, June 1999.
4. Sklar, B. "Digital Communications, Fundamentals and Applications", Second Edition, Prentice Hall, Inc., New Jersey, 2001.
5. Korn, I. "Digital Communications", Van Nostrand Reinhold Company, Inc., New York, 1985.
6. Lindsey, W.C., and Simon, M.K. "Telecommunications Systems Engineering", Prentice Hall, Inc., New Jersey, 1973.
7. Andren C., Webster M. "CCK Modulation Delivers 11Mbps for High Rate IEEE 802.11 Extension", Harris Corporation Semiconductor, Palm Bay, Florida, 1999.

3. Test Background and Procedure

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, PG of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-rate (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) at the case, where spread spectrum processes (coding, modulation) are engaged, relative to the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2]. In accordance with the new NPRM 99-231, if the vendor has a system with less than 10 chips per symbol, the CW jamming results must be supported by a theoretical explanation of the system processing gain.

4. Theoretical calculations

The processing gain for predefined reference SER (Symbol Error Rate) is related to the jamming margin as follows [2]:

$$PG = (E_S/No) + (J/S) + L_{sys}$$

Where (E_S/No) corresponds to theoretical output signal to noise ratio per symbol, (J/S) is the jamming margin and Lsys are the system implementation losses.

1.1. Implementation Loss

Since the maximum allowed system implementation loss is 2 dB then

$$PG = (E_S/No) + (J/S) + 2dB \geq 10dB$$

1.2. Jamming to Signal Ration (J/S)

The (J/S) must be measured for reference SER or BER (for example 1e-5 or 1e-6) using FCC suggested procedure and after discarding 20% worst ratios next worst (J/S) ratio must be taken for calculation.

1.3. Signal to Noise Ratio Value Definition

As above mentioned, the (E_S/No) ratio is a theoretical (not measured) output signal to noise (AWGN) ratio per symbol which directly relates with particularly used modulation technique. Theoretical (E_S/No) ratios are a priory known for each modulation vs. SER or BER. So, we have to fix reference SER or BER and take corresponding (E_S/No) value in dB for particular modulation.

For large energy-to-noise ratios, the symbol error performance $P_E(M)$, for equally likely, coherent detected M-ary PSK signaling, can be expressed [5] as

$$P_E(M) \approx 2Q\left(\sqrt{\frac{2E_s}{N_0}}\sin\frac{\pi}{M}\right)$$

Where $P_E(M)$ is the probability of symbol error, $E_S = E_B(\log_2 M)$ is the energy per symbol, and $M = 2^k$ is the size of the symbol set.

The symbol error performance for differentially coherent detection of M-ary DPSK (for large E_S/No) is similarly expressed [5] as

$$P_E(M) \approx 2Q\left(\sqrt{\frac{2E_s}{N_0}}\sin\frac{\pi}{\sqrt{2}M}\right)$$

For the same SER=1e-5 BPSK requires (E_b/N_O) = 10.0dB and QPSK (E_b/N_O) = 10.0dB. The BPSK modulation has 1 bit to 1 symbol and QPSK => 2 bits to 1 symbol representation, therefore for SER=1e-5:

BPSK => $(Es/N_O) = (E_b/N_O) + 10\log 1 = 10.0 + 0 = 10.0$dB;

QPSK => $(Es/N_O) = (E_b/N_O) + 10\log 2 = 10.0 + 3 = 13.0$dB.

The $P_E(M)$ performance curves for coherently detected MPSK signaling are plotted versus E_B/N_O in Figure 1 [6].

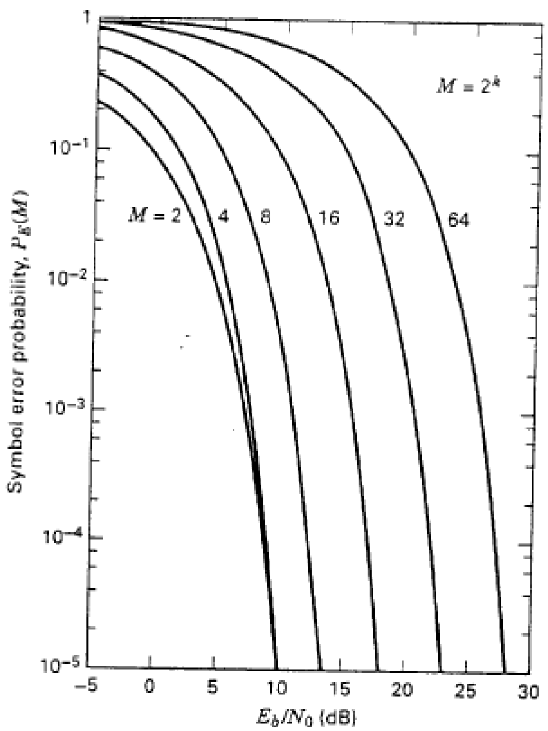

Figure 1 Symbol Error Rate for Coherently Detected Multiple Phase Signaling

The HFA3863 direct sequence spread spectrum baseband processor uses also CCK modulation, which is a form of M-ary Orthogonal Keying. Figure 2 shows a comparison of the measured Eb/N0 performance of HFA3863 in the two CCK modes against theoretical curves [7].

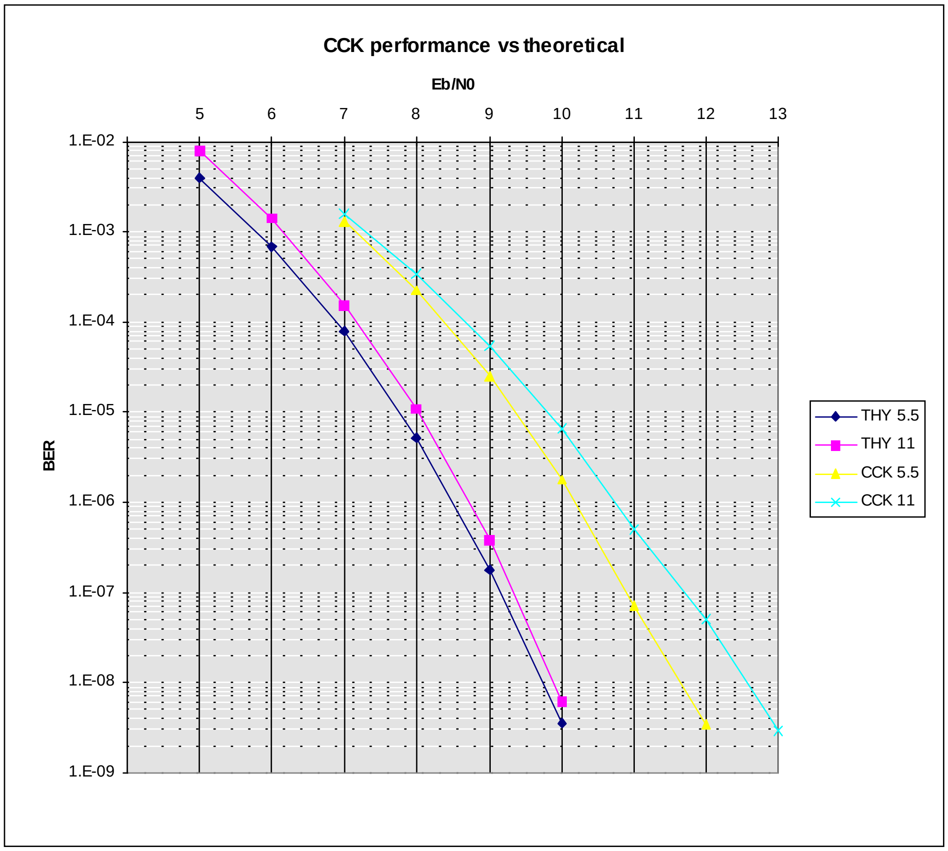

Figure 2 Bit Error Rate for Coherently Detected CCK Signaling

The (E_S/N_O) performance of the waveform can be calculated by adding 10 log(bits per symbol) or 6dB to the basic 5.5Mbps waveform to account for the 4 bits per symbol. For the 11Mbps case, add 9dB for 8 bits per symbol (10log(8) = 9 dB). This gives a required (E_b/N_O) of 7.8dB for the 5.5Mbps case and 8.0dB for the 11Mbps case (for the same BER=1e-5):

8CCK => $(Es/N_O) = (E_b/N_O) + 10\log4 = 7.8 + 6 = 13.8$dB;

64CCK => $(Es/N_O) = (E_b/N_O) + 10\log8 = 8.0 + 9 = 17.0$dB.

Note: The 8CCK (5.5Mb/s) requires 3dB less (E_S/N_O) than CCK 11Mb/s due to being half the data rate and an additional 0.2dB less due to coding gain achieved using the 4 best 8 chip orthogonal codes rather than 64 8 chip orthogonal codes [3].

1.1.1. Minimum Required Jammer to Signal Ratio

$$PG = (E_s/N_o) + (J/S) + L_{sys} = (E_s/N_o) + (J/S) + 2.0dB \geq 10dB$$
$$(J/S) \geq 10dB - (E_s/N_o) - L_{sys} = 10dB - (E_s/N_o) - 2.0dB$$

To meet the FCC requirement for 10dB Processing Gain, the minimum jammer to signal ratio must be as follows:

BPSK => $(J/S) = 10dB - 10.0dB - 2.0dB \geq -2.0dB$

QPSK => $(J/S) = 10dB - 13.0dB - 2.0dB \geq -5.0dB$

8CCK => $(J/S) = 10dB - 13.8dB - 2.0dB \geq -5.8dB$

64CCK => $(J/S) = 10dB - 17.0dB - 2.0dB \geq -9.0dB$